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# RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

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|---|---|---|---|---|---|---|
| Title | The errata of DAC, ADC and Electrical characteristics on the RA6T2 Group MCU Products | | Information Category | Technical Notification | | |
| Applicable Product | RA6T2 Group | Lot No.<br>All | Reference Document | RA6T2 Group User's Manual : Hardware Rev.1.30 | | |

This document describes the errata of DAC, ADC and Electrical characteristics in the RA6T2 Group User's Manual.

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## Before correction

Table 36.2 Association between ADC functions and ADC operation mode

| Function | | SAR mode | | Oversampling mode | | Hybrid mode | | |
|---|---|---|---|---|---|---|---|---|
| | | Single scan mode | Continuous scan mode | Single scan mode | Continuous scan mode | Single scan mode | Continuous scan mode | Background continuous scan mode |
| Analog input | Single-ended input | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Differential input | –*1 | –*1 | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Programmable gain amplifier | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Channel-dedicated sample-and-hold circuit | ✓ | – | – | – | ✓ | ✓ | ✓ |
| Diagnosis function/extended analog function | Disconnection detection assist function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | – |
| | Self-diagnosis | ✓ | ✓ | ✓ | – | ✓ | – | – |
| | Internal reference voltage | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Temperature sensor | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | D/A converter (DA0 to DA3) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Scanning operation | Group priority operation | ✓ | ✓ | – | – | – | – | – |
| | Multiple A/D converter synchronous operation | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Digital calculation | Digital filter function | – | – | ✓*2 | ✓*2 | ✓*2 | ✓*2 | ✓*2 |
| | User's gain/offset adjustment function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Addition/average function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Limiter clip function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Compare match function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| FIFO function | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note 1. As an exception, only in the self-diagnosis operation, the Differential input mode is supported.

Note 2. Use of the digital filter function is required when in Oversampling mode and Hybrid mode.

## After correction

Table 36.2 Association between ADC functions and ADC operation mode

| Function | | SAR mode | | Oversampling mode | | Hybrid mode | | |
|---|---|---|---|---|---|---|---|---|
| | | Single scan mode | Continuous scan mode | Single scan mode | Continuous scan mode | Single scan mode | Continuous scan mode | Background continuous scan mode |
| Analog input | Single-ended input | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Differential input | –*1 | –*1 | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Programmable gain amplifier | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Channel-dedicated sample-and-hold circuit | ✓ | – | – | – | ✓ | ✓ | ✓ |
| Diagnosis function/extended analog function | Disconnection detection assist function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | – |
| | Self-diagnosis | ✓ | ✓ | ✓ | – | ✓ | –*3 | –*3 |
| | Internal reference voltage | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Temperature sensor | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | D/A converter (DA0 to DA3) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Scanning operation | Group priority operation | ✓ | ✓ | – | – | – | – | – |
| | Multiple A/D converter synchronous operation | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Digital calculation | Digital filter function | – | – | ✓*2 | ✓*2 | ✓*2 | ✓*2 | ✓*2 |
| | User's gain/offset adjustment function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Addition/average function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Limiter clip function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | Compare match function | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| FIFO function | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note 1. As an exception, only in the self-diagnosis operation, the Differential input mode is supported.

Note 2. Use of the digital filter function is required when in Oversampling mode and Hybrid mode.

Note 3. As an exception, Continuous scan mode and Background continuous scan mode are supported only when using dummy conversion channels with the channel-dedicated sample-and-hold circuit.
For details, see "36.3.16.3(1) Limitations on usage of channel-dedicated sample-and-hold circuit in Hybrid mode.

## Before correction

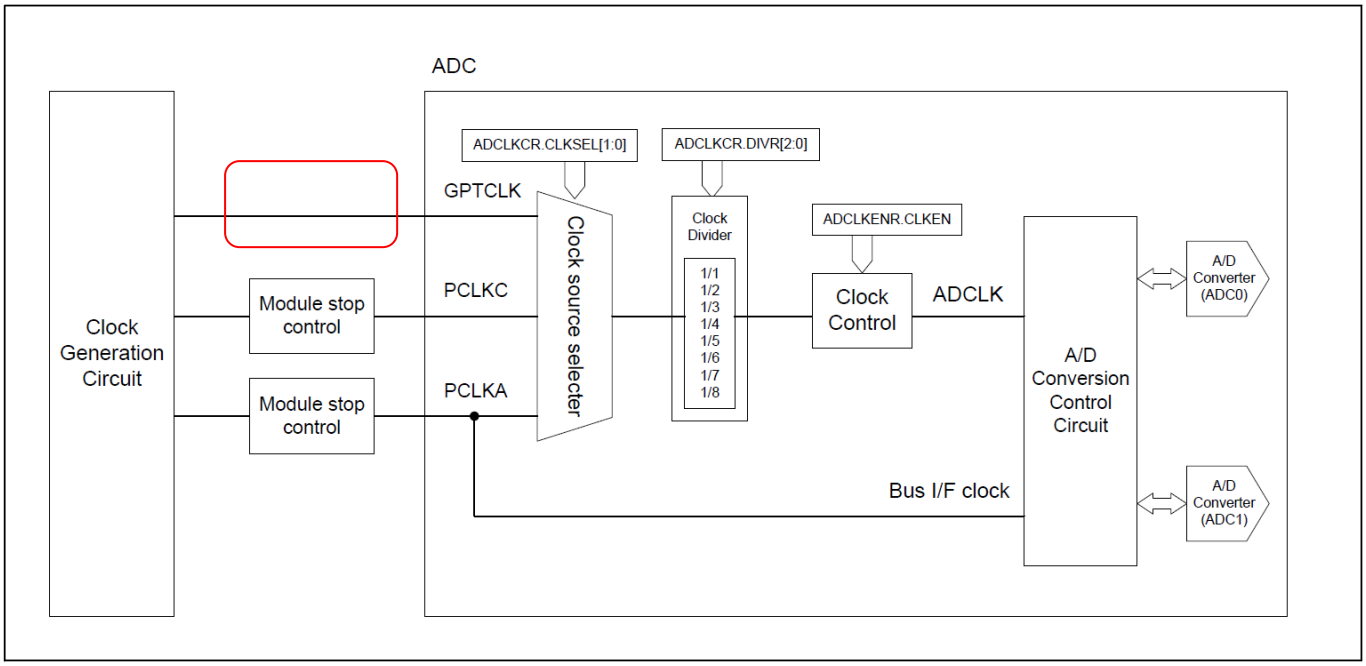


Figure 36.4 Clock structure

## After correction

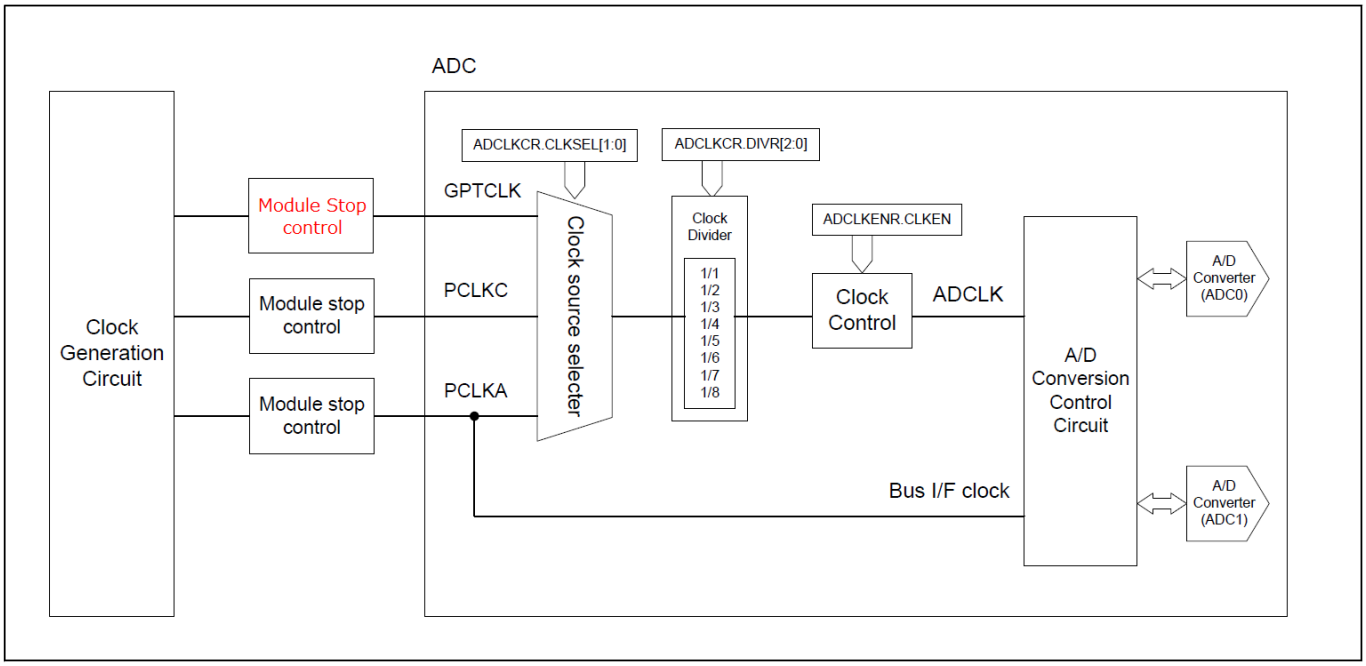


Figure 36.4 Clock structure

## Before correction

Table 36.12 Example of the scanning operation in Hybrid mode – Continuous scan mode

| step | Operation |
|---|---|
| 1 | When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group corresponding to the trigger is started.<br>When scanning operation starts, ADGRSR.ACTGRn (n = 0 to 8) corresponding to that scan group is set to 1.<br>ADSR.ADACTm(m = 0, 1) bit corresponding to the A/D converter performing the A/D conversion is also set to 1. |
| 2 | In Hybrid mode, the scanning operation is performed while switching analog channels every time oversampling is performed. |
| 3 | After the oversampling corresponding to the number of TAPs of the digital filter and the number of A/D-converted value addition/averaging times is performed to each analog channel, A/D conversion data is output. (The time taken for the oversampling required to obtain the first A/D conversion data is called the initial delay time.)<br>The A/D conversion data is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If FIFO is used, A/D conversion data is also stored in FIFO data register (ADFIFODRk (k = 0 to 8)). |
| 4 | If the scan end interrupt is enabled, the scan end interrupt corresponding to that scan group is generated when the A/D conversion of all virtual channels assigned to that scan group is completed. |
| 5 | The second and subsequent rounds of scanning operations are performed while the oversampling data stored in the digital filter is retained.<br>Each one time oversampling or each multiple times oversampling corresponding to the number of A/D-converted value addition/averaging times is performed for each analog channel, the next A/D conversion data is output. (The time taken for the oversampling required to obtain the second and subsequent A/D conversion data in continuous scan operation is called the group delay time.)<br>The A/D conversion data is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If FIFO is used, A/D conversion data is also stored in FIFO data register (ADFIFODRk (k = 0 to 8)). |
| 6 | If the scan end interrupt is enabled, the scan end interrupt corresponding to that scan group is generated when the A/D conversion of all virtual channels assigned to that scan group is completed. |
| 7 | Thereafter, until the A/D conversion stop process is performed, Step 5 to 6 are repeated, and the scanning operation continues. To stop the A/D conversion, you must follow to section 36.5.4. Force Stops the A/D Conversion Operation. |

## After correction

Table 36.12 Example of the scanning operation in Hybrid mode – Continuous scan mode

| step | Operation |
|---|---|
| 1 | When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group corresponding to the trigger is started.<br>When scanning operation starts, ADGRSR.ACTGRn (n = 0 to 8) corresponding to that scan group is set to 1.<br>ADSR.ADACTm(m = 0, 1) bit corresponding to the A/D converter performing the A/D conversion is also set to 1. |
| 2 | In Hybrid mode, the scanning operation is performed while switching analog channels every time oversampling is performed. |
| 3 | After the oversampling corresponding to the number of TAPs of the digital filter and the number of A/D-converted value addition/averaging times is performed to each analog channel, A/D conversion data is output. (The time taken for the oversampling required to obtain the first A/D conversion data is called the initial delay time.)<br>The A/D conversion data is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If FIFO is used, A/D conversion data is also stored in FIFO data register (ADFIFODRk (k = 0 to 8)). |
| 4 | If the scan end interrupt is enabled, the scan end interrupt corresponding to that scan group is generated when the A/D conversion of all virtual channels assigned to that scan group is completed. |
| 5 | In scanning operation after the initial delay time has elapsed, each time oversampling is performed for each analog channel, the data in the digital filter is updated. The updated A/D conversion data for each analog channel can be output each one time oversampling or each multiple times oversampling corresponding to the number of A/D-converted value addition/averaging times is performed.<br>The A/D conversion data is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If FIFO is used, A/D conversion data is also stored in FIFO data register (ADFIFODRk (k = 0 to 8)). |
| 6 | If the scan end interrupt is enabled, the scan end interrupt corresponding to that scan group is generated when the A/D conversion of all virtual channels assigned to that scan group is completed. |
| 7 | Thereafter, until the A/D conversion stop process is performed, Step 5 to 6 are repeated, and the scanning operation continues. To stop the A/D conversion, you must follow to section 36.5.4. Force Stops the A/D Conversion Operation. |

## Before correction

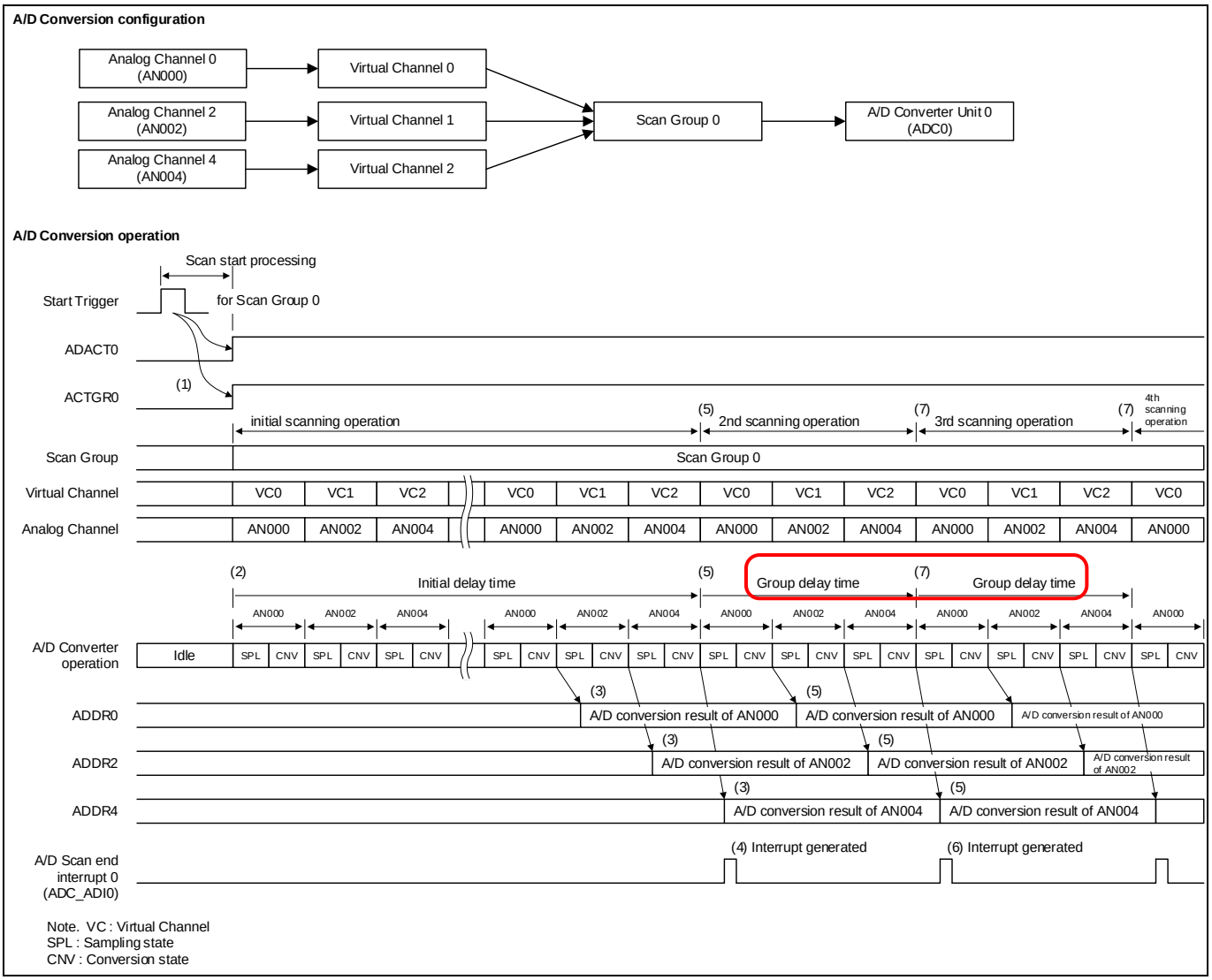


Figure 36.12 Example of the scanning operation in Hybrid mode – Continuous scan mode

## After correction

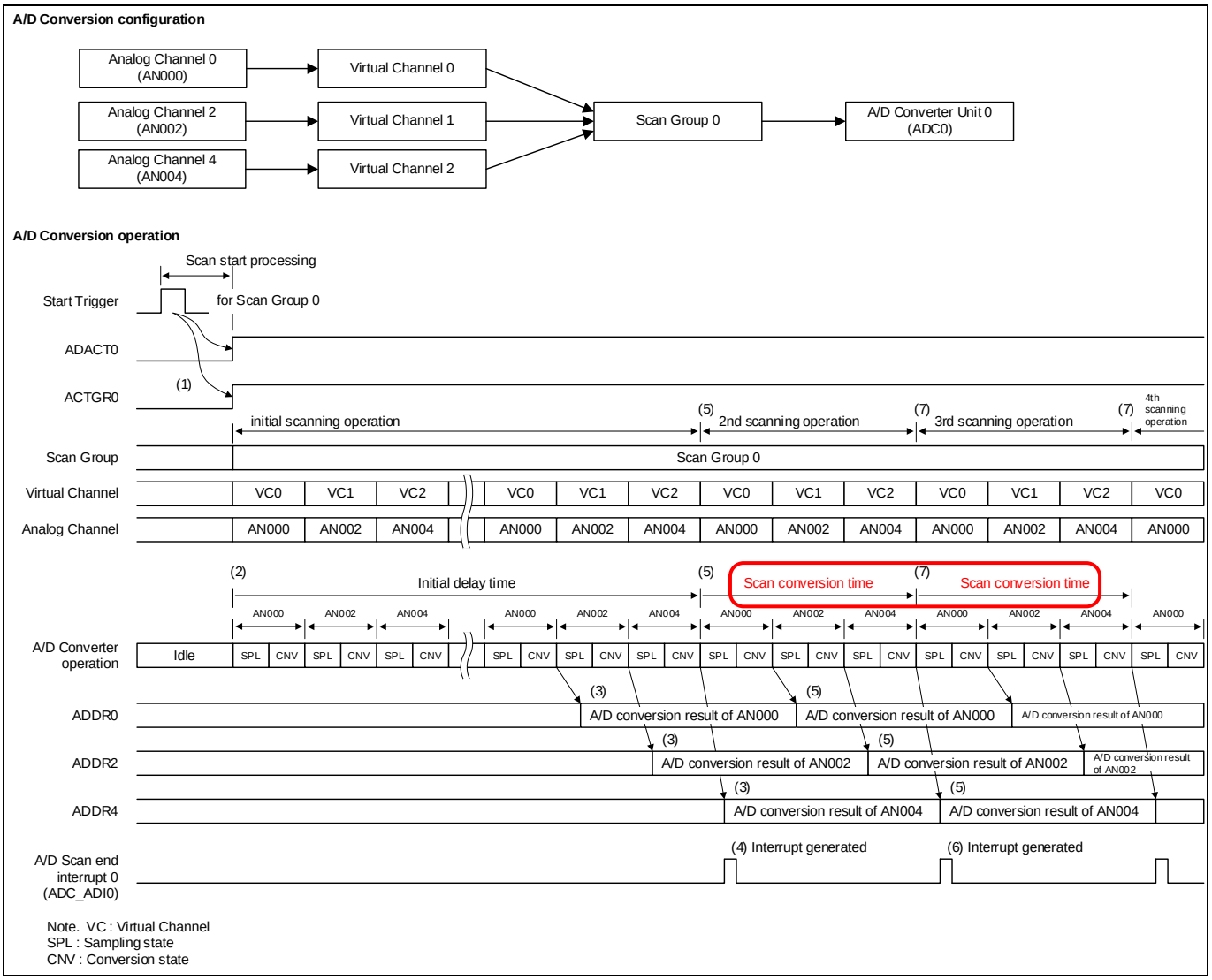


Figure 36.12 Example of the scanning operation in Hybrid mode – Continuous scan mode

## Before correction

Table 36.13 Example of the scanning operation in Hybrid mode – Background continuous scan mode

| Step | Operation |
|---|---|
| 1 | When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group corresponding to the trigger is started.<br>When scanning operation starts, ADGRSR.ACTGRn (n = 0 to 8) corresponding to that scan group is set to 1. ADSR.ADACTm (m = 0, 1) bit corresponding to the A/D converter performing the A/D conversion is also set to 1. |
| 2 | In Hybrid mode, the scanning operation is performed while switching analog channels every time oversampling is performed. |
| 3 | After the oversampling corresponding to the number of TAPs of the digital filter and the number of A/D-converted value addition/averaging times is performed to each analog channel, A/D conversion data becomes in ready to be output.<br>(The time taken for the oversampling required to obtain the first A/D conversion data is called the initial delay time. In the background continuous scan operation, A/D conversion data can be obtained after the initial delay time has elapsed from the start of the scanning operation.) |
| 4 | The second and subsequent rounds of scanning operations are performed while the oversampling data stored in the digital filter is retained. Each time oversampling is performed for each analog channel, the data in the digital filter is updated. Each one time oversampling or each multiple times oversampling corresponding to the number of A/D-converted value addition/averaging times is performed for each analog channel, the next A/D conversion data becomes in ready to be output.<br>(The time taken for the oversampling required to obtain the second and subsequent A/D conversion data in continuous scan operation is called the group delay time. In background continuous scan operation, after the initial delay time has elapsed from the start of the scanning operation, the updated A/D conversion data can be obtained every time the group delay time elapses.) |
| 5 | When an A/D conversion start trigger is input during background continuous scanning operation, the most recent A/D conversion data at that time is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If FIFO function is set to enabled, A/D conversion data is also stored in the FIFO data register (ADFIFODRk (k = 0 to 8)). |
| 6 | If scan end interrupt is set to enable, scan end interrupt is generated. |
| 7 | Thereafter, until the A/D conversion stop process is performed, Background continuous scanning operation (Step 4) is repeated. And whenever the A/D conversion start trigger is input during Background continuous scanning operation, the A/D conversion data is output (Step 5 and Step 6). To stop A/D conversion, you must follow to section 36.5.4. Force Stops the A/D Conversion Operation. |

## After correction

Table 36.13 Example of the scanning operation in Hybrid mode – Background continuous scan mode

| Step | Operation |
|---|---|
| 1 | When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group corresponding to the trigger is started.<br>When scanning operation starts, ADGRSR.ACTGRn (n = 0 to 8) corresponding to that scan group is set to 1. ADSR.ADACTm (m = 0, 1) bit corresponding to the A/D converter performing the A/D conversion is also set to 1. |
| 2 | In Hybrid mode, the scanning operation is performed while switching analog channels every time oversampling is performed. |
| 3 | After the oversampling corresponding to the number of TAPs of the digital filter and the number of A/D-converted value addition/averaging times is performed to each analog channel, A/D conversion data becomes in ready to be output.<br>(The time taken for the oversampling required to obtain the first A/D conversion data is called the initial delay time. In the background continuous scan operation, A/D conversion data can be obtained after the initial delay time has elapsed from the start of the scanning operation.) |
| 4 | In scanning operation after the initial delay time has elapsed, each time oversampling is performed for each analog channel, the data in the digital filter is updated. The updated A/D conversion data for each analog channel can be output each one time oversampling or each multiple times oversampling corresponding to the number of A/D-converted value addition/averaging times is performed. |
| 5 | When an A/D conversion start trigger is input during background continuous scanning operation, the most recent A/D conversion data at that time is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If FIFO function is set to enabled, A/D conversion data is also stored in the FIFO data register (ADFIFODRk (k = 0 to 8)). |
| 6 | If scan end interrupt is set to enable, scan end interrupt is generated. |
| 7 | Thereafter, until the A/D conversion stop process is performed, Background continuous scanning operation (Step 4) is repeated. And whenever the A/D conversion start trigger is input during Background continuous scanning operation, the A/D conversion data is output (Step 5 and Step 6). To stop A/D conversion, you must follow to section 36.5.4. Force Stops the A/D Conversion Operation. |

## Before correction

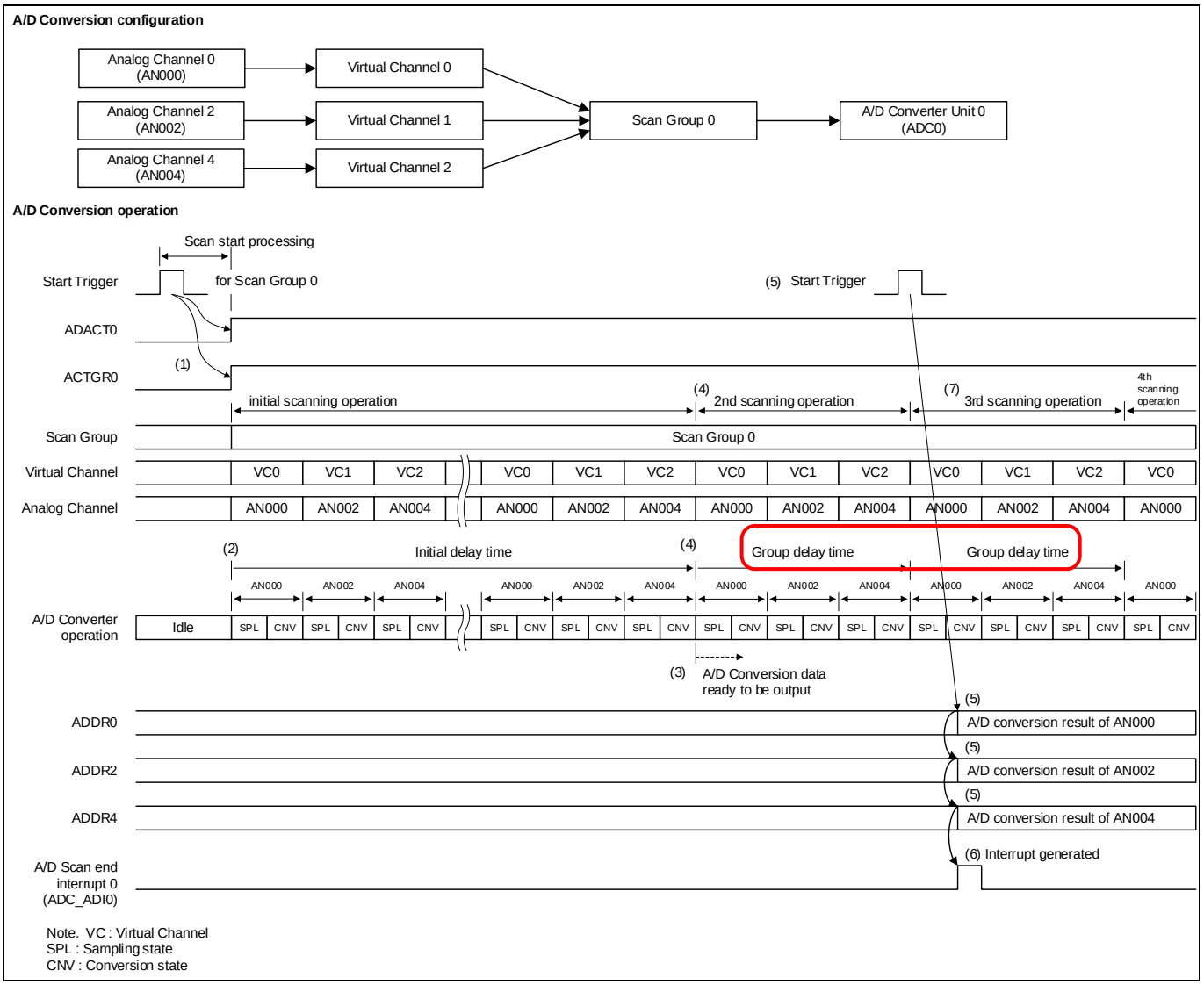


Figure 36.13 Example of the scanning operation in Hybrid mode – Background continuous scan mode

## After correction

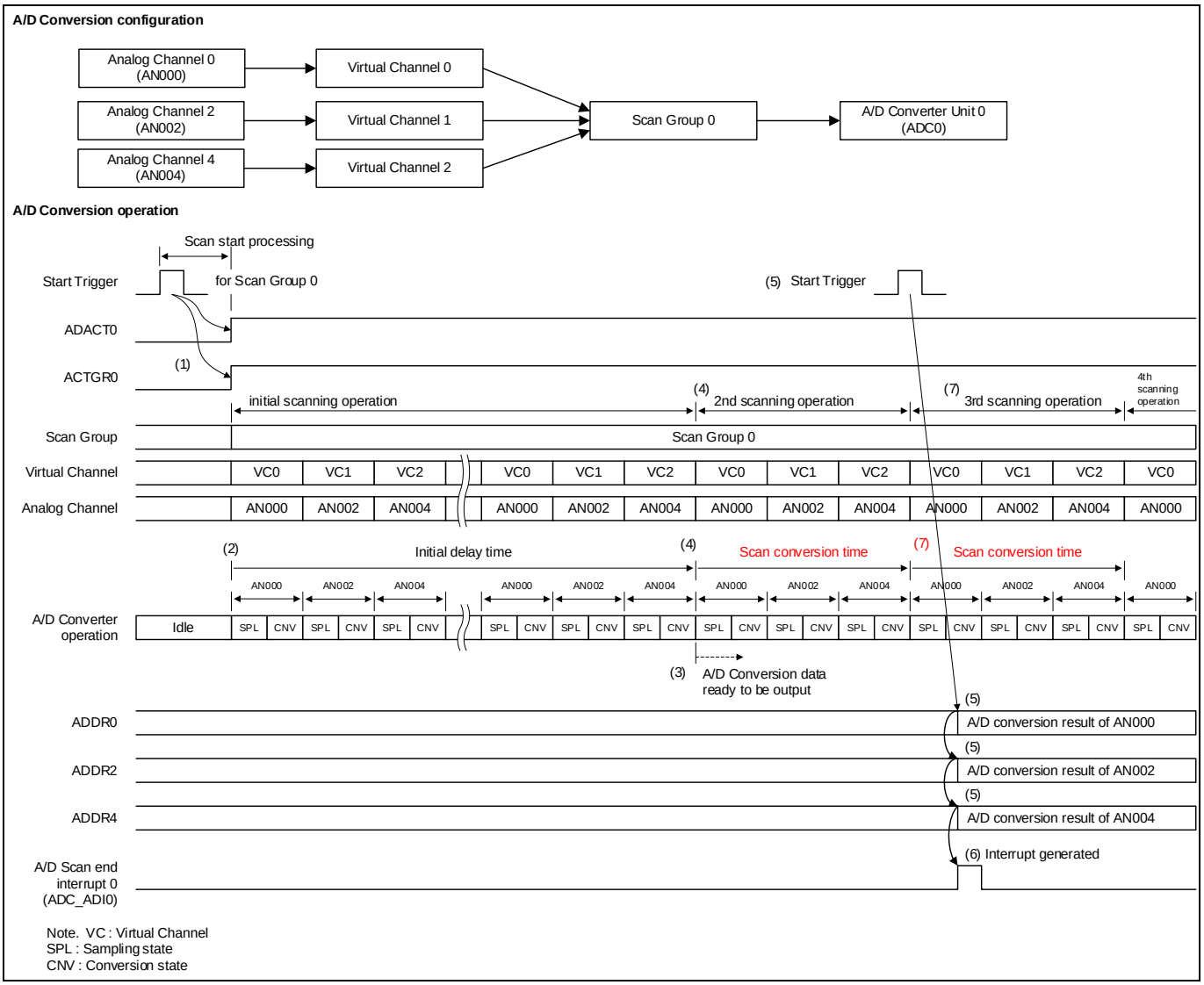


Figure 36.13 Example of the scanning operation in Hybrid mode – Background continuous scan mode

## Before correction

Table 36.16 List of operation mode for which the self-diagnostic function is available

| Operation mode – Scan mode | Self-diagnosis Function |
|---|---|
| SAR mode - Single scan mode | ✓ |
| SAR mode - Continuous scan mode | - |
| Oversampling mode - Single scan mode | ✓ |
| Oversampling mode - Continuous scan mode | - |
| Hybrid mode - Single scan mode | ✓ |
| Hybrid mode - Continuous scan mode | - |
| Hybrid mode - Background continuous scan mode | - |

Note: ✓: Available, —: Not Available

## After correction

Table 36.16 List of operation mode for which the self-diagnostic function is available

| Operation mode – Scan mode | Self-diagnosis Function |
|---|---|
| SAR mode - Single scan mode | ✓ |
| SAR mode - Continuous scan mode | ✓ |
| Oversampling mode - Single scan mode | ✓ |
| Oversampling mode - Continuous scan mode | - |
| Hybrid mode - Single scan mode | ✓ |
| Hybrid mode - Continuous scan mode | –*1 |
| Hybrid mode - Background continuous scan mode | –*1 |

Note: ✓: Available, —: Not Available

Note 1. As an exception, Continuous scan mode and Background continuous scan mode are supported only when using dummy conversion channels with the channel-dedicated sample-and-hold.
For details, see "36.3.16.3(1) Limitations on usage of channel-dedicated sample-and-hold circuit in Hybrid mode.

## Before correction

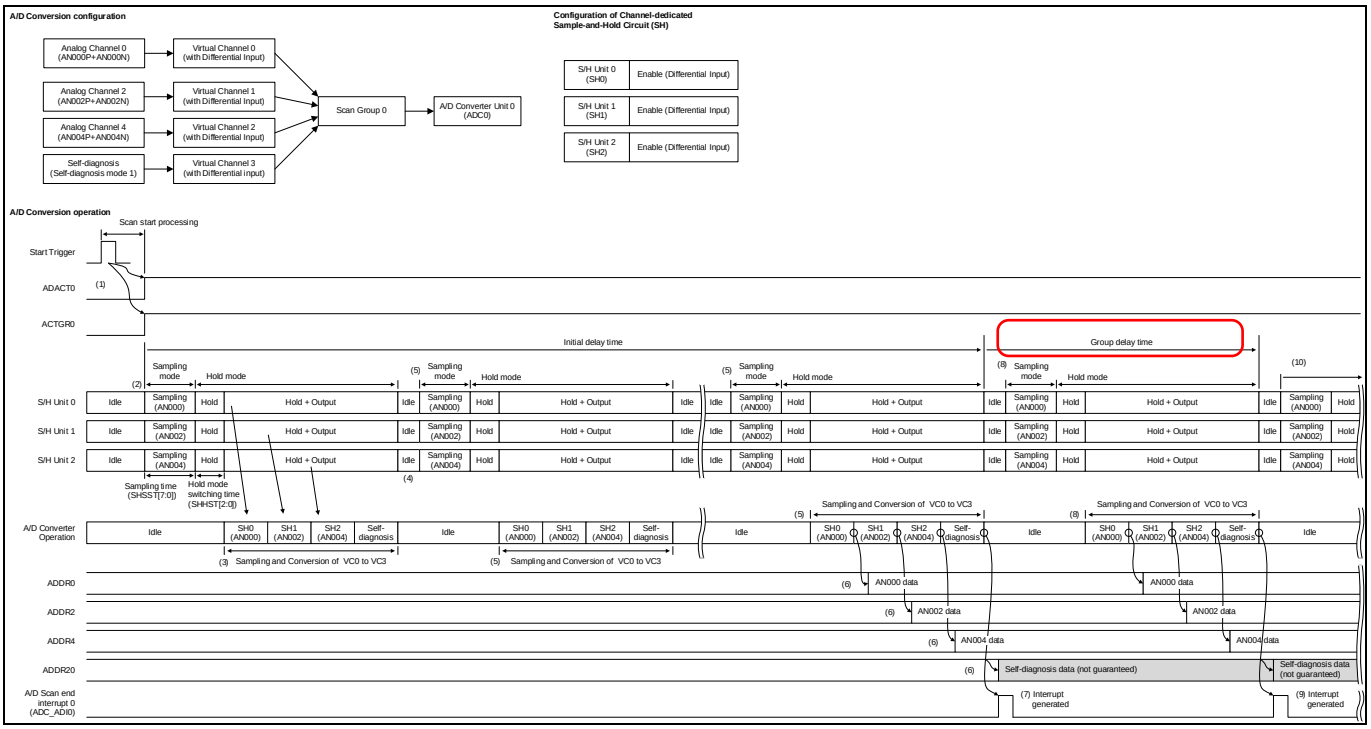


Figure 36.21 Basic operation of channel-dedicated sample-and-hold circuit in Hybrid mode – Continuous scan mode

## After correction

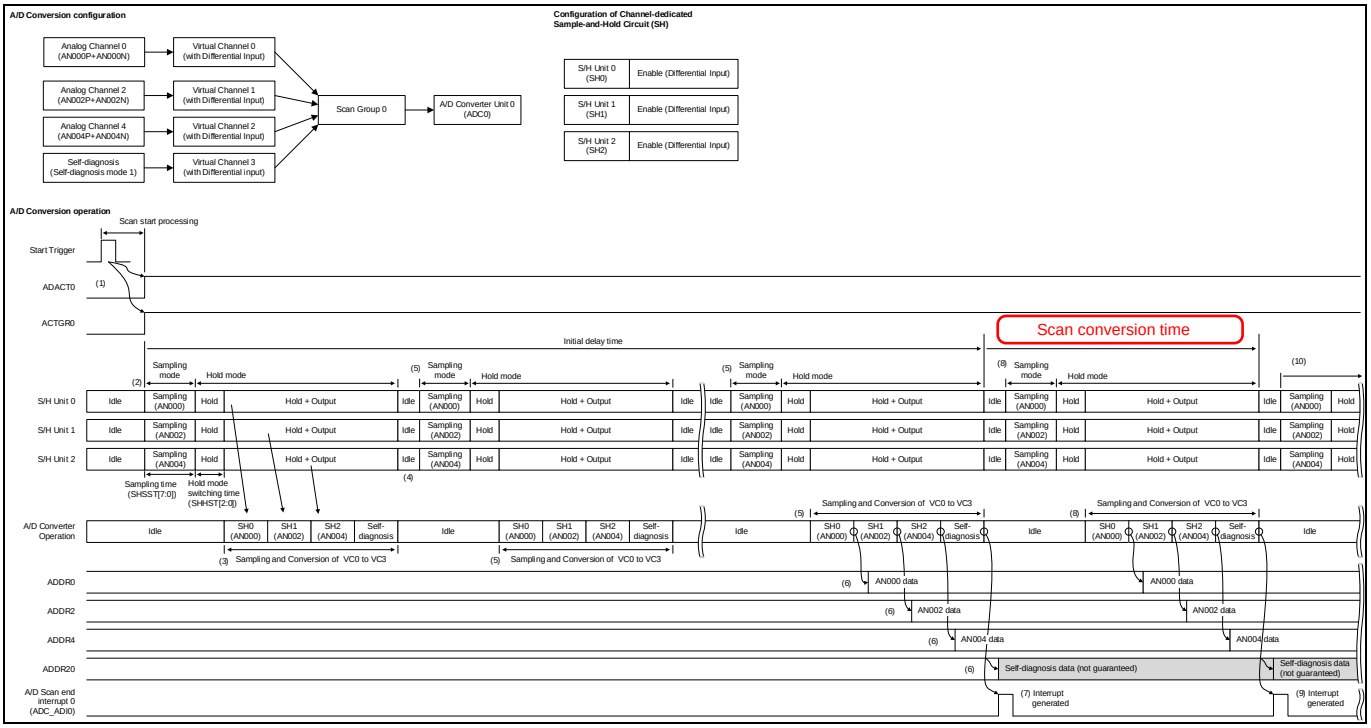


Figure 36.21 Basic operation of channel-dedicated sample-and-hold circuit in Hybrid mode – Continuous scan mode

## Before correction

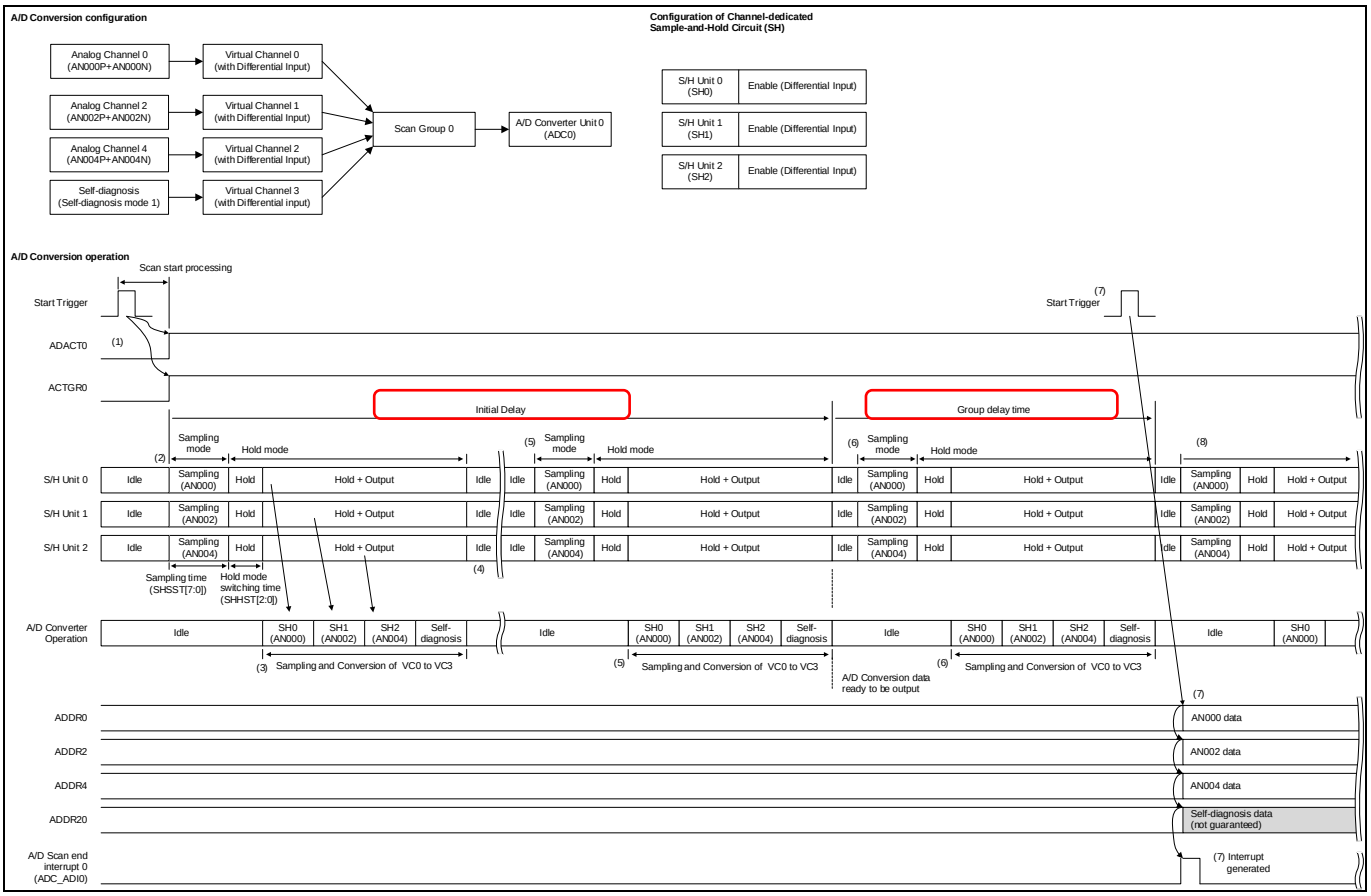


Figure 36.22 Basic operation of channel-dedicated sample-and-hold circuit in Hybrid mode – Background continuous scan mode

## After correction

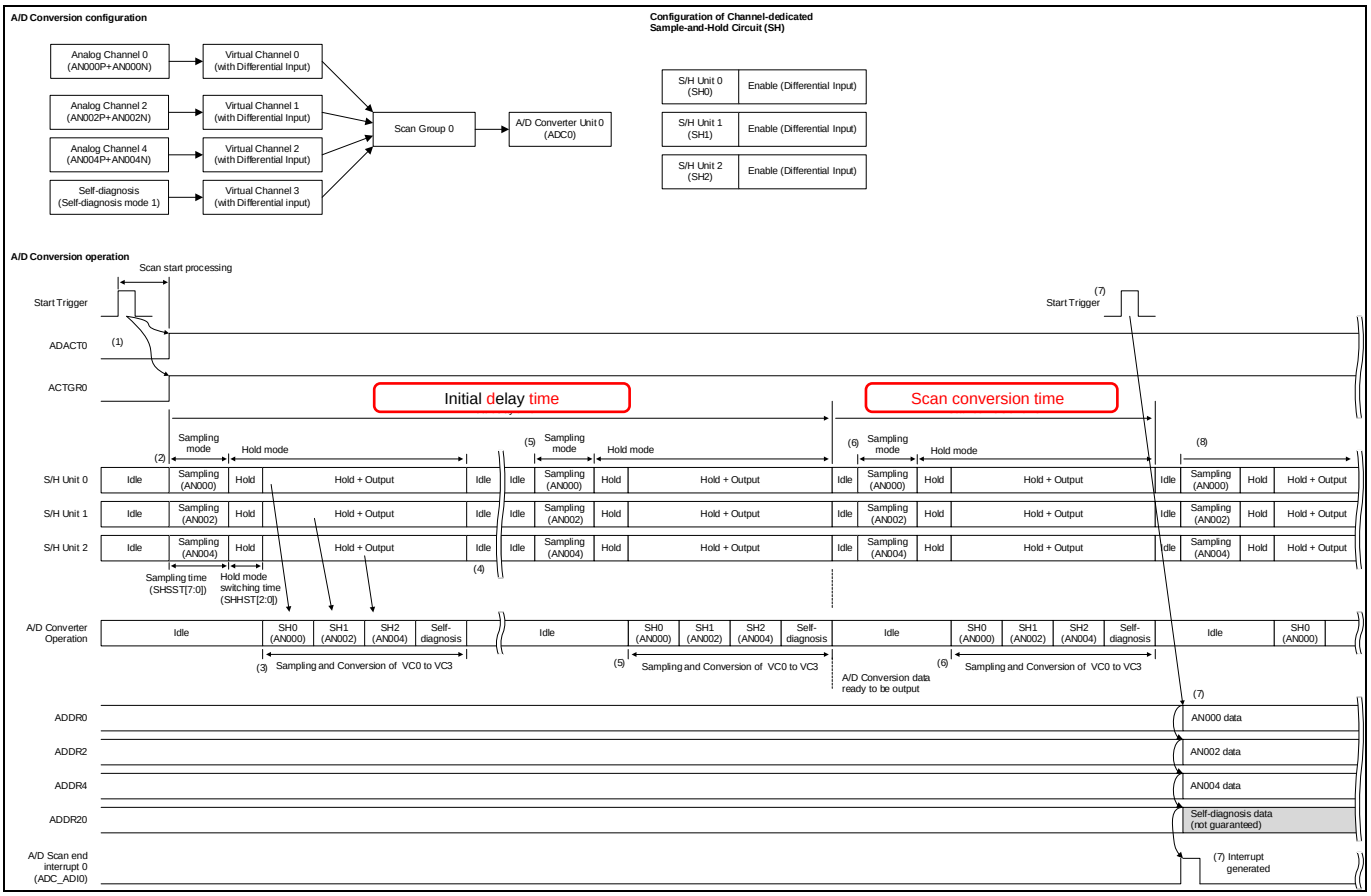


Figure 36.22 Basic operation of channel-dedicated sample-and-hold circuit in Hybrid mode – Background continuous scan mode

## Before correction

Table 36.51 Initial setup procedure

| No. | Step | Description |
|---|---|---|
| 1 | Release module-stop | Release the module-stop bit for ADC in MSTPCR register. |
| 2 | I/O port configuration | Set ASEL bit of the pin used as analog input to 1. |
| 3 | Synchronous operation configuration | Set the synchronous operation function.<br>The synchronous operation function is enabled at the initial value of the register after reset release. If the synchronous operation function is not used, be sure to disable the synchronous operation function (ADSYCR.ADSYDISm = 1 (m = 0, 1)). |
| 4 | ADCLK configuration | Set the clock source and division ratio for ADCLK.<br>Then, set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1). |
| 5 | A/D conversion configuration | Configure the A/D conversion settings. |
| 6 | Wait for operation stabilization | Wait until the operating stabilization times specified in the Electrical Characteristics have elapsed. |
| 7 | Self-calibration | Self-calibration must be executed prior to starting A/D conversion.<br>Set up for self-calibration and execute it.<br>For details, see section 36.3.8. Self-calibration. |
| 8 | Trigger configuration | To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group. |
| 9 | Start of A/D conversion | When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts. |

## After correction

Table 36.51 Initial setup procedure

| No. | Step | Description |
|---|---|---|
| 1 | Release module-stop | Release the module-stop bit for ADC in MSTPCR register. |
| 2 | I/O port configuration | Set ASEL bit of the pin used as analog input to 1. |
| 3 | Synchronous operation configuration | Set the synchronous operation function.<br>The synchronous operation function is enabled at the initial value of the register after reset release. If the synchronous operation function is not used, be sure to disable the synchronous operation function (ADSYCR.ADSYDISm = 1 (m = 0, 1)). |
| 4 | ADCLK configuration | Set the clock source and division ratio for ADCLK. *1<br>Then, set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1). |
| 5 | A/D conversion configuration | Configure the A/D conversion settings. |
| 6 | Wait for operation stabilization | Wait until the operating stabilization times specified in the Electrical Characteristics have elapsed. |
| 7 | Self-calibration | Self-calibration must be executed prior to starting A/D conversion.<br>Set up for self-calibration and execute it.<br>For details, see section 36.3.8. Self-calibration. |
| 8 | Trigger configuration | To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group. |
| 9 | Start of A/D conversion | When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts. |

Note 1. When GPTCLK is selected, release the GPT module stop state using the module stop register E (MSTPCRE). For details, see section 10, Low Power Modes.

## Before correction

Table 36.52 Procedure for changing ADCLK setting

| No. | Step | Description |
|---|---|---|
| 1 | Disable trigger input | Disables the trigger input from the peripheral module.<br>(Write ADTRGENR.STTRGENn = 0 (n = 0 to 8)) |
| 2 | Stop A/D conversion | Check that all A/D converter is stopped.<br>When A/D conversion is in progress, wait until all A/D conversion is completed or forcibly stop A/D conversion operation.<br>For details about forcibly stop A/D conversion operation, see section 36.5.4. Force Stops the A/D Conversion Operation. |
| 3 | Stop ADCLK supplies | Set ADCLKENR.CKEN bit to 0. Then, wait for ADCLK to stop (ADCLKSR.CLKSR = 0). |
| 4 | Change ADCLK setting | Change the clock-source and the division ratio for ADCLK. |
| 5 | Started supplying ADCLK | Set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1). |
| 6 | Change the A/D conversion configuration | Change the following settings according to the changed ADCLK frequency.<br>• Successive approximation time for A/D converter<br>• Number of sampling states for A/D conversion<br>• Number of sampling states and hold mode switching states for channel-dedicated sample-and-hold circuit *1<br>• Number of states for self-calibration operation (A/D converter and channel-dedicated sample-and-hold circuit *1)<br>• Synchronous operation period *2<br>• Disconnection detection assist period *3<br>If other settings related to A/D conversion are also to be changed, change them in this step. |
| 7 | Wait for operation stabilization | Wait until the operating stabilization times specified in the section 46, Electrical Characteristics have elapsed. |
| 8 | Self-calibration | Execute self-calibration operation prior to starting A/D conversion. For details, see section 36.3.8. Self-calibration. |
| 9 | Trigger configuration | To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group. |
| 10 | Start of A/D conversion | When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts. |

Note 1. Setting is not required when channel-dedicated sample-and-hold circuit is not used.
Note 2. No change is required when synchronous operation setting is disabled (ADSYCR, ADSYDISm = 1 (m = 0, 1))
Note 3. Setting is not required when disconnection detection assist function is not used.

## After correction

Table 36.52 Procedure for changing ADCLK setting

| No. | Step | Description |
|---|---|---|
| 1 | Disable trigger input | Disables the trigger input from the peripheral module.<br>(Write ADTRGENR.STTRGENn = 0 (n = 0 to 8)) |
| 2 | Stop A/D conversion | Check that all A/D converter is stopped.<br>When A/D conversion is in progress, wait until all A/D conversion is completed or forcibly stop A/D conversion operation.<br>For details about forcibly stop A/D conversion operation, see section 36.5.4. Force Stops the A/D Conversion Operation. |
| 3 | Stop ADCLK supplies | Set ADCLKENR.CKEN bit to 0. Then, wait for ADCLK to stop (ADCLKSR.CLKSR = 0). |
| 4 | Change ADCLK setting | Change the clock-source and the division ratio for ADCLK. *4 |
| 5 | Started supplying ADCLK | Set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1). |
| 6 | Change the A/D conversion configuration | Change the following settings according to the changed ADCLK frequency.<br>• Successive approximation time for A/D converter<br>• Number of sampling states for A/D conversion<br>• Number of sampling states and hold mode switching states for channel-dedicated sample-and-hold circuit *1<br>• Number of states for self-calibration operation (A/D converter and channel-dedicated sample-and-hold circuit *1)<br>• Synchronous operation period *2<br>• Disconnection detection assist period *3<br>If other settings related to A/D conversion are also to be changed, change them in this step. |
| 7 | Wait for operation stabilization | Wait until the operating stabilization times specified in the section 46, Electrical Characteristics have elapsed. |
| 8 | Self-calibration | Execute self-calibration operation prior to starting A/D conversion. For details, see section 36.3.8. Self-calibration. |
| 9 | Trigger configuration | To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group. |
| 10 | Start of A/D conversion | When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts. |

Note 1. Setting is not required when channel-dedicated sample-and-hold circuit is not used.
Note 2. No change is required when synchronous operation setting is disabled (ADSYCR, ADSYDISm = 1 (m = 0, 1))
Note 3. Setting is not required when disconnection detection assist function is not used.
Note 4. When GPTCLK is selected, release the GPT module stop state using the module stop register E (MSTPCRE). For details, see section 10, Low Power Modes.

## Before correction

Table 36.56 A/D conversion processing time

| Item | | | Symbol | Processing Time |
|---|---|---|---|---|
| Channel-dedicated sample-and-hold processing time | Sampling time | | $t_{SH\_SPL}$ | ADSHSTRm.SHSST[7:0] × ADCLK |
| | Hold mode switching time | | $t_{SH\_HLD}$ | ADSHSTRm.SHHST[2:0] × ADCLK |
| | Sampling mode switching time (only when Hybrid mode) | | $t_{SH\_D}$ | (ADSYCR.ADSYCYC[10:0] - 1) × ADCLK |
| Disconnection detect assist processing time | | | $t_{DDA}$ | [When disconnection detect assist function is disabled]<br>● 0<br>[When disconnection detect assist function is enabled]<br>● ADSGDCRn.ADNDIS[3:0] × ADCLK |
| A/D conversion time | Sampling time | | $t_{AD\_SPL}$ | ADSSTRp.SSTq[9:0] × ADCLK |
| | Successive approximation time | | $t_{AD\_CNV}$ | ADCNVSTR.CSTm[5:0] × ADCLK |
| A/D conversion data processing time | SAR mode (Not using digital filter function) | When ADCLK = PCLKA/1 is set[*1] | $t_{ADDP}$ | [When A/D-converted value addition/averaging function is not used]<br>● 6 ADCLK + 2 PCLKA<br>[When A/D-converted value addition/averaging function is used]<br>● 7 ADCLK + 2 PCLKA |
| | | Other than above | | [When A/D-converted value addition/averaging function is not used]<br>● 7 ADCLK + (5～6 PCLKA)<br>[When A/D-converted value addition/averaging function is used]<br>● 8 ADCLK + (5～6 PCLKA) |
| | Oversampling mode or Hybrid mode (Using with digital filter function) | When ADCLK = PCLKA/1 is set[*1] | | [When A/D-converted value addition/averaging function is not used]<br>● 8 ADCLK + 2 PCLKA<br>[When A/D-converted value addition/averaging function is used]<br>● 9 ADCLK + 2 PCLKA |
| | | Other than above | | [When A/D-converted value addition/averaging function is not used]<br>● 9 ADCLK + 5～6 PCLKA<br>[When A/D-converted value addition/averaging function is used]<br>● 10 ADCLK + 5～6 PCLKA |
| Total A/D conversion time (SAR mode)[*3] | Channel conversion time[*2] | | $t_{ADCH\_S}$ | $(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times N_{ADC} \times$ ADCLK |
| | Scan conversion time[*4] | | $t_{SCAN\_S}$ | [When channel-dedicated sample-and-hold circuit is not used]<br>● $\Sigma t_{ADCH\_S}$<br>[When channel-dedicated sample-and-hold circuit is used]<br>● $t_{SH\_SPL} + t_{SH\_HLD} + \Sigma t_{ADCH\_S}$ |
| Total A/D conversion time (Oversampling mode)[*3] | Oversampling period | | $t_{OV\_OS}$ | $(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times$ ADCLK |
| | Channel conversion time | | $t_{ADCH\_O}$ | $(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times (N_{TAP} + N_{ADC}) \times$ ADCLK |
| | Scan conversion time[*5] | | $t_{SCAN\_O}$ | $\Sigma t_{ADCH\_O}$ |
| Total A/D conversion time (Hybrid mode)[*3] | Channel-dedicated sample-and-hold processing time in Hybrid mode | | $t_{HY\_SH}$ | $t_{SH\_SPL} + t_{SH\_HLD} + t_{SH\_D}$ |
| | Oversampling period | | $t_{HY\_OS}$ | $(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times$ ADCLK |

| | | | | |
|---|---|---|---|---|
| | Scan conversion time | Initial delay | $t_{HY\_ID}$ | [When channel-dedicated sample-and-hold circuit is not used]<br>●( $N_{TAP}$ + $N_{ADC}$ ) × $\Sigma t_{HY\_OS}$ *6<br>[When channel-dedicated sample-and-hold circuit is used]<br>●( $t_{HY\_SH}$ × ($N_{ADC}$ + $N_{TAP}$ ) - $t_{SH\_D}$ ) + ( $N_{TAP}$ + $N_{ADC}$ ) × $\Sigma t_{HY\_OS}$ *6 |
| | | Group delay | $t_{HY\_GD}$ | [When channel-dedicated sample-and-hold circuit is not used]<br>●$\Sigma t_{HY\_OS}$ *6<br>[When channel-dedicated sample-and-hold circuit is used]<br>● $t_{HY\_SH}$ + $\Sigma t_{HY\_OS}$ *6 |

Note: n = 0～8、m = 0、1、p = 0～7、q = 0～15

$N_{ADC}$ : This value is the number of the times of the addition/averaging according to the setting value of ADDOPCRBx.ADC[3:0] (x = 0 to 36). If A/D-converted value addition/averaging function is not used, this value is 1.

$N_{TAP}$ : This value is the number of TAP of the digital filter that selected in ADDOPCRAx.DFSEL[2:0] (x = 0 to 36) and ADDFSRm.DFSELy[1:0] (m = 0, 1, y = 0 to 4).

$N_{SGCH}$ : This value is the number of the channels in the scan group.

Note 1. When ADCLKCR.CLKSEL[1:0] = 10b and ADCLKCR.DIVR[2:0] = 000b are set.
Note 2. It does not include the channel-dedicated sample-and-hold processing time.
Note 3. It does not include the A/D conversion data processing time.
Note 4. This is the sum of the channel conversion times ($t_{ADCH\_N}$) that calculated from the conversion settings for each analog channel assigned to the scan group. If channel-dedicated sample-and-hold circuits are used, channel-dedicated sample-and-hold processing times ($t_{SH\_SPL}$ and $t_{SH\_HLD}$) are also added.
Note 5. This is the sum of the channel conversion times ($t_{ADCH\_O}$) that calculated from the conversion settings for each analog channel assigned to the scan group.
Note 6. This is the sum of the oversampling period ($t_{HY\_OS}$) that calculated from the conversion settings for each analog channel assigned to the scan group.

## After correction

Table 36.56 A/D conversion processing time

| Item | | | Symbol | Processing Time |
|---|---|---|---|---|
| Channeldedicated sample-and-hold processing time | Sampling time | | $t_{SH\_SPL}$ | ADSHSTRm.SHSST[7:0] × ADCLK |
| | Hold mode switching time | | $t_{SH\_HLD}$ | ADSHSTRm.SHHST[2:0] × ADCLK |
| | Sampling mode switching time (only when Hybrid mode) | | $t_{SH\_D}$ | (ADSYCR.ADSYCYC[10:0] - 1) × ADCLK |
| Disconnection detect assist processing time | | | $t_{DDA}$ | [When disconnection detect assist function is disabled]<br>● 0<br>[When disconnection detect assist function is enabled]<br>● ADSGDCRn.ADNDIS[3:0] × ADCLK |
| A/D conversion time | Sampling time | | $t_{AD\_SPL}$ | ADSSTRp.SSTq[9:0] × ADCLK |
| | Successive approximation time | | $t_{AD\_CNV}$ | ADCNVSTR.CSTm[5:0] × ADCLK |
| A/D conversion data processing time | SAR mode (Not using digital filter function) | When ADCLK = PCLKA/1 is set*1 | $t_{ADDP}$ | [When A/D-converted value addition/averaging function is not used]<br>● 6 ADCLK + 2 PCLKA<br>[When A/D-converted value addition/averaging function is used]<br>● 7 ADCLK + 2 PCLKA |
| | | Other than above | | [When A/D-converted value addition/averaging function is not used]<br>● 7 ADCLK + (5～6 PCLKA)<br>[When A/D-converted value addition/averaging function is used]<br>● 8 ADCLK + (5～6 PCLKA) |
| | Oversampling mode or Hybrid mode (Using with digital filter | When ADCLK = PCLKA/1 is set*1 | | [When A/D-converted value addition/averaging function is not used]<br>● 8 ADCLK + 2 PCLKA<br>[When A/D-converted value addition/averaging function is used] |

| | | | | |
|---|---|---|---|---|
| | function) | | | ● 9 ADCLK + 2 PCLKA |
| | | Other than above | | [When A/D-converted value addition/averaging function is not used]<br>● 9 ADCLK + 5～6 PCLKA<br>[When A/D-converted value addition/averaging function is used]<br>● 10 ADCLK + 5～6 PCLKA |
| Total A/D conversion time (SAR mode)*3 | Channel conversion time*2 | | $t_{ADCH\_S}$ | $(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times N_{ADC} \times ADCLK$ |
| | Scan conversion time*4 | | $t_{SCAN\_S}$ | [When channel-dedicated sample-and-hold circuit is not used]<br>● $\Sigma t_{ADCH\_S}$<br>[When channel-dedicated sample-and-hold circuit is used]<br>● $t_{SH\_SPL} + t_{SH\_HLD} + \Sigma t_{ADCH\_S}$ |
| Total A/D conversion time (Oversampling mode)*3 | Oversampling period | | $t_{OV\_OS}$ | $(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times ADCLK$ |
| | Channel conversion time | | $t_{ADCH\_O}$ | $(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times (N_{TAP} + N_{ADC}) \times ADCLK$ |
| | Scan conversion time*5 | | $t_{SCAN\_O}$ | $\Sigma t_{ADCH\_O}$ |
| Total A/D conversion time (Hybrid mode)*3 | Channel-dedicated sample-and-hold processing time in Hybrid mode | | $t_{HY\_SH}$ | $t_{SH\_SPL} + t_{SH\_HLD} + t_{SH\_D}$ |
| | Oversampling period | | $t_{HY\_OS}$ | $(t_{DDA} + t_{AD\_SPL} + t_{AD\_CNV}) \times ADCLK$ |
| | Scan conversion time | Initial delay | $t_{HY\_ID}$ | [When channel-dedicated sample-and-hold circuit is not used]<br>●$( N_{TAP} + N_{ADC} ) \times \Sigma t_{HY\_OS}$ *6<br>[When channel-dedicated sample-and-hold circuit is used]<br>●$( t_{HY\_SH} \times (N_{ADC} + N_{TAP}) - t_{SH\_D} ) + ( N_{TAP} + N_{ADC} ) \times \Sigma t_{HY\_OS}$ *6 |
| | | After initial delay time | $t_{SCAN\_HY}$ | [When channel-dedicated sample-and-hold circuit is not used]<br>●$\Sigma t_{HY\_OS}$ *6<br>[When channel-dedicated sample-and-hold circuit is used]<br>● $t_{HY\_SH} + \Sigma t_{HY\_OS}$ *6 |

Note: n = 0～8、m = 0、1、p = 0～7、q = 0～15

$N_{ADC}$：This value is the number of the times of the addition/averaging according to the setting value of ADDOPCRBx.ADC[3:0] (x = 0 to 36). If A/D-converted value addition/averaging function is not used, this value is 1.

$N_{TAP}$：This value is the number of TAP of the digital filter that selected in ADDOPCRAx.DFSEL[2:0] (x = 0 to 36) and ADDFSRm.DFSELy[1:0] (m = 0, 1, y = 0 to 4).

$N_{SGCH}$：This value is the number of the channels in the scan group.

Note 1. When ADCLKCR.CLKSEL[1:0] = 10b and ADCLKCR.DIVR[2:0] = 000b are set.
Note 2. It does not include the channel-dedicated sample-and-hold processing time.
Note 3. It does not include the A/D conversion data processing time.
Note 4. This is the sum of the channel conversion times ($t_{ADCH\_N}$) that calculated from the conversion settings for each analog channel assigned to the scan group. If channel-dedicated sample-and-hold circuits are used, channel-dedicated sample-and-hold processing times ($t_{SH\_SPL}$ and $t_{SH\_HLD}$) are also added.
Note 5. This is the sum of the channel conversion times ($t_{ADCH\_O}$) that calculated from the conversion settings for each analog channel assigned to the scan group.
Note 6. This is the sum of the oversampling period ($t_{HY\_OS}$) that calculated from the conversion settings for each analog channel assigned to the scan group.

## Before correction

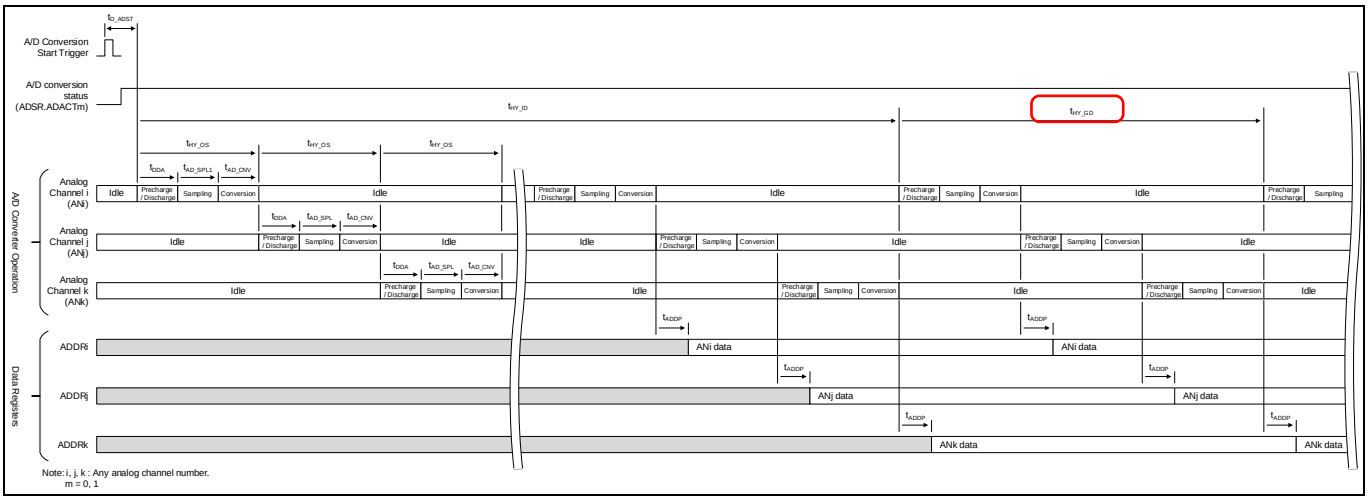


Figure 36.55 A/D conversion processing time (Hybrid mode)

## After correction

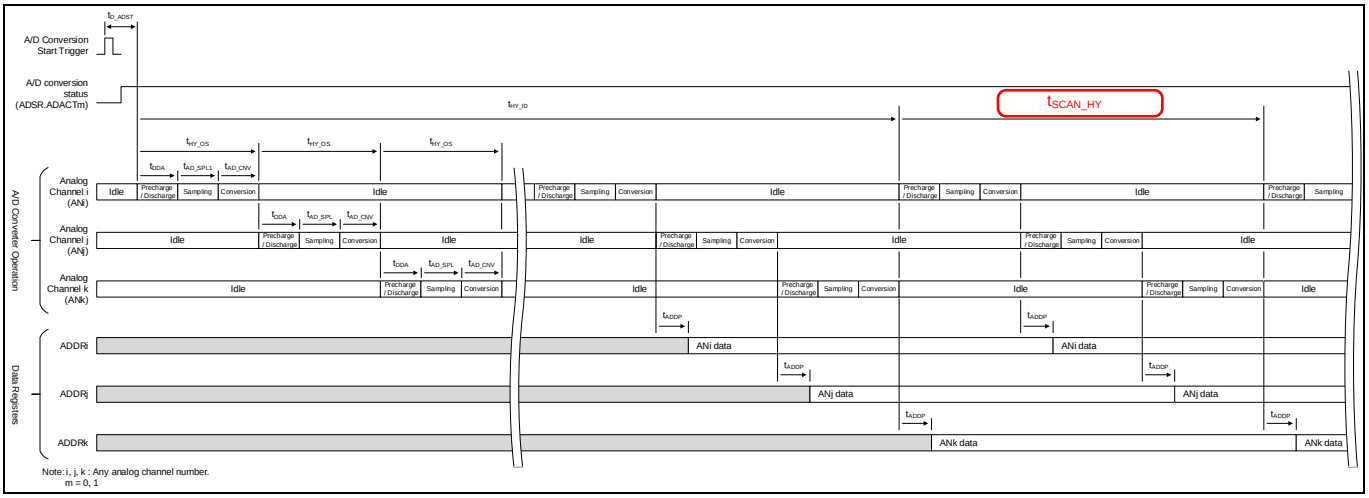


Figure 36.55 A/D conversion processing time (Hybrid mode)

## Before correction

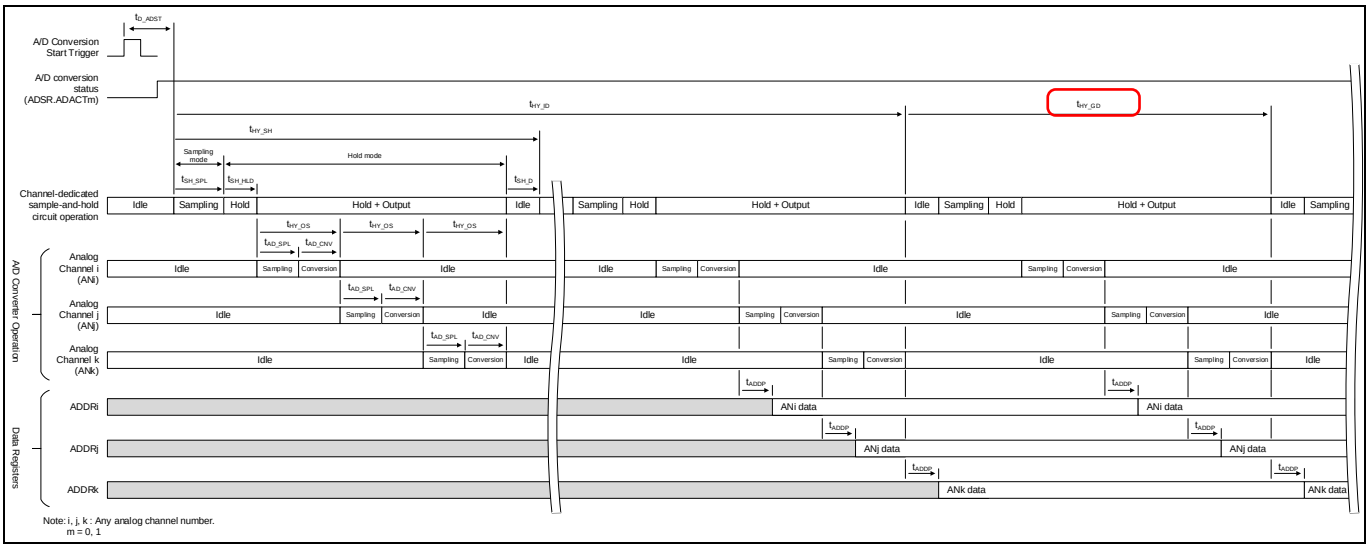


Figure 36.56 A/D conversion processing time (Hybrid mode with channel-dedicated sample-and-hold circuit)

## After correction

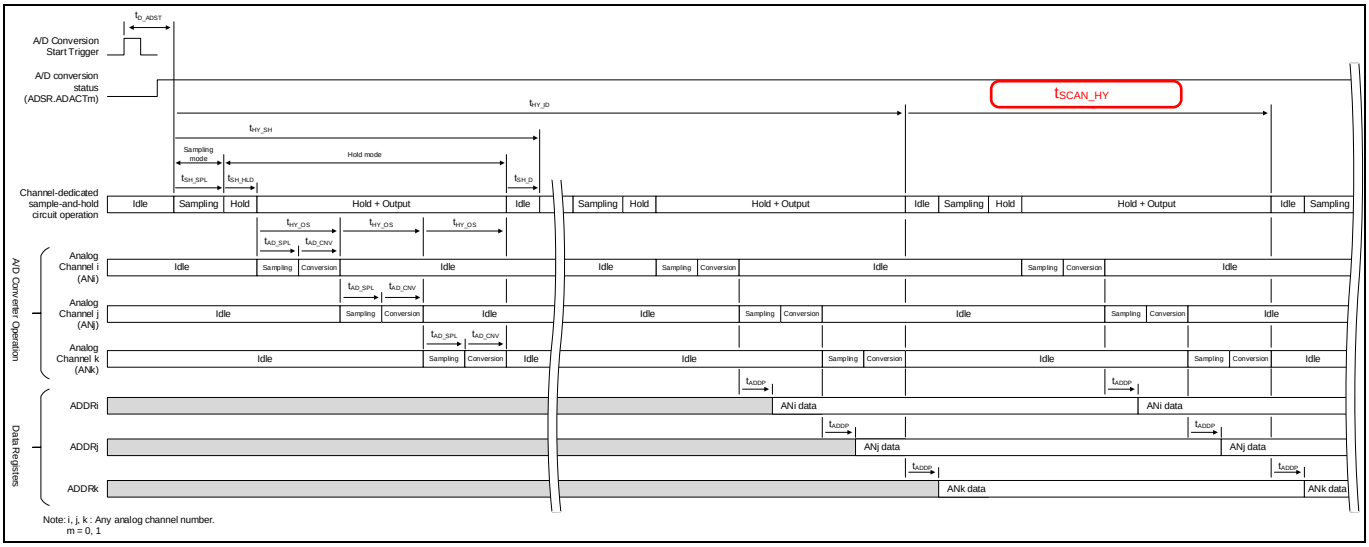


Figure 36.56 A/D conversion processing time (Hybrid mode with channel-dedicated sample-and-hold circuit)

## Before correction

36.10.1 Prohibitation of Changing the Operation Settings During A/D Conversion Operation
The registers related to the operation setting of the A/D converter should be set while all A/D converters are stopped (ADSR.ADACTm = 0 and ADSR.CALACTm = 0 (m = 0, 1)). Changing (writing) of registers except for those listed below is prohibited during A/D conversion. If the operation setting is changed during A/D conversion, operation is not guaranteed.

[Registers that can be written while the A/D converter is operating]
- Status clear registers
  – Status clear registers related to A/D converter operation
    (ADERSCR, ADCALSCR, ADCALENDSCR, ADSCANENDSCR)

## After correction

36.10.1 Prohibition of Changing the Operation Settings During A/D Conversion Operation
The registers related to the operation setting of the A/D converter should be set while all A/D converters are stopped (ADSR.ADACTm = 0 and ADSR.CALACTm = 0 (m = 0, 1)). Changing (writing) of registers except for those listed below is prohibited during A/D conversion. If the operation setting is changed during A/D conversion, operation is not guaranteed.

[Registers that can be written while the A/D converter is operating]
- Status clear registers
  – Status clear registers related to A/D converter operation
    (ADERSCR, ADCALENDSCR, ADSCANENDSCR)

## Before correction

Table 37.1 DAC12 specifications

| Parameter | Specifications |
|---|---|
| Resolution | 12 bits |
| Output channels | 4 channels |
| Module-stop function | Module-stop state can be set to reduce power consumption |
| Event link function (input) | The DA0, DA1, DA2 and DA3 conversion can be started on input of an event signal |
| D/A output amplifier control function | Controls whether the output amplifier (for both amplifier-through and amplifier-bias controls) is used |
| Destination of D/A output control function | Controls whether the output to the external pin or to the internal modules (ACMPHS) is used |
| TrustZone Filter | Security attribution can be set |

## After correction

Table 37.1 DAC12 specifications

| Parameter | Specifications |
|---|---|
| Resolution | 12 bits |
| Output channels | 4 channels |
| Module-stop function | Module-stop state can be set to reduce power consumption |
| Event link function (input) | The DA0, DA1, DA2 and DA3 conversion can be started on input of an event signal |
| D/A output amplifier control function | Controls whether the output amplifier (for both amplifier-through and amplifier-bias controls) is used |
| Destination of D/A output control function | Controls whether the output to the external pin or to the internal modules (ACMPHS and ADC) is used |
| TrustZone Filter | Security attribution can be set |

## Before correction

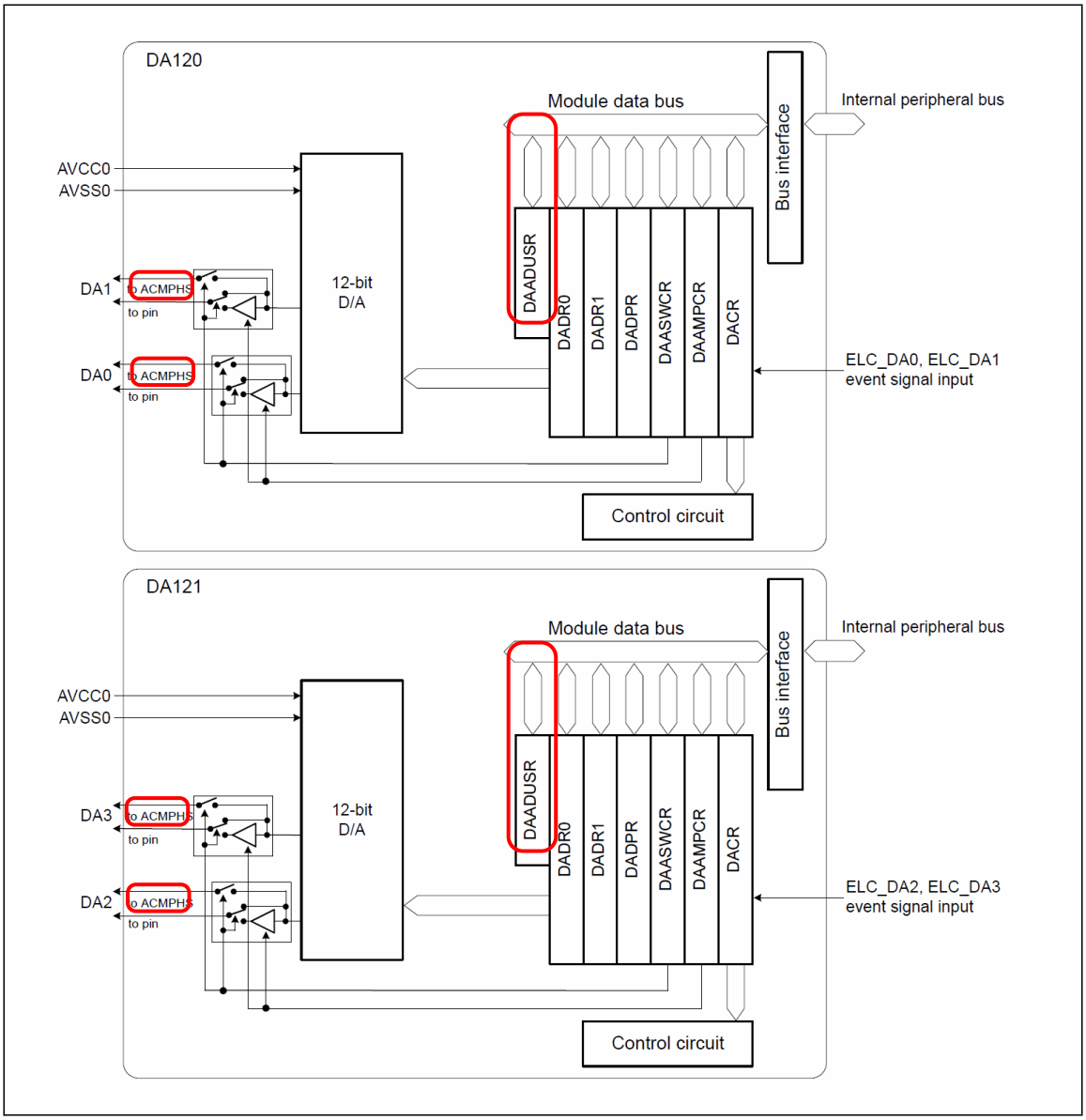


Figure 37.1 DAC12 block diagram

## After correction

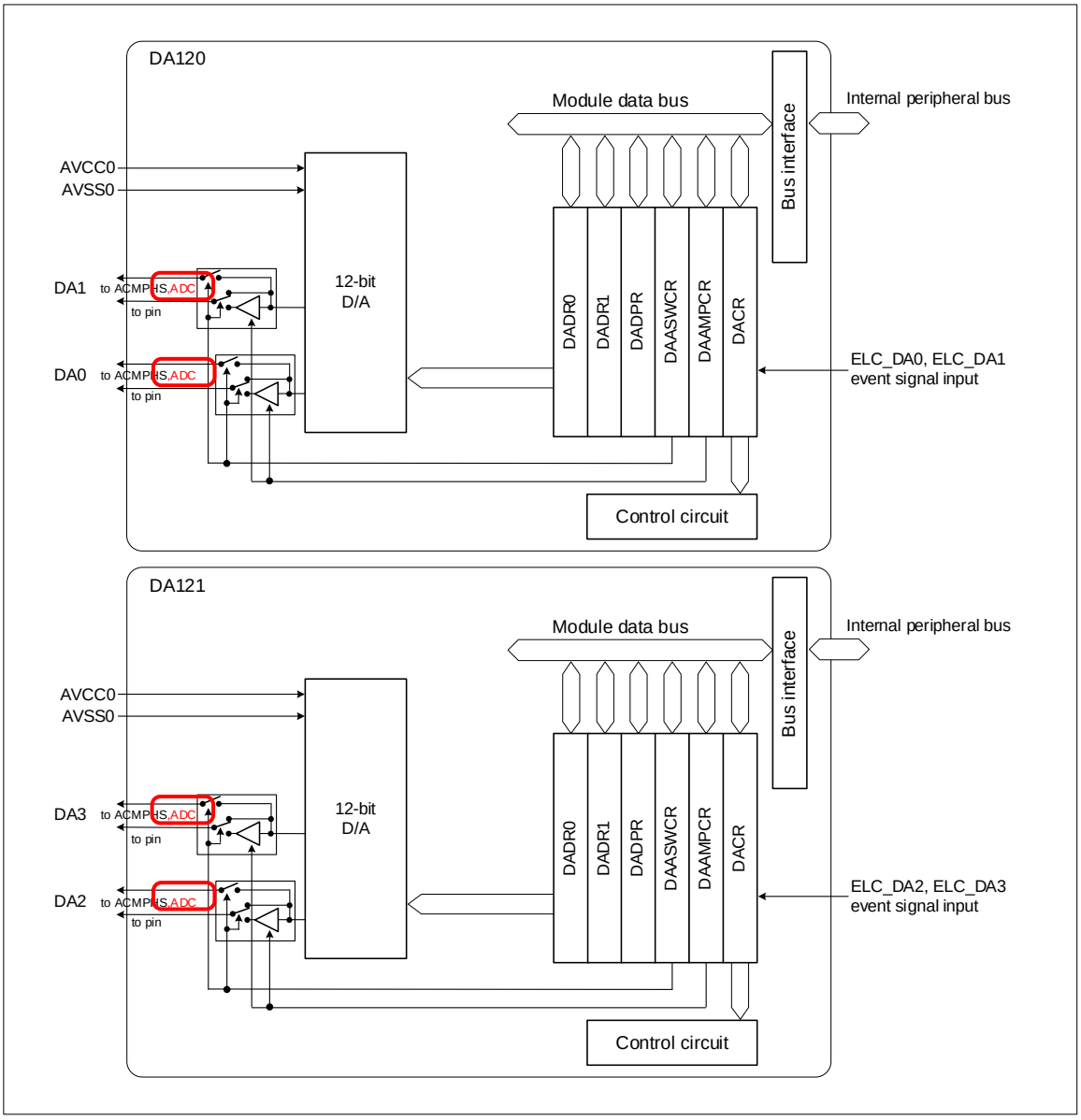


Figure 37.1 DAC12 block diagram

## Before correction

Table 37.5 D/A conversion and analog output control

| DACR | | DAAMPCR | DAASWCR | Channel i operation | Amplifier operation of channel i | Analog external output of channel i*1 | Analog internal output of channel i*2 |
|---|---|---|---|---|---|---|---|
| DAE | DAOEi | DAAMPi | DAASWi | | | | |
| 0 | 0 | x | x | Stop | Stop | Hi-Z | Hi-Z |
| 0 | 1 | 0 | 0 | Run | Stop | Amplifier-through | Hi-Z |
| 0 | 1 | 0 | 1 | Run | Stop | Hi-Z | Amplifier-through |
| 0 | 1 | 1 | 0 | Run | Run | Amplifier output | Hi-Z |
| 0 | 1 | 1 | 1 | Run | Run | Hi-Z | Hi-Z |
| 1 | x | 0 | 0 | Run | Stop | Amplifier-through | Hi-Z |
| 1 | x | 0 | 1 | Run | Stop | Hi-Z | Amplifier-through |
| 1 | x | 1 | 0 | Run | Run | Amplifier output | Hi-Z |
| 1 | x | 1 | 1 | Run | Run | Hi-Z | Hi-Z |

Note. x : Don't care
Note 1. output to pin
Note 2. output to ACMPHS

## After correction

Table 37.5 D/A conversion and analog output control

| DACR | | DAAMPCR | DAASWCR | Channel i operation | Amplifier operation of channel i | Analog external output of channel i*1 | Analog internal output of channel i*2 |
|---|---|---|---|---|---|---|---|
| DAE | DAOEi | DAAMPi | DAASWi | | | | |
| 0 | 0 | x | x | Stop | Stop | Hi-Z | Hi-Z |
| 0 | 1 | 0 | 0 | Run | Stop | Amplifier-through | Hi-Z |
| 0 | 1 | 0 | 1 | Run | Stop | Hi-Z | Amplifier-through |
| 0 | 1 | 1 | 0 | Run | Run | Amplifier output | Hi-Z |
| 0 | 1 | 1 | 1 | Run | Run | Hi-Z | Hi-Z |
| 1 | x | 0 | 0 | Run | Stop | Amplifier-through | Hi-Z |
| 1 | x | 0 | 1 | Run | Stop | Hi-Z | Amplifier-through |
| 1 | x | 1 | 0 | Run | Run | Amplifier output | Hi-Z |
| 1 | x | 1 | 1 | Run | Run | Hi-Z | Hi-Z |

Note. x : Don't care
Note 1. output to pin
Note 2. output to ACMPHS and ADC

## Before correction

Table 46.36 A/D conversion characteristics (Oversampling mode and Hybrid mode)

| Parameter | | | | Min | Typ | Max | Unit | Test condition |
|---|---|---|---|---|---|---|---|---|
| Oversampling mode and Hybrid mode | Analog input voltage range | Single-ended input voltage | | VREFL0 | - | VREFH0 | V | - |
| | | Differential input voltage*1 | | -VREFH0 | - | +VREFH0 | V | - |
| | Resolution | | | - | - | 16 | bit | - |
| | Oversampling period | Oversampling mode | | 0.16 | - | - | µs | ●ADCLK: 50 MHz<br>●Sampling time: 3 ADCLK<br>●Successive approximation time: 5 ADCLK<br>●Without disconnection detection assist function |
| | | Hybrid mode | | 0.18 | - | - | µs | ●ADCLK: 50 MHz<br>●Sampling time: 4 ADCLK<br>●Successive approximation time: 5 ADCLK<br>●Without disconnection detection assist function |
| | Digital filter characteristics *2 | Sinc filter | Initial delay | - | 22 | - | Fos | - |
| | | | Group delay | - | 11 | - | | - |
| | | | Normalized Cutoff Frequency | - | 0.033 | - | Fin/Fos | - |
| | | Minimum phase filter | Initial delay | - | 22 | - | Fos | - |
| | | | Group delay | - | 2 | - | | - |
| | | | Normalized Cutoff Frequency | - | 0.116 | - | Fin/Fos | - |
| | | | Passband ripple | - | <±0.01 | - | dB | - |

Note: Fos is oversampling frequency.

Note 1. Differential input voltage is (AINP - AINN)
- AINP is input voltage of ANx, and VREFL0 ≤ AINP ≤ VREFH0.
- AINN is input voltage of ANy, and VREFL0 ≤ AINN ≤ VREFH0.

(x = 2i, y = 2i +1, i = 0, 1, 2… (any integer))

Note 2. See Figure 46.50 and Figure 46.51.

## After correction

Table 46.36 A/D conversion characteristics (Oversampling mode and Hybrid mode)

| Parameter | | | | Min | Typ | Max | Unit | Test condition |
|---|---|---|---|---|---|---|---|---|
| Oversampling mode and Hybrid mode | Analog input voltage range | Single-ended input voltage | | VREFL0 | - | VREFH0 | V | - |
| | | Differential input voltage*1 | | -VREFH0 | - | +VREFH0 | V | - |
| | Resolution | | | - | - | 16 | bit | - |
| | Oversampling period | Oversampling mode | | 0.16 | - | - | μs | ●ADCLK: 50 MHz<br>●Sampling time: 3 ADCLK<br>●Successive approximation time: 5 ADCLK<br>●Without disconnection detection assist function<br>●Signal source impedance: 50 Ω or less |
| | | Hybrid mode*3 | | 0.18 | - | - | μs | ●ADCLK: 50 MHz<br>●Sampling time: 4 ADCLK<br>●Successive approximation time: 5 ADCLK<br>●Without disconnection detection assist function<br>●Signal source impedance: 50 Ω or less |
| | Digital filter characteristics *2 | Sinc filter | Initial delay | - | 22 | - | 1/Fos | - |
| | | | Group delay | - | 11 | - | | - |
| | | | Normalized Cutoff Frequency | - | 0.033 | - | Fin/Fos | - |
| | | Minimum phase filter | Initial delay | - | 22 | - | 1/Fos | - |
| | | | Group delay | - | 2 | - | | - |
| | | | Normalized Cutoff Frequency | - | 0.116 | - | Fin/Fos | - |
| | | | Passband ripple | - | <±0.01 | - | dB | - |

Note: Fos is oversampling frequency.
When in Hybrid mode, Fos is 1/ (the sum of the oversampling periods of each analog channel assigned to the scan group).
Note 1. Differential input voltage is (AINP - AINN)
- AINP is input voltage of ANx, and VREFL0 ≤ AINP ≤ VREFH0.
- AINN is input voltage of ANy, and VREFL0 ≤ AINN ≤ VREFH0.

(x = 2i, y = 2i +1, i = 0, 1, 2… (any integer))
Note 2. See Figure 46.50 and Figure 46.51.
Note 3. Value per channel.