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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0174A/E	Rev.	1.00
Title	Errata Corrections to the User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RA2L2 Group	Lot No. All lots	Reference Document	Renesas RA2L2 Group User's Manual: Hardware R01UH1080EJ0110 Rev.1.10		

We are correcting errors in the RA2L2 Group User's Manual, Hardware Section.

Please see the following pages for details.

Errata Corrections to the User's Manual: Hardware

10. Low Power Modes

10.1 Overview, Table 10.2 Operating conditions of each low power mode
Note 8. contains a typographical error.

Before

Note 8. When using the 12-bit A/D Converter (ADC12) in Snooze mode, the ADCMPCR.CMPAE or ADCMPCR.CMPBE bit must be 1.

After

Note 8. When using the 12-bit A/D Converter (ADC12) in Snooze mode, the ADCMPCR.CMPAE and ADCMPCR.CMPBE bit must be 1.

10.2.14 LPOPT : Lower Power Operation Control Register

Incorrect initial value and write value for bit 6 in "10.2.14 LPOPT: Lower Power Operation Control Register ".

Before

10.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W

After

10.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	—	This bit is read as 1. The write value should be 1.	R/W

26. USB Type-C Interface

Typographical error in "26.1 Overview"

Before

26.1 Overview

The USB Type-C interface complies with Universal Serial Bus Type-C Cable and Connector Specification, Release 2.3.

USB Type-C interface supports the following function through configuration channels (USB_CC1 and USB_CC2) and USB bus power status (USB_VBUS).

After

26.1 Overview

The USB Type-C interface complies with Universal Serial Bus Type-C Cable and Connector Specification, Release 2.4.

USB Type-C interface supports the following function through configuration channels (USB_CC1 and USB_CC2) and USB bus power status (USB_VBUS).

34. 12-Bit A/D Converter (ADC12)

There is a typographical error in the DBLANS[4:0] bit setting value in "Table 34.16 Relationship between DBLANS bit settings and double-trigger enabled channels".

Before

Table 34.16 Relationship between DBLANS bit settings and double-trigger enabled channels

DBLANS[4:0]	Duplication channel
0x00	AN000
0x01	AN001
0x02	AN002
0x03	AN003
0x04	AN004
0x05	AN005
0x06	AN006
0x07	AN007
0x08	AN008
0x09	AN009
0x0A	AN010
0x11	AN017
0x13	AN018
0x14	AN019
0x15	AN020
0x16	AN021
0x17	AN022

After

Table 34.16 Relationship between DBLANS bit settings and double-trigger enabled channels

DBLANS[4:0]	Duplication channel
0x00	AN000
0x01	AN001
0x02	AN002
0x03	AN003
0x04	AN004
0x05	AN005
0x06	AN006
0x07	AN007
0x08	AN008
0x09	AN009
0x0A	AN010
0x11	AN017
0x12	AN018
0x13	AN019
0x14	AN020
0x15	AN021
0x16	AN022

41. Electrical Characteristics

(1) The section 41.3.4 Wakeup Time has been corrected in Table 41.23 Timing of recovery from low power modes (2).

- Border position of symbol t_{SBYMO}.
- Oscillator frequency when VCC = 1.6V to 1.8V in "External clock input to main clock oscillator" and recovery time for Typ and Max.
- Remove *4 from "System clock source is HOCO" and add *4 to the voltage range description (VCC = 1.8V to 5.5V).

Before

Table 41.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 41.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (20 MHz)*3 VCC = 1.6 V to 1.8 V		—	11.7	13		
		System clock source is HOCO*4	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	
			VCC = 1.6 V to 1.8 V	t_{SBYMO}	—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V		—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

After

Table 41.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 41.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (4 MHz)*3 VCC = 1.6 V to 1.8 V		—	8.5	9.1		
		System clock source is HOCO	VCC = 1.8 V to 5.5 V*4	t_{SBYHO}	—	7.7	9.4	µs	
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

(2) Correct the frequency error in "System clock source is MOCO" in Table 41.24 Timing of recovery from low power modes (3) of 41.3.4 Wakeup Time.

Before

Table 41.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 41.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (2 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

After

Table 41.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 41.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

41.4.2 USBCC Characteristics

Incorrect description in Table 41.43 USB Type-C interface characteristics.

Before

Table 41.43 USB Type-C interface characteristics

Conditions: VCC = 3.0 to 3.6

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SRC voltage detection threshold	V_{SRC}	0.15	0.20	0.25	V	—
SNK VRD-1.5 voltage detection threshold	V_{VRD15}	0.613	0.66	0.70	V	—
SNK VRD-3.0 voltage detection threshold	V_{VRD30}	1.165	1.23	1.31	V	—
Rd pull-down resistor	Rd	4.6	5.1	5.6	kΩ	—
Rzopen pull-down resistor	Rzopen	126	—	—	kΩ	—

After

Table 41.43 USB Type-C interface characteristics

Conditions: VCC = 3.0 to 3.6

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SRC voltage detection threshold	V_{SRC}	0.15	0.20	0.25	V	—
SNK VRD-1.5 voltage detection threshold	V_{VRD15}	0.613	—	0.70	V	—
SNK VRD-3.0 voltage detection threshold	V_{VRD30}	1.165	—	1.31	V	—
Rd pull-down resistor	Rd	4.6	5.1	5.6	kΩ	—
Rzopen pull-down resistor	Rzopen	126	—	—	kΩ	—