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RENESAS TECHNICAL UPDATE

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Product Category	System LSI		Document No.	TN-ECL-A004A/E	Rev.	1.00
Title	EC-1 User's Manual: Hardware Correction for description regarding Receive Buffer, Receive FIFO Buffer, Transmit/Receive FIFO Buffer and Transmit Queue of RSCAN		Information Category	Technical Notification		
Applicable Product	EC-1	Lot No. All lots	Reference Document	EC-1 User's Manual: Hardware Rev.1.10 R01UH0691EJ0110 Rev.1.10		

Incorrect description regarding Receive Buffer, Receive FIFO Buffer, Transmit/Receive FIFO Buffer and Transmit Queue of RSCAN has been found.

When incorrect description of User's manual is used, there is a possibility CAN communication is not performed correctly, such as receiving data and/or sending data are incorrect and interrupt is not generated.

Please use RSCAN function with correct setting as shown below.

■ **Correction:**

No.	Page	Current description	Correct description
1	955	27.2.15 Reception Rule Pointer 0 Registers (RSCAN0GAFLP0j) (j = 0 to 15) **GAFLRMDP[6:0] Bits (Receive Buffer Number Select)** These bits are used to select the number of the receive buffer that stores received messages that have passed through the filter when the GAFLRMV bit is set to 1. Set these bits to a value smaller than the value set by the NRXMB[7:0] bits in the RSCAN0RMNB register.	27.2.15 Reception Rule Pointer 0 Registers (RSCAN0GAFLP0j) (j = 0 to 15) **GAFLRMDP[6:0] Bits (Receive Buffer Number Select)** These bits are used to select the number of the receive buffer that stores received messages that have passed through the filter when the GAFLRMV bit is set to 1. **Set the value (number) for these bits to which would satisfies the following.** **16≦GAFLRMDP[6:0]＜(16 + (the value of NRXMB[7:0] bits of RSCAN0RMNB register))**
2	964	27.2.23 Receive FIFO Buffer Configuration and Control Registers (RSCAN0RFCCx)(x = 0 to 7) **[b10 to b8] RFDC[2:0] Receive FIFO Buffer Depth Configuration** b10 b9 b8 0 0 0: 0 messages 0 0 1: 4 messages 0 1 0: 8 messages 0 1 1: 16 messages 1 0 0: 32 messages 1 0 1: 48 messages 1 1 0: 64 messages 1 1 1: 128 messages	27.2.23 Receive FIFO Buffer Configuration and Control Registers (RSCAN0RFCCx)(x = 0 to 7) **[b10 to b8] RFDC[2:0] Receive FIFO Buffer Depth Configuration** b10 b9 b8 0 0 0: 0 messages 0 0 1: 4 messages 0 1 0: 8 messages 0 1 1: 16 messages 1 0 0: 32 messages 1 0 1: 48 messages 1 1 0: 64 messages 1 1 1: **Setting prohibited**

<table>
<tr><td>3</td><td>973</td><td>27.2.30 Transmit/Receive FIFO Buffer Configuration and Control Registers k (RSCAN0CFCCk) (k = 3 to 5)

[b10 to b8] CFDC[2:0] Transmit/Receive FIFO Buffer Depth Configuration
b10 b9 b8
0 0 0: 0 messages
0 0 1: 4 messages
0 1 0: 8 messages
0 1 1: 16 messages
1 0 0: 32 messages
1 0 1: 48 messages
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<tr><td>4</td><td>997 to 1001</td><td>27.2.45 to 27.2.49
Table 27.5 to Table 27.9

<table><tr><th>Bit</th><th>Channel</th><th>Transmit Buffer Number</th></tr><tr><td>16</td><td>1</td><td>0</td></tr><tr><td>.
.</td><td>.
.</td><td>.
.</td></tr><tr><td>30</td><td>1</td><td>14</td></tr><tr><td>31</td><td>1</td><td>15</td></tr></table></td><td>27.2.45 to 27.2.49
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<table><tr><th>Bit</th><th>Channel</th><th>Transmit Buffer Number</th></tr><tr><td>16</td><td>1</td><td>16</td></tr><tr><td>.
.</td><td>.
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<tr><td>5</td><td>1007</td><td>27.2.54 Transmit Queue Configuration and Control Register (RSCAN0TXQCC1)

TXQDC[3:0] Bits (Transmit Queue Depth Configuration) Table 27.10

<table><tr><th>Settings of TXQDC[3:0] Bits</th><th>Transmit Buffers p Allocated to the Transmit Queue (p = 16 to 31)
Channel 1</th></tr><tr><td>0000b</td><td>Transmit buffer 16</td></tr><tr><td>0001b</td><td>Transmit buffer 17</td></tr><tr><td>0010b</td><td>Transmit buffer 18</td></tr><tr><td>0011b</td><td>Transmit buffer 19</td></tr><tr><td>0100b</td><td>Transmit buffer 20</td></tr><tr><td>0101b</td><td>Transmit buffer 21</td></tr><tr><td>0110b</td><td>Transmit buffer 22</td></tr><tr><td>0111b</td><td>Transmit buffer 23</td></tr><tr><td>1000b</td><td>Transmit buffer 24</td></tr><tr><td>1001b</td><td>Transmit buffer 25</td></tr><tr><td>1010b</td><td>Transmit buffer 26</td></tr><tr><td>1011b</td><td>Transmit buffer 27</td></tr><tr><td>1100b</td><td>Transmit buffer 28</td></tr><tr><td>1101b</td><td>Transmit buffer 29</td></tr><tr><td>1110b</td><td>Transmit buffer 30</td></tr><tr><td>1111b</td><td>Transmit buffer 31</td></tr></table></td><td>27.2.54 Transmit Queue Configuration and Control Register (RSCAN0TXQCC1)

TXQDC[3:0] Bits (Transmit Queue Depth Configuration) Table 27.10

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<tr><td>6</td><td>1036</td><td>27.5 Reception Function

• Reception by receive buffers:
Receive buffers from 0 to 31 can be used. Since messages stored in receive buffers are overwritten at each reception, the latest receive data can always be read.</td><td>27.5 Reception Function

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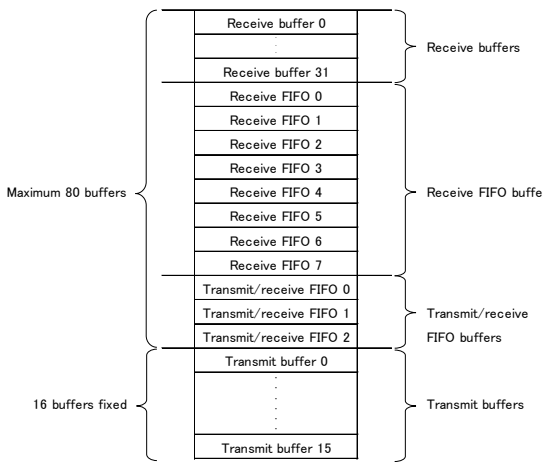
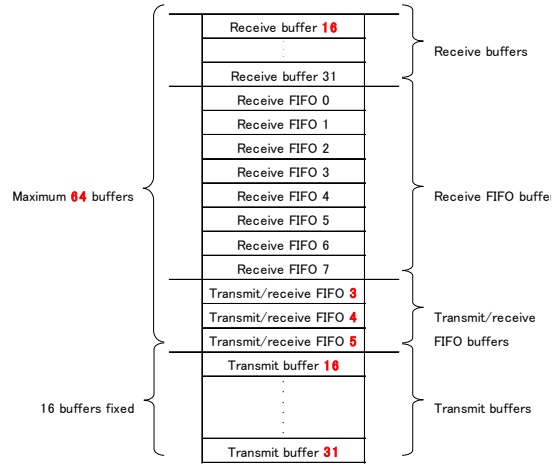
<tr><td>7</td><td>1040</td><td>27.6 Transmission Functions

• Transmission using transmit/receive FIFO buffers (transmit mode):
Channel 1 has three FIFO buffers. Up to 128 messages can be contained in a single FIFO buffer. Each FIFO buffer is used with a link to a transmit buffer. Only the message to be transmitted next in a FIFO buffer becomes the target of transmit priority determination. Messages are transmitted sequentially on a first-in, first-out basis.</td><td>27.6 Transmission Functions

• Transmission using transmit/receive FIFO buffers (transmit mode):
Channel 1 has three FIFO buffers. Up to 64 messages can be contained in a single FIFO buffer. Each FIFO buffer is used with a link to a transmit buffer. Only the message to be transmitted next in a FIFO buffer becomes the target of transmit priority determination. Messages are transmitted sequentially on a first-in, first-out basis.</td></tr>
</table>

8	1071	27.9.1.5 Buffer Setting Figure 27.19 	27.9.1.5 Buffer Setting Figure 27.19 
9	1057	27.9.1.5 Buffer Setting Figure 27.20 Description in the flow-chart - Set the number of receive buffers (0 to 32) by the NRXMB[7:0] bits.	27.9.1.5 Buffer Setting Figure 27.20 Description in the flow-chart - Set the number of receive buffers (0 to **16**) by the NRXMB[7:0] bits.
10	1064, 1065	27.9.3.1 Procedure for Transmission from Transmit Buffers Figure 27.26 and 27.27 Description in the flow-chart Transmit buffers a and b a = 0 to 31, b = 0 to 31	27.9.3.1 Procedure for Transmission from Transmit Buffers Figure 27.26 and 27.27 Description in the flow-chart Transmit buffers a and b a = **16** to 31, b = **16** to 31