RENESAS TECHNICAL UPDATE

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Product Category	System LSI	Document No.	TN-ECL-A004A/E	Rev.	1.00	
Title	EC-1 User's Manual: Hardware Correction for description regarding Receive Receive FIFO Buffer, Transmit/Receive FIFC and Transmit Queue of RSCAN	Information Category	Technical Notification			
Applicable Product		Lot No.				
	EC-1	All lots	Reference Document	User's Manual: Hardware Rev		1.10

Incorrect description regarding Receive Buffer, Receive FIFO Buffer, Transmit/Receive FIFO Buffer and Transmit Queue of RSCAN has been found.

When incorrect description of User's manual is used, there is a possibility CAN communication is not performed

correctly, such as receiving data and/or sending data are incorrect and interrupt is not generated.

Please use RSCAN function with correct setting as shown below.

■ Correction:

No.	Page	Current description	Correct description			
1	955	27.2.15 Reception Rule Pointer 0 Registers (RSCAN0GAFLP0j) (j = 0 to 15)	27.2.15 Reception Rule Pointer 0 Registers (RSCAN0GAFLP0j) (j = 0 to 15)			
			GAFLRMDP[6:0] Bits (Receive Buffer Number Select)			
		These bits are used to select the number of the receive buffer that stores received messages that have passed through the filter when the GAFLRMV bit is set to 1. Set these bits to a value smaller than	These bits are used to select the number of the receive buffer that stores received messages that have passed through the filter when the GAFLRMV bit is set to 1. Set the value (number) for these			
		the value set by the NRXMB[7:0] bits in the	bits to which would satisfies the following.			
		RSCAN0RMNB register.	16≦GAFLRMDP[6:0]<(16 + (the value of NRXMB[7:0] bits of RSCAN0RMNB register))			
2	964	27.2.23 Receive FIFO Buffer Configuration and Control Registers (RSCAN0RFCCx)(x = 0 to 7)	27.2.23 Receive FIFO Buffer Configuration and Control Registers (RSCAN0RFCCx)(x = 0 to 7)			
		[b10 to b8] RFDC[2:0] Receive FIFO Buffer Depth Configuration	[b10 to b8] RFDC[2:0] Receive FIFO Buffer Depth Configuration			
		b10 b9 b8 0 0 0: 0 messages	b10 b9 b8 0 0 0: 0 messages			
		0 0 1: 4 messages	0 0 1: 4 messages			
		0 1 0: 8 messages 0 1 1: 16 messages	0 1 0: 8 messages 0 1 1: 16 messages			
		1 0 0: 32 messages	1 0 0: 32 messages			
		1 0 1: 48 messages 1 1 0: 64 messages	1 0 1: 48 messages 1 1 0: 64 messages			
		1 1 1: 128 messages	1 1 1: Setting prohibited			



3	973	27.2.30 Transmit/Receive FIFO Buffer Configuration and Control Registers k (RSCAN0CFCCk) (k = 3 to 5)			27.2.30 Transmit/Receive FIFO Buffer Configuration and Control Registers k (RSCAN0CFCCk) (k = 3 to 5)				
		[b10 to b8] CFDC[2:0] Transmit/Receive FIFO Buffer Depth Configuration			[b10 to b8] CFDC[2:0] Transmit/Receive FIFO Buffer Depth Configuration				
			0 0 0: 0 mes 0 0 1: 4 mes		0 0 0: 0 messages 0 0 1: 4 messages				
			0 1 0: 8 mes	sages	0 1 0: 8 messages				
			0 1 1: 16 me 1 0 0: 32 me	0		0 1 1: 16 messages			
			1 0 0. 32 me		1 0 0: 32 messages 1 0 1: 48 messages				
			1 1 0: 64 me	0	1 1 0: 64 messages				
4	997	27.2.45 to 27	<u>111:128 m</u> 7249	essages	1 1 1: Setting prohibited 27.2.45 to 27.2.49				
	to 1001	Table 27.5 to Table 27.9			Table 27.5 to Table 27.9				
		Bit Channel		Transmit Buffer Number	Bit Channel Transmit Bu		Transmit Buffer Number		
		16	1	0	16	1	16		
		•	•	•	•	•	•		
		•	•	•	•	•	•		
		30 31	1	14 15	30 31	1	30		
		31	1	15	31	1	31		
5	1007	007 27.2.54 Transmit Queue Configuration and Control Register (RSCAN0TXQCC1) TXQDC[3:0] Bits (Transmit Queue Depth Configuration) Table 27.10			27.2.54 Transmit Queue Configuration and Control Register (RSCAN0TXQCC1)				
					TXQDC[3:0] Bits (Transmit Queue Depth Configuration) Table 27.10				
		Settings TXQDC[3:0]	T	hit Buffers p Allocated to the hit Queue (p = 16 to 31) Channel 1	Settings TXQDC[3:0]	T	smit Buffers p Allocated to the smit Queue (p = 16 to 31) Channel 1		
		Bits			Bits				
		0000b 0001b		Transmit buffer 16 Transmit buffer 17	0000b 0001b		Setting prohibited Setting Prohibited		
		0001b		Transmit buffer 18	0010b		Transmit buffer 31 to 29		
		0011b		Transmit buffer 19			Transmit buffer 31 to 28		
		0100b		Transmit buffer 20	0100b		Transmit buffer 31 to 27		
		0101b		Transmit buffer 21			Fransmit buffer 31 to 26		
		0110b		Transmit buffer 22	0110b		Transmit buffer 31 to 25		
		0111b		Transmit buffer 23	0111b		Transmit buffer 31 to 24		
		1000b 1001b		Transmit buffer 24 Transmit buffer 25	1000b 1001b		Transmit buffer 31 to 23		
		1001b		Transmit buffer 25	1001b		Transmit buffer 31 to 22 Transmit buffer 31 to 21		
		1010b		Transmit buffer 27	1010b		Transmit buffer 31 to 20		
		1100b		Transmit buffer 28	1100b		Transmit buffer 31 to 19		
		1101b		Transmit buffer 29	1101b		Transmit buffer 31 to 18		
		1110b		Transmit buffer 30	1110b		Transmit buffer 31 to 17		
		1111b		Transmit buffer 31	1111b		Transmit buffer 31 to 16		
6	1036	27.5 Reception Function		27.5 Rece	eption Fund	ction			
		• Deconting !	hu roccius to	ifforo	Reception by receive buffers:				
		Reception b		Inters: 0 to 31 can be used. Since					
					Receive buffers from 16 to 31 can be used. Since messages stored in receive buffers are				
		messages stored in receive buffers are overwritten at each reception, the latest receive			overwritten at each reception, the latest receive				
		data can always be read.			data can always be read.				
7	1040	27.6 Transi			 27.6 Transmission Functions Transmission using transmit/receive FIFO buffers (transmit mode): 				
		Transmissi	on using tran	smit/racaiva EIEO buffara					
				smit/receive FIFO buffers					
			(transmit mode): Channel 1 has three FIFO buffers. Up to 128			Channel 1 has three FIFO buffers. Up to 64			
		messages can be contained in a single FIFO buffer. Each FIFO buffer is used with a link to a					ontained in a single FIFO		
					buffer. Each FIFO buffer is used with a link to a				
		transmit b	transmit buffer. Only the message to be transmitted next in a FIFO buffer becomes the			transmit buffer. Only the message to be transmitted next in a FIFO buffer becomes the			
		target of transmit priority determination.			target of transmit priority determination.				
		Messages are transmitted sequentially on a first-in, first-out basis.			Messages are transmitted sequentially on a first in first out basis				
		first-in, firs		first-in, first-out basis.					



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8	1071	27.9.1.5 Buffer Setting	27.9.1.5 Buffer Setting			
		Figure 27.19	Figure 27.19			
		Receive buffer 0	Receive buffer 16			
		Receive buffers	Receive buffers			
		Receive buffer 31	Receive buffer 31			
		Receive FIFO 0 Receive FIFO 1	Receive FIFO 0 Receive FIFO 1			
		Receive FIFO 1	Receive FIFO 1			
		Receive FIFO 3	Receive FIFO 3			
		Maximum 80 buffers \prec Receive FIFO 4 \succ Receive FIFO buffe	Maximum 64 buffers Receive FIFO 4			
		Receive FIFO 5	Receive FIFO 5			
		Receive FIFO 6	Receive FIFO 6			
		Receive FIFO 7	Receive FIFO 7			
		Transmit/receive FIFO 0	Transmit/receive FIFO 3			
		Transmit/receive FIFO 1	Transmit/receive FIFO 4 Transmit/receive			
		Transmit/receive FIFO 2 FIFO buffers	Transmit/receive FIFO 5 FIFO buffers			
		Transmit buffer 0	Transmit buffer 16			
		16 buffers fixed	16 buffers fixed Transmit buffers			
		Transmit buffer 15	Transmit buffer 31			
9	1057	27.9.1.5 Buffer Setting	27.9.1.5 Buffer Setting			
_		Figure 27.20 Description in the flow-chart	Figure 27.20 Description in the flow-chart			
		· ·g···· = · ·= · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·			
		- Set the number of receive buffers (0 to 32) by the	- Set the number of receive buffers (0 to 16) by the			
		NRXMB[7:0] bits.				
10	1064.	27.9.3.1 Procedure for Transmission from Transmit Buffers	NRXMB[7:0] bits. 27.9.3.1 Procedure for Transmission from Transmit Buffers			
10	,					
	1065	Figure 27.26 and 27.27 Description in the flow-chart	Figure 27.26 and 27.27 Description in the flow-chart			
		Townson it has fformer a smalle	- ··· "			
		Transmit buffers a and b	Transmit buffers a and b			
		a = 0 to 31, $b = 0$ to 31	a = 16 to 31, $b = 16$ to 31			

