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RENESAS TECHNICAL UPDATE

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Product Category	System LSI		Document No.	TN-ECL-A003A/E	Rev.	1.00
Title	EC-1 User's Manual: Hardware Correction and adding notifications about EtherCAT Slave Controller		Information Category	Technical Notification		
Applicable Product	EC-1	Lot No. All lots	Reference Document	EC-1 User's Manual: Hardware Rev.1.10 R01UH0691EJ0110 Rev.1.10		

Correction and adding notification about EtherCAT Slave Controller.

Correction of manual are below.

■ **Correction of EtherCAT Slave Controller:**

No.	Page	Current description	Correct description
1	525	22.3.7.1 AL Control Register (AL_CONTROL) Description of b5 Value after reset: x Symbol:— Bit Name: Reserved Description : When read, the value returned is undefined. PDI:R(Clear) ECAT:R/(W)	22.3.7.1 AL Control Register (AL_CONTROL) Description of b5 Value after reset: **0** Symbol:**DEVICEID** Bit Name: **Device ID Request** Description:**Device ID Request** **0: No request** **1: Device ID request** PDI:R(Clear) ECAT:R/(W)
2	525	22.3.7.2 AL Status Register (AL_STATUS) Description of b5 Value after reset: x Symbol:— Bit Name: Reserved Description : When read, the value returned is undefined.	22.3.7.2 AL Status Register (AL_STATUS) Description of b5 Value after reset: **0** Symbol:**DEVICEID** Bit Name: **Device ID Status** Description:**Device ID Status** **0: Device ID not valid** **1: Device ID loaded**
3	530	22.3.8.3 PDI Configuration Register (PDI_CONFIG) Description of b7 to b5 Value after reset: 010 Symbol:ONCHIPBUS Bit Name: On-Chip Bus Type Indication Description:Indicate the type of on-chip bus. In this chip, the value is always 100.	22.3.8.3 PDI Configuration Register (PDI_CONFIG) Description of b7 to b5 Value after reset: 010 Symbol:ONCHIPBUS Bit Name: On-Chip Bus Type Indication Description:Indicate the type of on-chip bus. In this chip, the value is always **010**.
4	549	22.3.13.7 PHY Port Status n Register (PHY_STATUSn)	~~**22.3.13.7 PHY Port Status n Register (PHY_STATUSn)**~~

5	588	[Current description] No description. [Correct description] Add the description in below. **22.4.4 Configuration of Reset Circuit** **The configuration of Reset Circuit of ESC is shown in Figure 22.3. When Reset Request (0040h) by ECAT or Reset Request (0041h) by PDI have been received, ESC will stop and RESET pin output from ESC becomes "1". The RESET pin output from ESC will cause the PHYRESETOUT# pin to be low, then it will reset the Ethernet PHY that connected outside. And ETHCRSTI interrupt is generated.** **After ETHCRSTI interrupt is detected, it is necessary to switch the CATRST bit in the ETHSFTRST register from "1" to "0" to "1". To be noted, at the time the ESC reset input goes from "1" to "0", the ESC reset output will be "0". At the time when the ESC reset input goes from "0" to "1", the ESC starts restarting and the loading of the EEPROM will be started. The loading of EEPROM will be completed in about 1 ms. Be sure to set the timing of cancelling the reset of the Ethernet PHY, so that the restart of the Ethernet PHY will be after the start of ESC is completed. The timing chart is shown in Figure 22.4.** **It is also possible to reset the ESC with the CATRST bit in the ETHSFTRST register, not by the ECAT/PDI reset request (0040h/0041h). In this case, since the PHYRESETOUT# pin does not automatically go low, set the Ethernet PHY to the reset state beforehand by the PHYRST bit in the ETHSFTRST register. The timing chart is shown in Figure 22.5.**

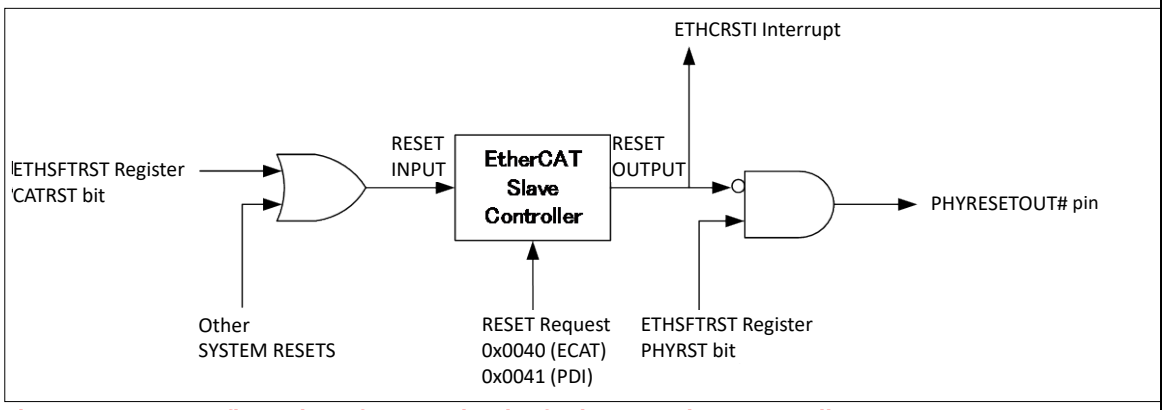

Figure 22.3 Configuration of Reset Circuit of EtherCAT Slave Controller

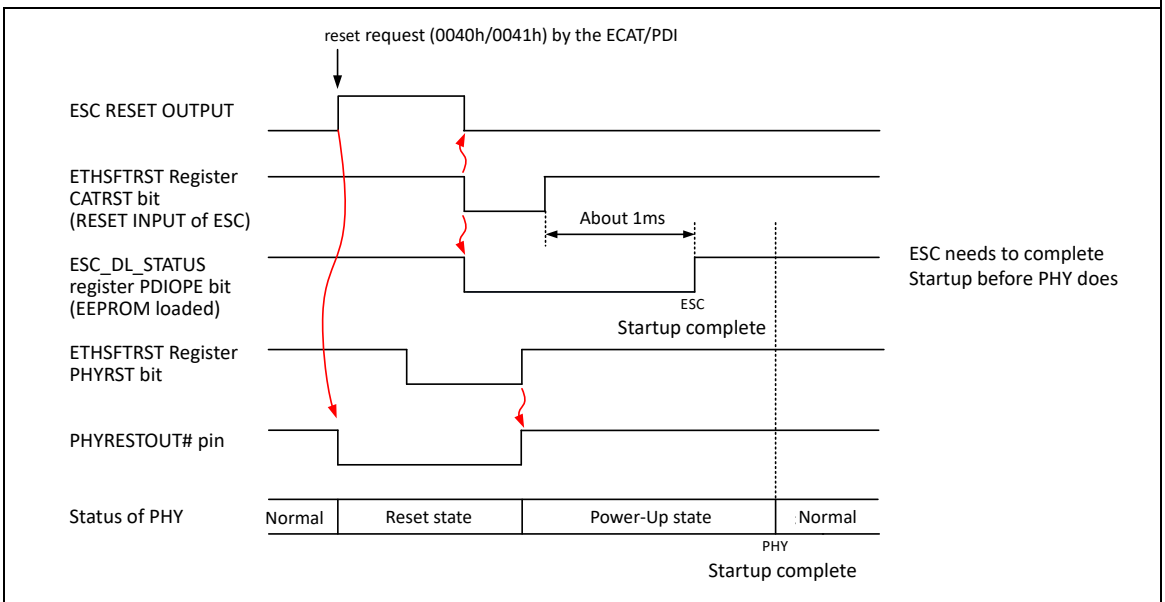

Figure 22.4 Reset timing of EtherCAT Slave Controller (when reset request by the ECAT/PDI)

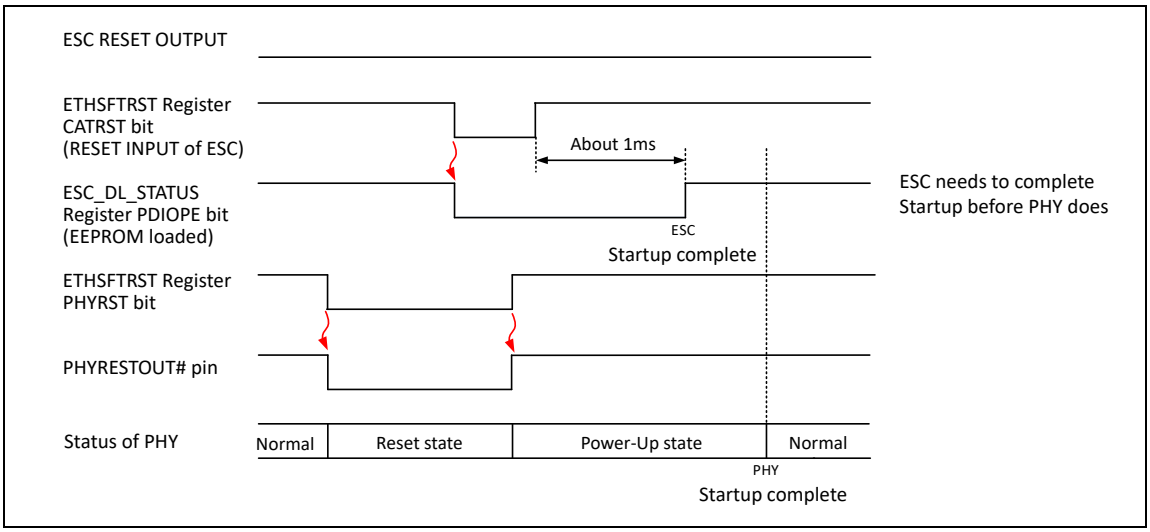

Figure 22.5 Reset timing of EtherCAT Slave Controller (when reset by the CATRST bit of ETHSFTRST)