RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A196A/E	Rev.	1.00
Title	Disclosure of the Electrical Characteristics for SD Host Interface (SDHI) and SD Slave Interface (SDSI) in RX65N Group and RX651 Group		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No. All	Reference Document	RX65N Group, RX651 Group User's Manual: Hardware Rev.2.10 (R01UH0590EJ0210)		

This document discloses the AC characteristics for the SD host interface (SDHI) and the SD slave interface (SDSI) in the RX65N and RX651 groups. The disclosed details are as follows.

Table 1. SDHI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the drive capacity control register. *1

Item		Symbol	Min.	Max.	Unit	Test Conditions*2
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	20	—	ns	Figure 1
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	3	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	3	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–6.5	4	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	6	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	2	—	ns	

Note 1. In the G-version products, the AC characteristics are measured by setting the drive capacity control register associated with the SDHI_CLK-C pin as a high-speed interface high-drive output.
Note 2. We recommend that pins suffixed with the same letter such as -A and -B, indicating grouping of the pins, should be used as a set. The AC characteristics of the SDHI are measured using the pins from the same group.

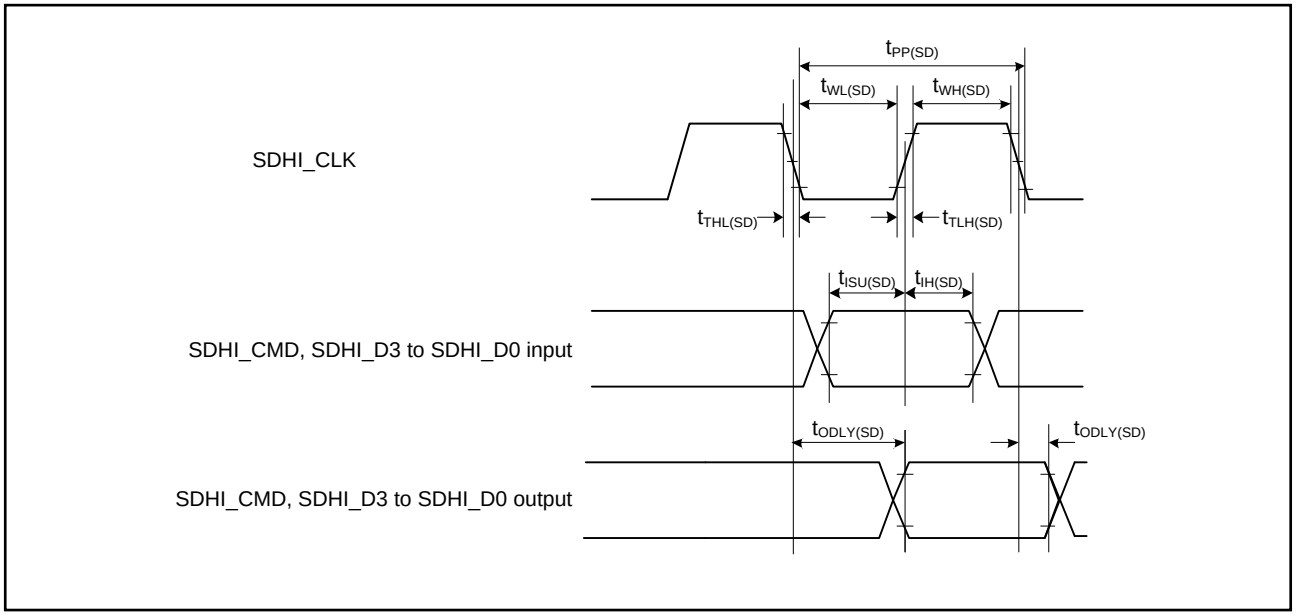

Figure 1. SD Host Interface Input/Output Signal Timing

Table 2. SDSI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions*1
SDSI	SDSI_CLK pin input cycle time	$t_{PP(SDSI)}$	20	—	ns	Figure 2
	SDSI_CLK pin input high pulse width	$t_{WH(SDSI)}$	0.4 × $t_{PP(SDSI)}$	—	ns	
	SDSI_CLK pin input low pulse width	$t_{WL(SDSI)}$	0.4 × $t_{PP(SDSI)}$	—	ns	
	SDSI_CLK pin input rise time	$t_{TLH(SDSI)}$	—	3	ns	
	SDSI_CLK pin input fall time	$t_{THL(SDSI)}$	—	3	ns	
	Input data setup time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins	$t_{ISU(SDSI)}$	5	—	ns	
	Input data hold time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins	$t_{IH(SDSI)}$	2	—	ns	
	Output data delay time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins (default speed mode)	$t_{ODLY(SDSI)}$	0	14	ns	Figure 3
	Output data delay time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins (high speed mode)		2.5	14	ns	Figure 4

Note 1. We recommend that pins suffixed with the same letter such as -A and -B, indicating grouping of the pins, should be used as a set. The AC characteristics of the SDSI are measured using the pins from the same group.

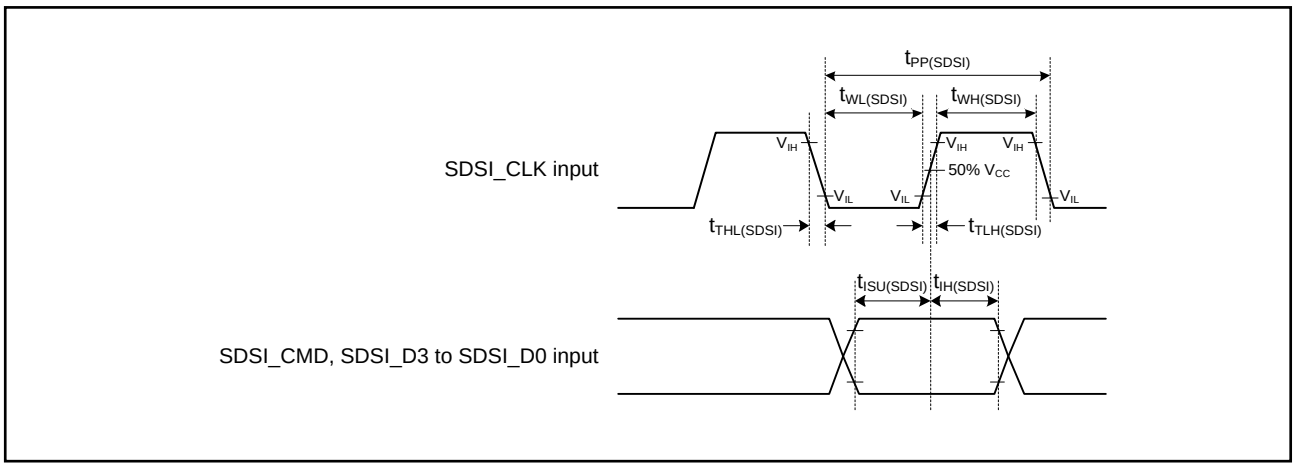

Figure 2. SD Slave Interface Input Signal Timing

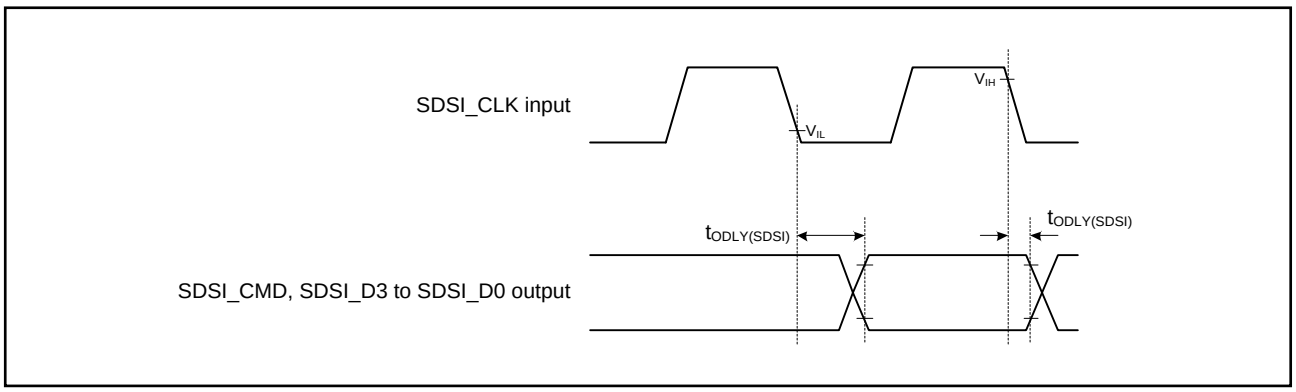

Figure 3. SD Slave Interface Output Signal Timing (Default Speed Mode)

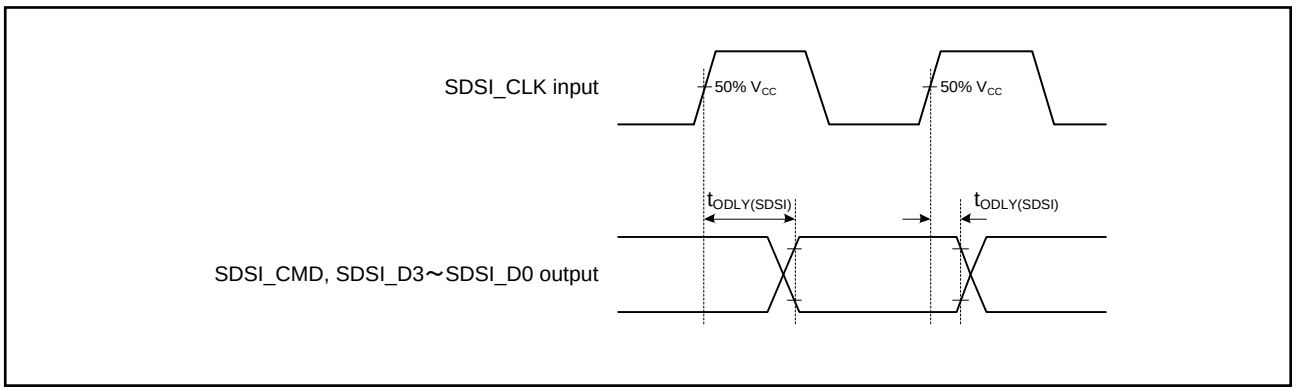

Figure 4. SD Slave Interface Output Signal Timing (High Speed Mode)