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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A227A/E	Rev.	1.00
Title	Descriptions Changed in the M16C/63 Group Manual		Information Category	Technical Notification		
Applicable Product	M16C/63 Group	Lot No. —	Reference Document	M16C/63 Group User's Manual: Hardware Rev.2.20		

Some specifications of the M16C/63 Group have been changed. MCU usage and setting procedures have also been added or changed.

- ➔: Indicates the titles in the M16C/63 Group User's Manual: Hardware Rev.2.20.
- Red frame or line: The changes are indicated with red frames or a red line.

1. Processor Mode

➔ PM13 (Internal area expansion bit 0) (b3) in 10.2.2 Processor Mode Register 1 (PM1)
When in memory expansion mode or microprocessor mode, addresses 40000h to 7FFFFh can be used as an external area regardless of the value of PM13 bit.

Table 10.5 Functions of PM13 Bit

Access Area			Bit Setting	
			PM13 = 0	PM13 = 1
Internal	RAM		Addresses 00400h up to 03FFFh (15 KB) are available (addresses 04000h to 0CFFFh cannot be used).	The entire area is usable.
	Program ROM 1		Addresses D0000h up to FFFFFh (192 KB) are available (addresses 40000h to CFFFFh cannot be used).	Addresses 80000h up to FFFFFh are available (addresses 40000h to 7FFFFh cannot be used).
External	Memory expansion mode	04000h to 0CFFFh	Usable	Reserved
		40000h to 7FFFFh	Usable	Usable
		80000 to CFFFFh	Usable	Reserved
	Micro-processor mode	04000h to 0CFFFh	Usable	Reserved
		40000h to 7FFFFh	Usable	Usable
		80000 to CFFFFh	Usable	Usable

PM13: Bit in the PM1 register

2. Bus

➔ 11.3.5.7 BCLK Output

When in memory expansion mode, the value output from the P3_0 pin is not A8, but an undefined value.

Table 11.8 Pin Functions for Each Processor Mode

Processor Mode	Memory Expansion Mode or Microprocessor Mode				Memory Expansion Mode
Bits PM05 to PM04	00b (separate bus)		01b ($\overline{CS2}$ is for multiplexed bus and the others are for separate bus) 10b ($\overline{CS1}$ is for multiplexed bus and the others are for separate bus)		11b (the entire $\overline{CS}$ space is for multiplexed bus)
Data bus width BYTE Pin	8 bits High	16 bits Low	8 bits High	16 bits Low	8 bits High
(omission)					
P3_0	A8	A8	A8	A8/D7	Undefined value is output
(omission)					

3. Remote Control Signal Receiver

➔ 22.3.3 Pattern Match Mode (Combined Operation of PMC0 and PMC1) and 22.5.4 Combined Operation

When using combined operation, set same value to bits TYP1 to TYP0 in the PMC0CON1 register and bits TYP1 to TYP0 in the PMC1CON1 register.

Table 22.13 Registers and Setting Values in Pattern Match Mode (Combined Operation) (1/2)

Register	Bit	Function	
		PMC0	PMC1
(omission)			
PMCiCON1	TYP0 TYP1	Select measuring object.	Select measuring object. Set the same value as PMC0.
(omission)			

4. Electrical Characteristics

➔ 31.1.2 Recommended Operating Conditions

The recommended operating condition of $f_{(XIN)}$ is a maximum of 10 MHz when 1.8 V ≤ V_{CC1} < 2.7 V. However $f_{(BCLK)}$ exceeded 10 MHz in the range of 1.8 V ≤ V_{CC1} < 2.7 V in the figure showing the relation between $f_{(BCLK)}$ and V_{CC1}. This section describes changes showing premodifications and post modifications.

Table 31.4 Recommended Operating Conditions (3/4)

Premodification:

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock input oscillation frequency	2.7 V ≤ V_{CC1} ≤ 5.5 V	1		20	MHz
		1.8 V ≤ V_{CC1} < 2.7 V	1		10	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768		kHz
$f_{(BCLK)}$	CPU operation clock	2.7 V ≤ V_{CC1} ≤ 5.5 V			20	MHz
		1.8 V ≤ V_{CC1} < 2.7 V			(Note 2)	MHz

Notes:
2. Calculated by the following equation according to V_{CC1}: 16.67 x V_{CC1} - 25 [MHz]
See Figure 31.1 "Relation between $f_{(BCLK)}$ and V_{CC1}"

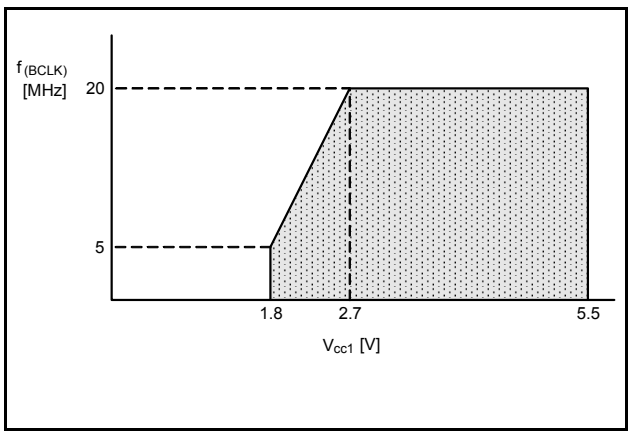
Post modification:

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock input oscillation frequency	2.7 V ≤ V_{CC1} ≤ 5.5 V	1		20	MHz
		1.8 V ≤ V_{CC1} < 2.7 V	1		10	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768		kHz
$f_{(BCLK)}$	CPU operation clock	2.7 V ≤ V_{CC1} ≤ 5.5 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 20 MHz			20	MHz
		2.1 V ≤ V_{CC1} < 2.7 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 10 MHz			10	MHz
		1.8 V ≤ V_{CC1} < 2.1 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 10 MHz			(Note 2)	MHz

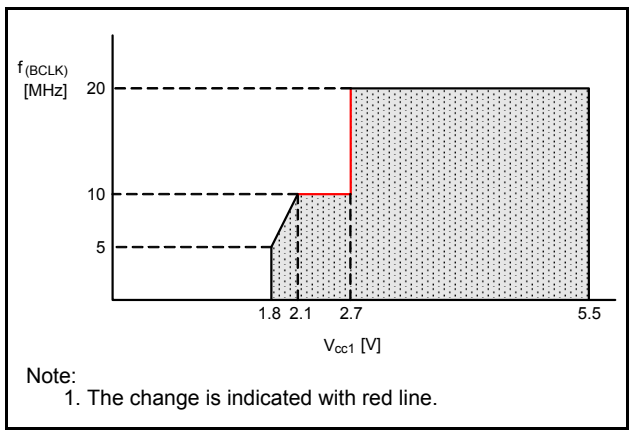
Notes:
2. Calculated by the following equation according to V_{CC1}: 16.67 x V_{CC1} - 25 [MHz]
See Figure 31.1 "Relation between $f_{(BCLK)}$ and V_{CC1}"

Figure 31.1 Relation between $f_{(BCLK)}$ and V_{CC1}

Premodification:



Post modification:



Note:
1. The change is indicated with red line.