To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-32R-A075A/E	Rev.	1.00
Title	Description about the duty-cycle when using Timer TOU in PWM output mode		Information Category	Technical Notification		
Applicable Product	32180 Group, 32192/32195/32196 Group, 32185/32186 Group	Lot No. -	Reference Document	Hardware Manual		

The following describe 100% and 0% duty-cycle output when using Timer TOU in PWM output mode.

(This information supplements the Hardware Manual)

[Contents]

By making the analogy of 80%, 0% and 100% duty-cycle, the following describe the definition and the operation of the duty-cycle when using Timer TOU in PWM output mode.

(1) 80% duty-cycle

80% duty-cycle PWM output means that when assuming a PWM period of 100%, the setting value of Reload 0 Register is 80% and that of Reload 1 Register is 20%.

(2) 0% duty-cycle

0% duty-cycle PWM output means that when assuming a PWM period of 100%, the setting value of Reload 0 Register is 0% and that of Reload 1 Register is 100%.

PWM output is 0% duty-cycle output when setting Reload 0 Register to H'FFFF.

At the time of reloading Reload 0 Register when the reload value is H'FFFF, F/F output is not inverted.

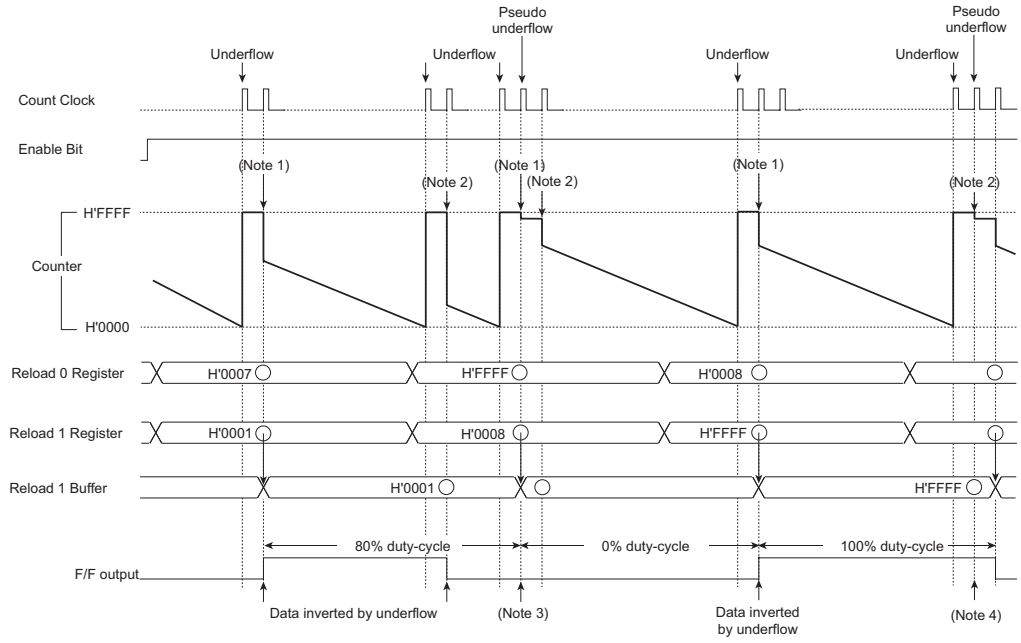
(3) 100% duty-cycle

100% duty-cycle PWM output means that when assuming a PWM period of 100%, the setting value of Reload 0 Register is 100% and that of Reload 1 Register is 0%.

PWM output is 100% duty-cycle output when setting Reload 0 Register to H'FFFF.

At the time of reloading Reload 1 Buffer when the reload value is H'FFFF, F/F output is not inverted.

Figure 1 shows a typical switching operation of 80%, 0% and 100% duty-cycle output when assuming F/F output initial value of "L."



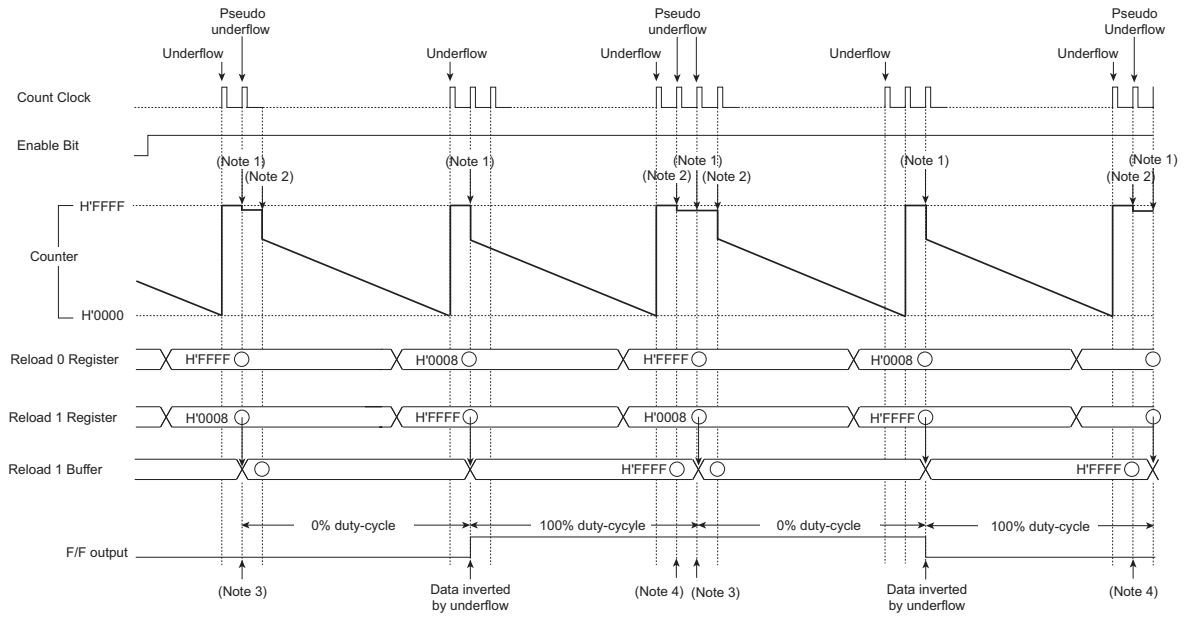
Note 1: The value of "Reload 0 Register -1" is reloaded by underflow.
Note 2: The value of "Reload 1 Buffer -1" is reloaded by underflow.
Note 3: Because reload value is H'FFFF, pseudo underflow occurs simultaneously with reloading and F/F output operates without inversion (F/F output inversion via reloading Reload 0 Register, and Reload 0 Register inversion via underflow operation overlaps).
Note 4: Because reload value is H'FFFF, pseudo underflow occurs simultaneously with reloading and F/F output operates without inversion (F/F output inversion via reloading Reload 1 Buffer, and Reload 1 Buffer inversion via underflow operation overlaps).

Figure 1 Typical switching operation of 80%, 0% and 100% duty-cycle output

[Precautions]

0% duty-cycle maintains the final PWM period output level, immediately preceding the switching to 0% output. Therefore, when switching the duty-cycle from 100% to 0%, the output level of the output pin (F/F) is output without inverted waveform.

Figure 2 shows a typical switching operation of 0%, 100%, 0% and 100% duty-cycle output.

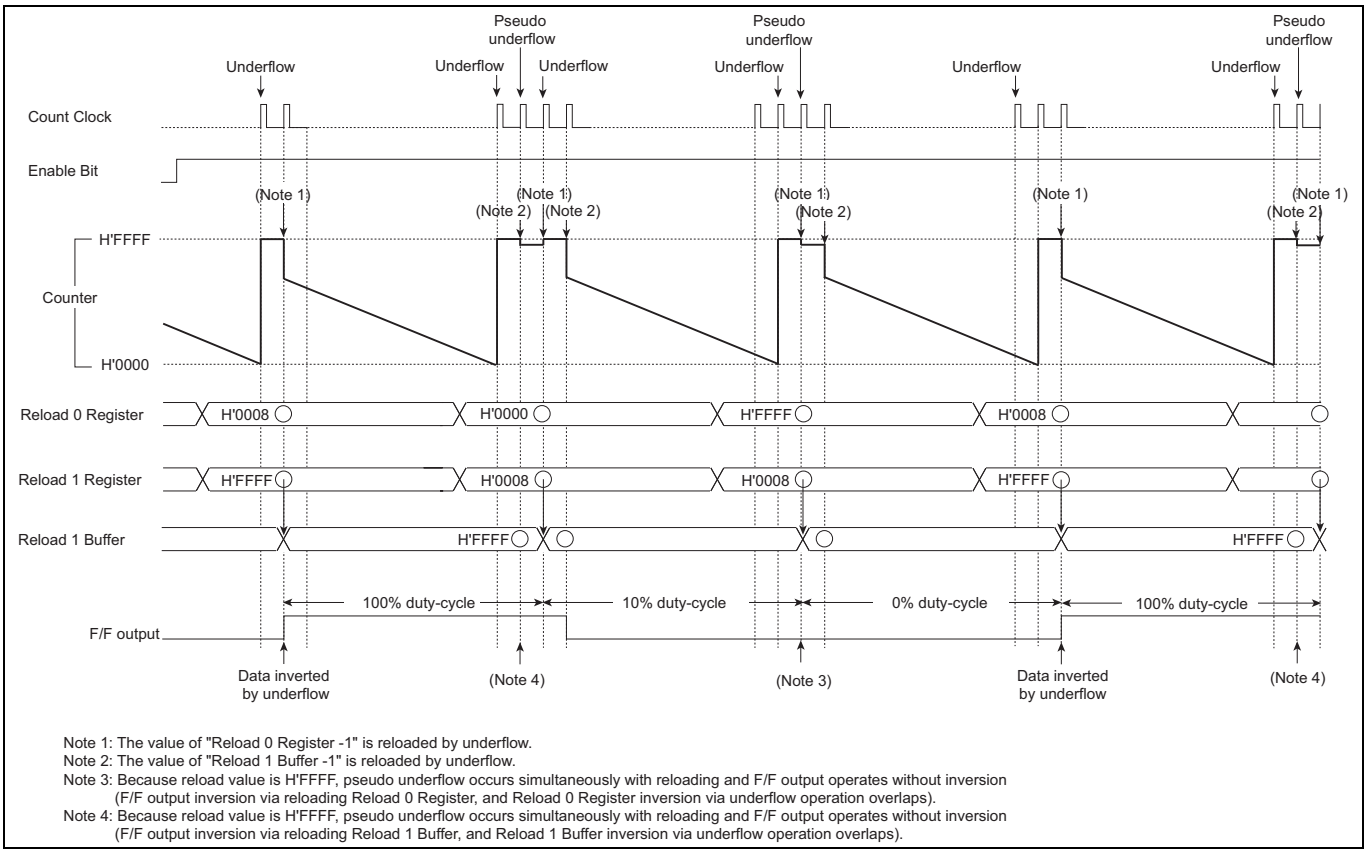


Note 1: The value of "Reload 0 Register -1" is reloaded by underflow.
Note 2: The value of "Reload 1 Register -1" is reloaded by underflow.
Note 3: Because reload value is H'FFFF, pseudo underflow occurs simultaneously with reloading and F/F output operates without inversion (F/F output inversion via reloading Reload 0 Register, and Reload 0 Register inversion via underflow operation overlaps).
Note 4: Because reload value is H'FFFF, pseudo underflow occurs simultaneously with reloading and F/F output operates without inversion (F/F output inversion via reloading Reload 1 Buffer, and Reload 1 Buffer inversion via underflow operation overlaps).

Figure 2 Typical switching operation of 0%, 100%, 0% and 100% duty-cycle output

In addition, if you want to invert the output level of the output pin (F/F) and maintain the output level while PWM output mode is operating, insert a PWM duty-cycle of between 0% and 100%, with the exception of 0% and 100%.

Figure 3 shows a typical switching operation of 100%, 10%, 0% and 100% duty-cycle output.



Note 1: The value of "Reload 0 Register -1" is reloaded by underflow.
Note 2: The value of "Reload 1 Buffer -1" is reloaded by underflow.
Note 3: Because reload value is H'FFFF, pseudo underflow occurs simultaneously with reloading and F/F output operates without inversion (F/F output inversion via reloading Reload 0 Register, and Reload 0 Register inversion via underflow operation overlaps).
Note 4: Because reload value is H'FFFF, pseudo underflow occurs simultaneously with reloading and F/F output operates without inversion (F/F output inversion via reloading Reload 1 Buffer, and Reload 1 Buffer inversion via underflow operation overlaps).

Figure 3 Typical switching operation of 100%, 10%, 0% and 100% duty-cycle output