

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-RZ*-A0143A/E	Rev.	1.00
Title	DDR Memory Controller issue	Information Category	Technical Notification		
Applicable Product	RZ/T2H and RZ/N2H Groups	Lot No.	Reference Document	RZ/T2H and RZ/N2H Groups User's Manual: Hardware Rev.1.10 (R01UH1039EJ0110)	
		All			

This document describes an issue with the DDR Memory Controller.

1. Target product

Product	Part Number	Package	Cortex-A55	Cortex-R52	Security
RZ/T2H	R9A09G077M48GBG#AC0 R9A09G077M48GBG#BC0	729-pin FCBGA	Quad cores	Two CPUs	Available
	R9A09G077M28GBG#AC0 R9A09G077M28GBG#BC0	729-pin FCBGA	Dual cores	Two CPUs	Available
	R9A09G077M08GBG#AC0 R9A09G077M08GBG#BC0	729-pin FCBGA	Single core	Two CPUs	Available
	R9A09G077M44GBG#AC0 R9A09G077M44GBG#BC0	729-pin FCBGA	Quad cores	Two CPUs	Not Available
	R9A09G077M24GBG#AC0 R9A09G077M24GBG#BC0	729-pin FCBGA	Dual cores	Two CPUs	Not Available
	R9A09G077M04GBG#AC0 R9A09G077M04GBG#BC0	729-pin FCBGA	Single core	Two CPUs	Not Available
RZ/N2H	R9A09G087M48GBG#AC0 R9A09G087M48GBG#BC0	576-pin FCBGA	Quad cores	Two CPUs	Available
	R9A09G087M28GBG#AC0 R9A09G087M28GBG#BC0	576-pin FCBGA	Dual cores	Two CPUs	Available
	R9A09G087M08GBG#AC0 R9A09G087M08GBG#BC0	576-pin FCBGA	Single core	Two CPUs	Available
	R9A09G087M44GBG#AC0 R9A09G087M44GBG#BC0	576-pin FCBGA	Quad cores	Two CPUs	Not Available
	R9A09G087M24GBG#AC0 R9A09G087M24GBG#BC0	576-pin FCBGA	Dual cores	Two CPUs	Not Available
	R9A09G087M04GBG#AC0 R9A09G087M04GBG#BC0	576-pin FCBGA	Single core	Two CPUs	Not Available

2. Issue

In rare cases, abnormal read data may be returned when the following bus masters access DDR memory.

Target bus master

- Port A0: SDHI (unit 0, 1), LCDC
- Port A1: GMAC (unit 1, 2), PCIE (unit 0, 1), USBHC, USBf, CoreSight ETR
- Port R2: DMAC (unit 0 to 2), GMAC (unit 0), CoreSight AXI-AP

Note. This issue does not affect Port R3 (Cortex-R52 CPU0, CPU1) and Port A4 (Cortex-A55).

3. Limitation

Use of the target product in the user's mass production is not recommended due to this issue.

However, it can be used for evaluation purposes by applying software that will be provided on Renesas web to reduce the likelihood of the issue occurring.

4. Revision plan

To address this issue, we will revise the target product.

Mass production of the revised version is scheduled to begin in October 2025, and the current version will be replaced by the revised one with PCN.