NEC

Customer Notification

Flash Programmer

PG-FP5-EE

Operating Precautions

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Table of Contents

Operating Precautions for PG-FP5

This document describes specifications added or changed, restrictions, and cautions on using the PG-FP5. Also refer to the user's manual of the PG-FP5 for cautions on using the PG-FP5.

Refer to the following documents for the restrictions in the target device.

- User's manual of target device
- Restrictions notification document for target device

(A) Product Version

Item No.	Control Code[Note]	Firmware	FPGA	Programming GUI	Remark
<1>	A	V1.00	V1	V1.00	
<2>		V1.01	V1	V1.00	
<3>		V2.00	V2	V2.00	
<4>		V2.01	V2	V2.01	

<Version confirmation>

- Firmware version: Displayed by selecting [Reset] from the [Programmer] menu
- FPGA version: Displayed by selecting [Reset] from the [Programmer] menu
- Programming GUI version: Displayed by selecting [About FP5] from the [Help] menu

Note The "Control Code" is the second digit from the left in the 10-digit serial number. If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP x on this label indicates the control code.

(B) Table of Additions and Changes to Specifications

No.	Outline	PG-FP5-EE			
		Product Version (Item No.)	<1>	<2>	<3>	<4>
b1	Modification of Cancel button specification		✗	○	○	○
b2	Addition of FP5 Manager functions		✗	✗	○	○
b3	Addition of communication command functions		✗	✗	○	○
b4	Addition of remote connector functions		✗	✗	○	○
b5	Change of location of [Erase memory before download] check box		✗	✗	○	○
b6	Addition of specification related to [Checksum] command display		✗	✗	○	○
b7	Addition of program file size check function		✗	✗	○	○
b8	Addition of [Enable target RESET] function		✗	✗	○	○
b9	Change of specification related to action log window view		✗	✗	○	○
b10	Change of specification related to message display view		✗	✗	○	○
b11	Addition of specification that enables specification of storage destination of ESF and PR5 files		✗	✗	○	○
b12	Addition of program file upload function		✗	✗	○	○
b13	Change of GUI language to Japanese for Japanese version OS <Japanese version only>		✗	✗	✗	○
b14	Addition of specification of UART communication at 500 kbps		✗	✗	✗	○

– : Not relevant
○ : Specification change implemented
✗ : Specification change not implemented

(C) Description of Additions and Changes to Specifications

No. b1	Modification of Cancel button specification

Details

The function of the Cancel button on the PG-FP5 main unit has been modified so that cancellation, which was applied to all commands, is only applied to the Read command.

Implementation

This item has been implemented in products with control code A (firmware: V1.01, FPGA: V1, GUI: V1.00) and later.

No. b2	Addition of FP5 Manager functions

Details

The following FP5 Manager functions have been added. Refer to the user's manual for function details.

- Password function
- Upload disable function
- Device setup disable function
- Bank mode enable function
- Simple mode enable function
- Checksum compare function
- Reset pin characteristics switch function

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b3	Addition of communication command functions

Details

The PG-FP5 main unit can now be manipulated via communication software by using communication commands, with the PG-FP5 being connected to the host machine via the serial connector. Refer to the user's manual for function details.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b4	Addition of remote connector functions

Details

The PG-FP5 main unit can now be manipulated from remote locations by connecting an external control unit to the PG-FP5 via the remote connector. Remote operation enables manipulating and checking of programming and PASS/ERROR display from the external control unit. Refer to the user's manual for function details.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b5	Change of location of [Erase memory before download] check box

Details

The location of the [Erase memory before download] check box has been moved from the [Download file] dialog box to the [Object HEX file] area on the [Target] tab in the Device Setup dialog box.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b6	Addition of specification related to [Checksum] command display

Details

The checksum result is now displayed in the message display even while the [Checksum] command is being executed, either via the programming GUI or the command option during standalone operation.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b7	Addition of program file size check function

Details

If the addresses of a downloaded program file are out of the address range set in the [Operation mode] area on the [Standard] tab in the Device Setup dialog box, warning message “WARNING: HEX file exceeds target device flash range.” is now displayed in the action log window when the Program, Verify, or Autoprocedure(E.P.) command is executed.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b8	Addition of [Enable target RESET] function

Details

The [Enable target RESET] function has been added. When this function is enabled, the RESET pin goes into input mode (Hi-Z), and the FP5 detects rising and falling edges input to the RESET pin immediately after executing a command. Refer to the user's manual for function details.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b9	Change of specification related to action log window view

Details

The message displayed in the action log window after command execution has been changed from “OK” to “PASS”. In addition, the error number is now displayed with the error message, as displayed in the message display.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b10	Change of specification related to message display view

Details

In conjunction with the addition of new functions in control code A (firmware: V2.00, FPGA: V2, GUI: V2.00), the display of all commands has been updated.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b11	Addition of specification that enables specification of storage destination of ESF and PR5 files

Details

In products with control code A (firmware: V1.01, FPGA: V1, GUI: V1.00) or earlier, the ESF and PR5 files can only be stored into the FP5_PRJ folder where the programming GUI is installed, but these files can now be stored in an arbitrary folder.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b12	Addition of program file upload function

Details

A function to upload program files has been added. Uploading can be disabled by using an FP5 Manager function.

Implementation

This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. b13	Change of GUI language to Japanese for Japanese version OS <Japanese version only>

Details

The GUI language has been changed to Japanese when used in the Japanese OS.

Implementation

This item has been implemented in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01) and later.

No. b14	Addition of specification of UART communication at 500 kbps

Details

Specifications have been changed so that 500 kbps can now be selected as the baud rate of UART communication, even if a target device other than 78K0R microcontrollers is selected. Communication at 500 kbps is not available if this specification is not supported in the target device, though. For the baud rate supported in each target device, see the user's manual for the device or a supplementary document for the parameter files. If a 78K0R microcontroller is used as the target device, communication at 500 kbps is available with Programming GUI V1.00 and later.

Implementation

This item has been implemented in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01) and later.

(D) Table of Cautions

No.	Cautions	Action
d1	Cautions for updating firmware from V2.00 to V1.xx	Described in document

(E) Description of Cautions

No. d1	Cautions for updating firmware from V2.00 to V1.xx
	Details If FP5 firmware is downgraded from V2.00 to V1.xx, the serial number that was displayed at a certain timing, such as during execution of the Reset command of the PG-FP5, is no longer displayed. In addition, the PG-FP5 can no longer operate via USB 1.1. When the PG-FP5 needs to be repaired, consult an NEC Electronics sales representative or distributor. NEC Electronics strongly recommends not to downgrade the firmware from V2.xx to V1.xx.

(F) Table of Restrictions

No.	Outline	PG-FP5-EE			
		Product Version (Item No.)	<1>	<2>	<3>	<4>
f1	Restriction whereby “Invalid Device Port” is displayed		✗	✗	✓	✓
f2	Restriction whereby standalone operation can no longer be performed under specific conditions		✗	✓	✓	✓
f3	Restriction whereby erase is performed even if [Erase memory before download] is not selected		✗	✗	✓	✓
f4	Restriction whereby status bar is displayed incorrectly		✗	✗	✓	✓
f5	Restriction whereby RESET pin is always pulled up at 5 V when Run after Disconnect is set		✗	✗	✓	✓
f6	Restriction whereby no clock is supplied when FP5CLK is selected for pseudo 3-wire communication or I2C communication		✗	✗	✓	✓
f7	Restriction whereby Motorola S type program file is not displayed in the list box		✗	✗	✓	✓
f8	Restriction whereby FLMD0 pin outputs Low when 78K0S (single-wire UART) is used		✗	✗	✓	✓
f9	Restriction whereby lowercase letters are illegally converted into uppercase letters when ‘upprm’ or ‘upset’ command is executed		✗	✗	✗	✓
f10	Restriction whereby an invalid Checksum result is obtained if a program file is downloaded in Simple mode		–	–	✗	✓
f11	Restriction whereby bank switching for the program file cannot be specified in bank mode		–	–	✗	✓

– : Not relevant
✓ : Not applicable or already corrected
✗ : Applicable

(G) Description of Restrictions

No. f1	Restriction whereby “Invalid Device Port” is displayed

Description

When a PR5 file is downloaded, the message “Invalid Device Port” may be displayed in the action log window. After that, PR5 files can no longer be downloaded correctly.

Workaround

There is no workaround.

Action

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. f2	Restriction whereby standalone operation can no longer be performed under specific conditions

Description

If execution of a command is continued using control buttons on the PG-FP5 main unit while the Programming GUI is not running, the message “ERROR: 800 Res. by Watchdog” is displayed in the message display on the PG-FP5 main unit and the subsequent operations may no longer be able to be performed.

Workaround

There is no workaround. When this situation occurs, control of the POWER button is also unavailable. Therefore, disconnect the AC adapter and connect it again to restart the PG-FP5.

Action

This issue has been corrected in products with control code A (firmware: V1.01, FPGA: V1, GUI: V1.00) and later.

No. f3	Restriction whereby erase is performed even if [Erase memory before download] is not selected

Description

Erase is performed even if the [Erase memory before download] check box is not selected in the [Download file] dialog box, which is opened via the [Object HEX file] area in the [Target] tab in the Device Setup dialog box.

Workaround

There is no workaround.

Action

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. f4	Restriction whereby status bar is displayed incorrectly

Description

The status bar is displayed incorrectly in the following cases:
(1) An error is displayed erroneously if it takes five or more seconds for SUM data to be returned during Checksum command execution.
(2) PASS is displayed erroneously if the code flash is verified to be OK and the data flash is verified to be error.

Workaround

There is no workaround.

Action

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. f5	Restriction whereby RESET pin is always pulled up at 5 V when Run after Disconnect is set

Description

The RESET pin of the PG-FP5 must go into the Hi-Z state when Run after Disconnect is set, but it is pulled up at 5 V.

Workaround

There is no workaround.

Action

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. f6	Restriction whereby no clock is supplied when FP5CLK is selected for pseudo 3-wire communication or I2C communication

Description

No clock is supplied when FP5CLK is selected for pseudo 3-wire communication or I²C communication.

Workaround

There is no workaround.

Action

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. f7	Restriction whereby Motorola S type program file is not displayed in the list box

Description

When a program file of Motorola S type (except for *.hex and *.rec) is selected in the [Download file] dialog box which is opened via the [Object HEX file] area on the [Target] tab in the Device Setup dialog box, the file is not displayed in the list box in the [Object HEX file] area.

Workaround

There is no workaround.

Action

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. f8	Restriction whereby FLMD0 pin outputs Low when 78K0S (single-wire UART) is used

Description

If the CLK and FLMD0 pins are shorted in the target system when 78K0S (single-wire UART) is used, the FLMD0 pin that should output Hi-Z incorrectly outputs Low, which disturbs programming. (This restriction is applicable only when using a microcontroller that uses the FLMD0 pin before using 78K0S (single-wire UART).)

Workaround

Execute the Reset command of the PG-FP5 or turn off and then on the PG-FP5 power before using 78K0S (single-wire UART); the FLMD0 pin afterward outputs Hi-Z.

Action

This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00) and later.

No. f9	Restriction whereby lowercase letters are illegally converted into uppercase letters when upprm or upset command is executed

Description

Letter “a” in the format version is illegally converted into “A” when the ‘upprm’ command is executed. The extension of parameter files are illegally converted into uppercase letters when the ‘upset’ command is executed. However, use of the files created by these commands does not cause problems.

Workaround

There is no workaround.

Action

This issue has been corrected in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01) and later.

No. f10	**Restriction whereby an invalid Checksum result is obtained if a program file is downloaded in Simple mode**

Description

If a program file that includes the data flash is downloaded in Simple mode, the checksum result to be displayed in the message display on the PG-FP5 main unit, which should indicate the checksum of the code flash and data flash areas, indicates the checksum of the code flash area only.

Workaround

There is no workaround.

Action

This issue has been corrected in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01) and later.

No. f11	**Restriction whereby bank switching for the program file cannot be specified in bank mode**

Description

When the PG-FP5 operates in bank mode and if a programming area is selected via a bank signal from the remote connector, the programming area selected via the bank signal should usually be selected, but the program file in the programming area selected by the Programming GUI is selected. To PR5 and ESF files, the settings selected via the bank signal are applied.

Example:
Programming area number selected by Programming GUI: 0
Programming area number selected via bank signal: 1
In this case, PR5 and ESF files in programming area 1 and the program file in programming area 0 are specified.

Workaround

There is no workaround.

Action

This issue has been corrected in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01) and later.

(H) Valid Specification

Item	Date published	Document No.	Document Title
1	March 2008	U18865EJ2V0UM00	User's Manual PG-FP5

(l) Revision History

Item	Date published	Document No.	Comment
1	24-Oct-2007	U19016EE1V0IF00	First release.
2	16-Apr-2008	U19016EE1V1IF00	Update for GUI V2.01 and firmware V2.01: - Addition of specifications (No. 13 and No. 14) - Addition of restriction (No. 11)