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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A122A/E	Rev.	1.00
Title	Corrections of “RX64M Group User's Manual:Hardware”		Information Category	Technical Notification		
Applicable Product	RX64M Group	Lot No. All	Reference Document	RX64M Group User’s Manual Hardware Rev 1.00 (R01UH0377EJ0100)		

This document describes corrections in “RX64M Group User's Manual:Hardware”

No	ChapterNo	Title	Correction
1	-	Features	Corrects the AES key lengths
2	1	Overview	・Deletes the notes in the figure 1.5 Pin Assignment (176-Pin LQFP) ・Corrects the List of Pin and Pin Functions etc
3	11	Low Power Consumption	Corrects the address of Module Stop Control Register D (MSTPCRD)
4	23	Multi-Function Pin Controller (MPC)	Adds the Pin Function Control Register of PF5(PF5PFS)
5	49	SD Host Interface (SDHI)	Corrects the value after reset of the transfer data size register (SDSIZE)
6	58	12-Bit D/A Converter (R12DA)	Corrects the Notes on the Output Amplifier

No1. 1. Ferature

・Page 69 of 2903 The following note for is corrected as follows.

Before correction

- AES (key lengths: 128, 196, and 256 bits)

After correction

- AES (key lengths: 128, 192, and 256 bits)

No2. 1. Overview

・Page 96 of 2903 The following note for the figure 1.5 Pin Assignment (176-Pin LQFP) is deleted.
But there isn't an issue with connections to VSS via a resistor.

Before correction

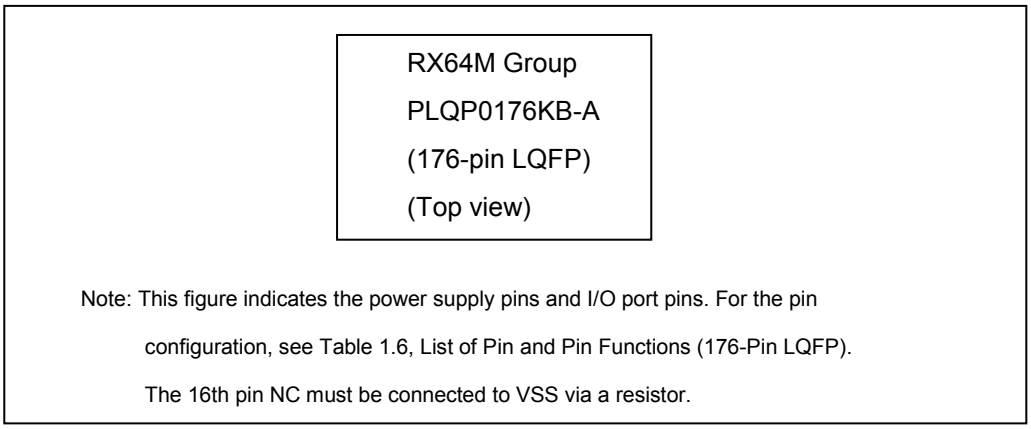

Figure 1.5 Pin Assignment (176-Pin LQFP)

After correction

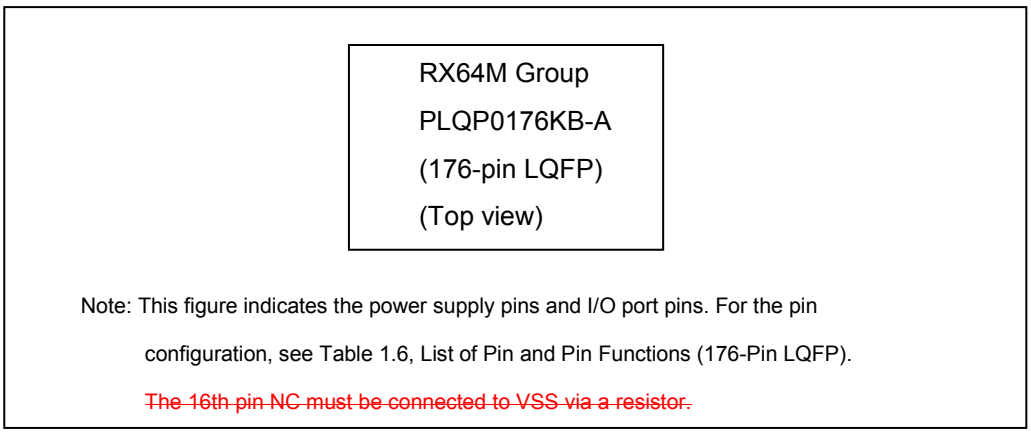

Figure 1.5 Pin Assignment (176-Pin LQFP)

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The table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/7)、(5/7) 、(6/7) is corrected as follows.

Before correction

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
M5	VCC_ USB	P12	WR3#/ BC3#	MTIC5U/TMCI1	RXD2/SMISO2/ SSCL2/ SCLO[FM+]		IRQ2	
M6	AVCC_ USBA							
M7	USBA_ RREF	P11		MTIC5V/TMCI3	SCK2/ USBA_VBUS/ USBA_VBUSEN		IRQ1	
M8	VCC_ USBA	P10	ALE	MTIC5W/TMRI3	USBA_OVRCURA		IRQ0	
R8		P11		MTIC5V/TMCI3	SCK2/ USBA_VBUS/ USBA_VBUSEN			

After correction

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
M5	VCC_ USB							
M6	AVCC_ USBA							
M7	USBA_ RREF							
M8	VCC_ USBA							
R8		P11		MTIC5V/TMCI3	SCK2/ USBA_VBUS/ USBA_VBUSEN		IRQ1	

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The table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5) (3/5) is corrected as follows.

Before correction

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
G13		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRIO/PO20	TXD5/SMOSI5/SSDA5/SSLA0-A/ET0_MDC		IRQ5-DS	
F13		PA2	A2	MTIOC7A/GTIOC1A-C/PO18	RXD5/SMISO5/SSCL5/SSLA3-A			
F12		PA1	A1	MTIOC0B/MTCLKC/MTIOC7B/GTIOC2A-C/TIOCB0/PO17	SCK5/SSLA2-A/ET0_WOL		IRQ11	
E10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/GTIOC0B-C/TIOCA0/CACREF/PO16	SSLA1-A/ET0_TX_EN/RMII0_TXD_EN			

After correction

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
G13		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRIO/PO20	TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC		IRQ5-DS	
F13		PA2	A2	MTIOC7A/GTIOC1A-C/PO18	RXD5/SMISO5/SSCL5/SSLA3-B			
F12		PA1	A1	MTIOC0B/MTCLKC/MTIOC7B/GTIOC2A-C/TIOCB0/PO17	SCK5/SSLA2-B/ET0_WOL		IRQ11	
E10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/GTIOC0B-C/TIOCA0/CACREF/PO16	SSLA1-B/ET0_TX_EN/RMII0_TXD_EN			

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The table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (4/5) is corrected as follows.

Before correction

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
92		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/SSLA0-A/ET0_MDC		IRQ5-DS	
95		PA2	A2	MTIOC7A/GTIOC1A-C/PO18	RXD5/SMISO5/SSCL5/SSLA3-A			
96		PA1	A1	MTIOC0B/MTCLKC/MTIOC7B/GTIOC2A-C/TIOCB0/PO17	SCK5/SSLA2-A/ET0_WOL		IRQ11	
97		PA0	A0/BC0#	MTIOC4A/MTIOC6D/GTIOC0B-C/TIOCA0/CACREF/PO16	SSLA1-A/ET0_TX_EN/RMII0_TXD_EN			

After correction

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
92		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC		IRQ5-DS	
95		PA2	A2	MTIOC7A/GTIOC1A-C/PO18	RXD5/SMISO5/SSCL5/SSLA3-B			
96		PA1	A1	MTIOC0B/MTCLKC/MTIOC7B/GTIOC2A-C/TIOCB0/PO17	SCK5/SSLA2-B/ET0_WOL		IRQ11	
97		PA0	A0/BC0#	MTIOC4A/MTIOC6D/GTIOC0B-C/TIOCA0/CACREF/PO16	SSLA1-B/ET0_TX_EN/RMII0_TXD_EN			

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The table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/4) is corrected as follows.

Before correction

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
F9		PA7	A7	TIOCB2/PO23	MISOA-A/ETO_WOL			

After correction

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
F9		PA7	A7	TIOCB2/PO23	MISOA-B/ETO_WOL			

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The table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (3/4) is corrected as follows.

Before correction

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
63		PA7	A7	TIOCB2/PO23	MISOA-A/ETO_WOL			

After correction

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
63		PA7	A7	TIOCB2/PO23	MISOA-B/ETO_WOL			

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The table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5) is corrected as follows.

Before correction

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
D13		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/SDHI_CD-B	IRQ6	AN104

After correction

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
D13		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/SDHI_CD-B	IRQ6	AN104

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The table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (4/5) is corrected as follows.

Before correction

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
102		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/SDHI_CD-B	IRQ6	AN104

After correction

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
102		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/SDHI_CD-B	IRQ6	AN104

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The table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/4) is corrected as follows.

Before correction

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
D7		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/SDHI_CD-B	IRQ6	AN104

After correction

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
D7		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/SDHI_CD-B	IRQ6	AN104

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The table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (3/4) is corrected as follows.

Before correction

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
72		PE6	D14[A14/D14]	TIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/SDHI_CD-B	IRQ6	AN104

After correction

Pin Number 100-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
72		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/SDHI_CD-B	IRQ6	AN104

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The table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (1/5) is corrected as follows.

Before correction

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
11		PJ5		POE#8				

After correction

Pin Number 144-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
11		PJ5		POE#8	CTS2#/RTS2#/SS2#			

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The table1.1 Outline of Specifications (9/9) is corrected as follows.

Before correction

Classification	Module/Function	Description
Encryption function	AES	・Key lengths: 128, 196, and 256 bits

After correction

Classification	Module/Function	Description
Encryption function	AES	・Key lengths: 128, 192, and 256 bits

No3. 11. Low Power Consumption

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The address of Module Stop Control Register D (MSTPCRD) is corrected as follows.

Before correction

Address(es): 0008 001Ah

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	–	–	–	–	–	–	–	–	MSTPD23	–	MSTPD21	–	MSTPD19	–	–	–
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPD15	MSTPD14	–	–	–	–	–	–	MSTPD7	MSTPD6	MSTPD5	MSTPD4	MSTPD3	MSTPD2	MSTPD1	MSTPD0
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

After correction

Address(es): 0008 001Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	–	–	–	–	–	–	–	–	MSTPD23	–	MSTPD21	–	MSTPD19	–	–	–
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPD15	MSTPD14	–	–	–	–	–	–	MSTPD7	MSTPD6	MSTPD5	MSTPD4	MSTPD3	MSTPD2	MSTPD1	MSTPD0
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

No.4 23. Multi-Function Pin Controller (MPC)

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The bit of PFn Pin Function Control Register (PFnPFS) is corrected as follows.

Before correction

23.2.17 PFn Pin Function Control Register (PFnPFS) (n = 0 to 2)

Address(es): PF0PFS 0008 C1B8h, PF1PFS 0008 C1B9h, PF2PFS 0008 C1BAh

	b7	b6	b5	b4	b3	b2	b1	b0
	–	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

After correction

23.2.17 PFn Pin Function Control Register (PFnPFS) (n = 0 to 2、5)

Address(es): PF0PFS 0008 C1B8h, PF1PFS 0008 C1B9h, PF2PFS 0008 C1BAh, PF5PFS 0008 C1BDh

	b7	b6	b5	b4	b3	b2	b1	b0
	–	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

No5. 49. SD Host Interface (SDHI)

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The value after reset of the transfer data size register (SDSIZE) is corrected as follows,

Before correction

Address 0008 AC4Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Symbol																							LEN[9:0]									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

After correction

Address 0008 AC4Ch

Bit	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Symbol																							LEN[9:0]									
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

No.6. 58. 12-Bit D/A Converter (R12DA)

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The document of 58.6.5 Notes on the Output Amplifier is corrected as follows,

Before Correction

When the output amplifier is used, an amplifier output should be executed under the following initial procedures. An
example for channel 0 is described below.

1. Write 000h to the DADR0 register.
2. Set the DACR.DAE bit or the DACR.DAOE0 bit to 1.
3. Set the DAAMPCR.DAAMP0 bit to 1 to start up the amplifier.
4. Write the value to be converted in the DADR0 register after waiting for 3μs.

After Correction

When the output amplifier is used, an amplifier output should be executed under the following initial procedures. An
example for channel 0 is described below.

1. Write 000h to the DADR0 register.
2. Set the DAAMPCR.DAAMP0 bit to 1.
3. Set the DACR.DAE bit or the DACR.DAOE0 bit to 1 to start up the amplifier.
4. Write the value to be converted in the DADR0 register after waiting for 3μs.