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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A120A/E	Rev.	1.00
Title	Corrections of "RX630 Group User's Manual: Hardware" and "RX63N Group, RX631 Group User's Manual: Hardware"		Information Category	Technical Notification		
Applicable Product	RX630 group RX63N, RX631 group	Lot No. All lots	Reference Document	RX630 group RX63N, RX631 group User's Manual, Hardware section		

This document describes corrections in "RX630 Group Use's Manual: Hardware" and "RX63N Group, RX631 Group User's Manual: Hardware". Changes are underlined in the list below.

- Description in "Over view" chapter is corrected as follows.
  - Target Product : RX63N, RX631 Group (page 106 to 114 of 2029)

The following note is eliminated from "Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA)" and "Table 1.10 List of Pins and Pin Functions (100-Pin LQFP)".

~~"Note 1. Enabled only for the ROM capacity of 768 Kbytes or more"~~

- Description in "Multi-Function Pin Controller (MPC)" chapter is corrected as follows.
  - Target Product : RX63N, RX631 Group (page 709 to 710 of 2029)

[Before correction]

22.2.2 P0n Pin Function Control Register (P0nPFS) (n = 0 to 3, 5, 7)

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see the below.	R/W
b5	-	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0 : Not used as IRQn input pin 1 : Used as IRQn input pin	R/W
b7	ASEL	Analog Input Function Select	0 : Used other than as analog pin. 1 : Used as analog pin.	R/W

Table 22.4 Register Setting for Input/Output Pin function in 64-Pin LQFP, 64-Pin TFLGA

	Pin
PSEL[4:0] Settings	P05
00000b (initial value)	Hi-Z
00101b	-
01001b	ADTRG0#
01010b	-

[Corrections]

22.2.2 P0n Pin Function Control Register (P0nPFS) (n = 0 to 3, 5, 7)

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PSEL[4:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see the below.	R/W
b5	-	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0 : Not used as IRQn input pin 1 : Used as IRQn input pin	R/W
b7	ASEL	Analog Function Select	0 : Used other than as analog pin. 1 : Used as analog pin. P03 : DA0 (177/176/145/144 pins) P05 : DA1 (177/176/145/144/100/64 pins)	R/W

Table 22.4 Register Setting for Input/Output Pin function in 64-Pin LQFP, 64-Pin TFLGA

	Pin
PSEL[4:0] Settings	P05
00000b (initial value)	Hi-Z
00101b	-
01001b	-
01010b	-

- Description in “USB2.0 Function Module (USBa)” chapter is corrected as follows.
  - Target Product : RX630 Group (page 965 of 1681)

[Before correction]

31.2.1 System Configuration Control Register (SYSCFG)

SCKE Bit (USB Module Clock Enable)

The SCKE bit stops or enables supplying 48-MHz clock signals to the USB module.

When this bit is 0, only SYSCFG, DMA0PCFG, and DMA1PCFG can be read from and written to; the other registers in the USB module cannot be read from or written to.

[Corrections]

31.2.1 System Configuration Control Register (SYSCFG)

SCKE Bit (USB Module Clock Enable)

The SCKE bit stops or enables supplying 48-MHz clock signals to the USB module.

When this bit is 0, only SYSCFG can be read from and written to; the other registers in the USB module cannot be read from or written to.

- Description in “Flash Memory” chapter is corrected as follows.
  - Target Product : RX630 Group (page 1491 of 1681)
    RX63N, RX631 Group (page 1793 of 2029)

The following describes correction using an example RX630 Group.

[Before correction]

Table 43.2 Correspondence between Blocks and Addresses of the User Area

Block No.	Start Address	Block Configuration	Area
69	FFE0 0000h	64 Kbyte x8 blocks	Area 3
68	FFE1 0000h		
…			
12	FFFE 4000h	16 Kbyte x22 blocks	Area 0
11	FFFE 8000h		
10	FFFE C000h		
9	FFFF 0000h		
8	FFFF 4000h		
7	FFFF 8000h	4 Kbyte x8 blocks	
6	FFFF 9000h		
5	FFFF A000h		
4	FFFF B000h		
3	FFFF C000h		
2	FFFF D000h		
1	FFFF E000h		
0	FFFF F000h		

[Corrections]

Table 43.2 Correspondence between Blocks and Addresses of the User Area

Block No.	Start Address	Block Configuration	Area
69	FFE0 0000h	64 Kbyte x8 blocks	Area 3
68	FFE1 0000h		
…			
12	FFFE 4000h	16 Kbyte x22 blocks	Area 0
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10	FFFE C000h		
09	FFFF 0000h		
08	FFFF 4000h		
07	FFFF 8000h	4 Kbyte x8 blocks	
06	FFFF 9000h		
05	FFFF A000h		
04	FFFF B000h		
03	FFFF C000h		
02	FFFF D000h		
01	FFFF E000h		
00	FFFF F000h		

- Description in “Flash Memory” chapter is corrected as follows.
  - Target Product : RX630 Group (page 1545 of 1681)
    RX63N, RX631 Group (page 1847 of 2029)

The following describes correction using an example RX630 Group.

[Before correction]

43.7 User Boot Mode

In user boot mode, the desired communications interface can be used for programming and erasing of the user area and data area. After a user boot program is written to the area, release the chip from the reset state by applying the low level to the MD pin and the high level to the PC7 pin.

At the time of shipment, the USB boot program is stored in the user boot area. To use user boot mode, after the chip starts up in boot mode, the USB boot program must be erased and a user boot program written to the user boot area. Accordingly, dynamic switching between user boot mode and USB boot mode is not possible without modifying the program.

After the chip has started up in user boot mode, setting the SYSCR0.EXBE bit to 1 (enabling the external bus) enables operation in on-chip ROM enabled extended mode.

[Corrections]

43.7 User Boot Mode

In user boot mode, the desired communications interface can be used for programming and erasing of the user area and data area. After a user boot program is written to the area, release the chip from the reset state by applying the low level to the MD pin and the high level to the PC7 pin.

The reset vector at this time points to the address FF7F FFFCh of the user boot area. For other vector tables, refer to normal vector table (see section 15, Interrupt controller (ICUb)).

At the time of shipment, the USB boot program is stored in the user boot area. To use user boot mode, after the chip starts up in boot mode, the USB boot program must be erased and a user boot program written to the user boot area. Accordingly, dynamic switching between user boot mode and USB boot mode is not possible without modifying the program.

After the chip has started up in user boot mode, setting the SYSCR0.EXBE bit to 1 (enabling the external bus) enables operation in on-chip ROM enabled extended mode.

- Description in “Flash Memory” chapter is corrected as follows.
  - Target Product : RX630 Group (page 1574 of 1681)
    RX63N, RX631 Group (page 1878 of 2029)

The following describes correction using an example RX630 Group.

[Before correction]

43.11 ROM Code Protection

ROM code protection is a facility for prohibiting a PROM programmer from reading from or programming flash memory. The ROM code in flash memory is a 32-bit code. Figure 43.37 shows the configuration of the ROM code. Set the ROM code in 32-bit units.

For release from ROM code protection, erase the EB00 block of the user area that contains the ROM code in boot mode or by user programming.

[Corrections]

43.11 ROM Code Protection

ROM code protection is a facility for prohibiting a PROM programmer from reading from or programming flash memory. The ROM code in flash memory is a 32-bit code. Figure 43.37 shows the configuration of the ROM code. Set the ROM code in 32-bit units.

For release from ROM code protection, erase the 00 block of the user area that contains the ROM code in boot mode or by user programming.

< Reference Documents >

Applicable Product	Manual Title	Rev.	Document Number
RX630 Group	RX630 Group User's Manual Hardware	1.60	R01UH0040EJ0160
RX63N, RX631 Group	RX63N Group, RX631 Group User's Manual Hardware	1.80	R01UH0041EJ0180