Date: Jul. 14, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0089A/E	Rev.	1.00
Title	Corrections of Peripheral Variant for CANFD		Information Category	Technical Notification		
Applicable Product	RA6T2 group	Lot No. All	Reference Document	Renesas RA6T2 Group User's Manual: Hardware Rev.1.30		

This document shows corrections of peripheral variant for CANFD.

[Before correction]

28. CAN with Flexible Data-rate (CANFD)

This is the CANFD_B version of the CANFD peripheral module.
CANFD_B is referred to as CANFD in this chapter.

[After correction]

28. CAN with Flexible Data-rate (CANFD)

(Removed)

[Before correction]

(Please refer applicable chapters in Table 1.)
Base address: CANFD_B = 0x400B_0000

[After correction]

Base address: CANFD = 0x400B_0000

Table 1. List of applicable chapters

28.2.3	CFDC0NCFG : Channel 0 Nominal Bitrate Configuration Register
28.2.4	CFDC0CTR : Channel 0 Control Register
28.2.5	CFDC0STS : Channel 0 Status Register
28.2.6	CFDC0ERFL : Channel 0 Error Flag Register
28.2.7	CFDC0DCFG : Channel 0 Data Bitrate Configuration Register
28.2.8	CFDC0FDCFG : Channel 0 CANFD Configuration Register
28.2.9	CFDC0FDCTR : Channel 0 CANFD Control Register
28.2.10	CFDC0FDSTS : Channel 0 CANFD Status Register
28.2.11	CFDC0FDCRC : Channel 0 CANFD CRC Register
28.2.12	CFDGCFG : Global Configuration Register
28.2.13	CFDGCTR : Global Control Register
28.2.14	CFDGSTS : Global Status Register
28.2.15	CFDGERFL : Global Error Flag Register
28.2.16	CFDGTINTSTS : Global TX Interrupt Status Register
28.2.17	CFDGTSC : Global Timestamp Counter Register
28.2.18	CFDGAFLECTR : Global Acceptance Filter List Entry Control Register
28.2.19	CFDGAFLCFG : Global Acceptance Filter List Configuration Register
28.2.20	CFDGAFLIDr : Global Acceptance Filter List ID Registers (r = 1 to 16)
28.2.21	CFDGAFLMr : Global Acceptance Filter List Mask Registers (r = 1 to 16)
28.2.22	CFDGAFLP0r : Global Acceptance Filter List Pointer 0 Registers (r = 1 to 16)
28.2.23	CFDGAFLP1r : Global Acceptance Filter List Pointer 1 Registers (r = 1 to 16)

28.2.24	CFDRMNB : RX Message Buffer Number Register
28.2.25	CFDRMND : RX Message Buffer New Data Register
28.2.26	CFDRFCCa : RX FIFO Configuration/Control Registers a (a = 0 to 1)
28.2.27	CFDRFSTSa : RX FIFO Status Registers a (a = 0 to 1)
28.2.28	CFDRFPCTRa : RX FIFO Pointer Control Registers a (a = 0 to 1)
28.2.29	CFDCFCC : Common FIFO Configuration/Control Register
28.2.30	CFDCFSTS : Common FIFO Status Register
28.2.31	CFDCFPCTR : Common FIFO Pointer Control Register
28.2.32	CFDFESTS : FIFO Empty Status Register
28.2.33	CFDFFSTS : FIFO Full Status Register
28.2.34	CFDFMSTS : FIFO Message Lost Status Register
28.2.35	CFDRFISTS : RX FIFO Interrupt Flag Status Register
28.2.36	CFDCDTCT : DMA Transfer Control Register
28.2.37	CFDCDTSTS : DMA Transfer Status Register
28.2.38	CFDTMCi : TX Message Buffer Control Registers i (i = 0 to 3)
28.2.39	CFDTMSTSj : TX Message Buffer Status Registers j (j = 0 to 3)
28.2.40	CFDTMTRSTS : TX Message Buffer Transmission Request Status Register
28.2.41	CFDTMTARSTS : TX Message Buffer Transmission Abort Request Status
28.2.42	CFDTMTCSTS : TX Message Buffer Transmission Completion Status Register
28.2.43	CFDTMTASTS : TX Message Buffer Transmission Abort Status Register
28.2.44	CFDTMIEC : TX Message Buffer Interrupt Enable Configuration Register
28.2.45	CFDTXQCC : TX Queue Configuration/Control Register
28.2.46	CFDTXQSTS : TX Queue Status Register
28.2.47	CFDTXQPCTR : TX Queue Pointer Control Register
28.2.48	CFDTHLCC : TX History List Configuration/Control Register
28.2.49	CFDTHLSTS : TX History List Status Register
28.2.50	CFDTHLACC0 : TX History List Access Register 0
28.2.51	CFDTHLACC1 : TX History List Access Register 1
28.2.52	CFDTHLPCTR : TX History List Pointer Control Register
28.2.53	CFDGRSTC : Global SW reset Register
28.2.54	CFDGTSTCFG : Global Test Configuration Register
28.2.55	CFDGTSTCTR : Global Test Control Register
28.2.56	CFDGFDCFG : Global FD Configuration Register
28.2.57	CFDGLOCKK : Global Lock Key Register
28.2.58	CFDRPGACCk : RAM Test Page Access Registers k (k = 0 to 63)
28.2.59	CFDGAFLIGNENT : Global AFL Ignore Entry Register
28.2.60	CFDGAFLIGNCTR : Global AFL Ignore Control Register
28.2.61	CFDRMIEC : RX Message Buffer Interrupt Enable Configuration Register
28.2.62.2	CFDRMBCPb[0] : RX Message Buffer Component b (b = 0 to 31)
28.2.62.3	CFDRMIDb : RX Message Buffer ID Registers (b = 0 to 31)
28.2.62.4	CFDRMPTRb : RX Message Buffer Pointer Registers (b = 0 to 31)
28.2.62.5	CFDRMFDSTSb : RX Message Buffer CANFD Status Registers (b = 0 to 31)
28.2.62.6	CFDRMDFb_p : RX Message Buffer Data Field p Registers (p = 0 to 15, b = 0 to 31)
28.2.62.7	CFDRFMBCPb[0] : RX FIFO Access Message Buffer Component b (b = 0 to 1)
28.2.62.8	CFDRFIDb : RX FIFO Access ID Register b (b = 0 to 1)
28.2.62.9	CFDRFPTRb : RX FIFO Access Pointer Register b (b = 0 to 1)
28.2.62.10	CFDRFFDSTSb : RX FIFO Access CANFD Status Register b (b = 0 to 1)
28.2.62.11	CFDRFDFb_p : RX FIFO Access Data Field p Register b (p = 0 to 15, b = 0 to 1)
28.2.62.12	CFDCFMBCP0[0] : Common FIFO Access Message Buffer Component
28.2.62.13	CFDCFID : Common FIFO Access ID Register
28.2.62.14	CFDCFPTR : Common FIFO Access Pointer Register
28.2.62.15	CFDCFFDCSTS : Common FIFO Access CANFD Control/Status Register
28.2.62.16	CFDCFDFp : Common FIFO Access Data Field p Registers (p = 0 to 15)
28.2.62.17	CFDTMBCPb[0] : TX Message Buffer Component b (b = 0 to 3)
28.2.62.18	CFDTMIDb : TX Message Buffer ID Registers (b = 0 to 3)
28.2.62.19	CFDTMPTRb : TX Message Buffer Pointer Register (b = 0 to 3)
28.2.62.20	CFDTMFDCTRb : TX Message Buffer CANFD Control Register (b = 0 to 3)
28.2.62.21	CFDTMDFb_p : TX Message Buffer Data Field Register (p= 0 to 15 , b= 0 to 3)

[Before correction]

Appendix 3. I/O Registers

Table 3.1 Peripheral base address (2 of 3)

Name	Description	Base address
KINT	Key Interrupt Function	0x4008_5000
POEG	Port Output Enable for GPT	0x4008_A000
CANFD_B	CANFD Module Control	0x400B_0000

[After correction]

Appendix 3. I/O Registers

Table 3.1 Peripheral base address (2 of 3)

Name	Description	Base address
KINT	Key Interrupt Function	0x4008_5000
POEG	Port Output Enable for GPT	0x4008_A000
CANFD	CANFD Module Control	0x400B_0000

[Before correction]

Appendix 4. Peripheral Variant

Table 4.1 shows the correspondence between the module neme used in this manual and the Peripheral Variant.

Table 4.1 Module name vs Peripheral Variant

Module name	Peripheral Variant
ELC	ELC_B
AGTW	AGTW_B
SCI	SCI_B
IIC	IIC_B
CANFD	CANFD_B
SPI	SPI_B
SCE5	SCE5_B
ADC	ADC_B
DOC	DOC_B

[After correction]

Appendix 4. Peripheral Variant

Table 4.1 shows the correspondence between the module neme used in this manual and the Peripheral Variant.

Table 4.1 Module name vs Peripheral Variant

Module name	Peripheral Variant
ELC	ELC_B
AGTW	AGTW_B
SCI	SCI_B
IIC	IIC_B
CANFD	CANFD
SPI	SPI_B
SCE5	SCE5_B
ADC	ADC_B
DOC	DOC_B