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RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A074A/E	Rev.	1.00
Title	Corrections of the electrical characteristics in the 'RX21A Group User's Manual: Hardware Rev.1.00'		Information Category	Technical Notification		
Applicable Product	RX21A Group	Lot No. All	Reference Document	RX21A Group User's Manual: Hardware Rev.1.00 (R01UH0251EJ0100)		

This document describes the corrections of the electrical characteristics in the 'RX21A Group User's Manual: Hardware Rev.1.00'. Changes are underlined in the list below.

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Change 'Table 44.3 DC Characteristics (2)'.

Original

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage						V	
	All input pins	ΔVT	VCC **× 0.03**	-	-		

Correction

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage							V	
	Port 0 to 5 **Port A to J**	**VCC ≥ 2.2V**	ΔVT	VCC **× 0.05**	-	-		
		VCC < 2.2V		VCC **× 0.03**				
	RES#			VCC **× 0.1**				

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Add the missing item in 'Table 44.4 DC Characteristics (3)'.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, **P35/**NMI	|Iin|	—	—	1.0	μA	Vin = 0 V, VCC

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Change the value in ‘Table 44.6 DC Characteristics (5)’.

Original

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode		I_{CC}			mA	
		Increase during BGO operation*2		30	—		

Correction

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode		I_{CC}			mA	
		Increase during BGO operation*2		23	—		

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Change the values in ‘Table 44.6 DC Characteristics (6)’.

Original

Item				Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Medium-speed operating modes 1A and 1B			I_{CC}			mA	
		Increase during BGO operation*2	Medium-speed operating mode 1A		31	—		
			Medium-speed operating mode 1B		39	—		
	Medium-speed operating modes 2A and 2B							
		Increase during BGO operation*2	Medium-speed operating mode 2A		24	—		
			Medium-speed operating mode 2B		35	—		

Correction

Item				Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Medium-speed operating modes 1A and 1B			I_{CC}			mA	
		Increase during BGO operation*2	Medium-speed operating mode 1A		23	—		
			Medium-speed operating mode 1B		20	—		
	Medium-speed operating modes 2A and 2B							
		Increase during BGO operation*2	Medium-speed operating mode 2A		23	—		
			Medium-speed operating mode 2B		20	—		

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Insert a table before ‘Table 44.9 DC Characteristics (8)’.

Correction

Table 44.X DC Characteristics (X)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0V

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	350	mW	Ta = –40 to 85°C
		—	150		85°C < Ta ≤ 105°C *2

Note 1. Total power dissipated by the entire chip (including output currents)

Note 2. In addition, refer to Application Note R01AN1717EJ.

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Add conditions of 'Table 44.9 DC Characteristics (8)'.

Correction

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, **VREFH = 1.8 to AVCC0, VREFH0 = 1.8 to AVCC0,**

VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, Ta = –40 to +105°C

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Change 'Table 44.13 DC Characteristics (12)'.

Original

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,

Ta = –40 to +105°C

The ripple voltage must meet at least either Vr(VCC) or dt/dVr(VCC). In either of these cases, fr(VCC) must be met.

Item	Symbol	Min.	Typ.	Max.	Unit
Allowable ripple voltage	$Vr_{(VCC)}$	—	—	VCC × 0.2	V
Ripple voltage rising/falling gradient	$\frac{dt}{dVr_{(VCC)}}$	1.0	—	—	ms/V
Allowable ripple frequency	$fr_{(VCC)}$	—	—	10	kHz

Correction

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,

Ta = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency fr(VCC) within the range between the VCC upper limit (3.6 V) and lower limit (1.8 V).

When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	fr(VCC)	—	—	10	kHz	Figure 44.10 VCC × 0.1 < Vr(VCC) ≤ VCC × 0.2
		—	—	1	MHz	Figure 44.10 VCC × 0.05 < Vr(VCC) ≤ VCC × 0.1
		—	—	10	MHz	Figure 44.10 Vr(VCC) ≤ VCC × 0.05
Allowable voltage change rising/ falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

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Replace ‘Table 44.14 with two tables.

Original

Table 44.14 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,

Ta = –40 to +105°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per 1 pin)		Normal output mode	I_{OL}	**4.0**	mA
		High-drive output mode		**8.0**	
Permissible output low current (maximum value per 1 pin)		Normal output mode		**4.0**	mA
		High-drive output mode		**8.0**	
Permissible output low current (total)	Total of all output pins	Ta = –40 to +85°C	I_{OL}	**60**	mA
		Ta = +85 to +105°C		**45**	
Permissible output high current (average value per 1 pin)		Normal output mode	I_{OH}	**-4.0**	mA
		High-drive output mode		**-8.0**	
Permissible output high current (maximum value per 1 pin)		Normal output mode		**-4.0**	mA
		High-drive output mode		**-8.0**	
Permissible output high current (total)	Total of all output pins		I_{OH}	**-60**	mA

Correction

Table 44.14 Permissible Output Currents(1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,

when total power (mW) < 1000 – 10 × Ta

Item		Symbol	Max.	Unit
Permissible output low current (maximum value per 1 pin)	Normal output mode	I_{OL}	4.0	mA
	High-drive output mode		8.0	
Permissible output low current (total)	Total of all output pins	I_{OL}	60	
Permissible output low current (maximum value per 1 pin)	Normal output mode	I_{OH}	-4.0	
	High-drive output mode		-8.0	
Permissible output high current (total)	Total of all output pins	I_{OH}	-60	

Table 44.xx Permissible Output Currents(2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,

when total power (mW) ≥ 1000 – 10 × Ta

Item		Symbol	Max.	Unit
Permissible output low current (maximum value per 1 pin)	Normal output mode	I_{OL}	**2.0**	mA
	High-drive output mode		**4.0**	
Permissible output low current (total)	Total of all output pins	I_{OL}	**30**	
Permissible output low current (maximum value per 1 pin)	Normal output mode	I_{OH}	**-2.0**	
	High-drive output mode		**-4.0**	
Permissible output high current (total)	Total of all output pins	I_{OH}	**-30**	

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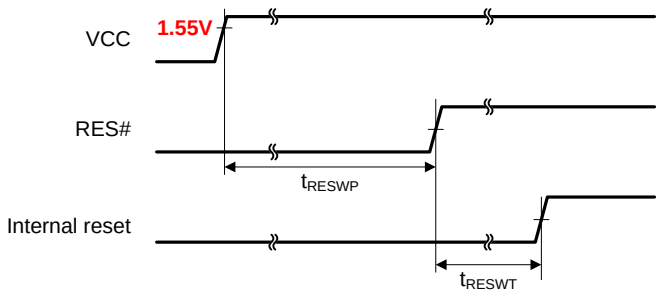
Add reset-start timing in ‘Figure 44.35 Reset Input Timing at Power-On’.



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Change the values in ‘Table 44.31 Timing of On-Chip Peripheral Modules (4)’.

Original

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI						
	SS input setup time	tLEAD	1	—	tSPcyc	C = 30 pF Figure 44.50 to Figure 44.53
	SS input hold time	tLAG	1	—	tSPcyc	

Correction

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI						
	SS input setup time	tLEAD	6	—	tPcyc	C = 30 pF Figure 44.50 to Figure 44.53
	SS input hold time	tLAG	6	—	tPcyc	

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Correct 'Table 44.35 A/D Conversion Characteristics (1)'.

Original

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0*4,

VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, fPCLKD = 1 to 25 MHz, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	10	Bit	
Conversion time*1 (Operation at fPCLKD = 25 MHz)*3	Permissible signal source impedance (Max.) = 1.5 kΩ	2.0 (1.0)*2	—	—	µs	Sampling in 25 states
Analog input capacitance		—	—	5	pF	
Offset error		—	±1.0	±2.0	LSB	
Full-scale error		—	±1.0	±2.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.0	±3.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.0	LSB	
INL integral nonlinearity error		—	±1.0	±2.0	LSB	

Note: • The characteristics include quantization errors and apply when no pin functions other than A/D converter input are used.

Note: • In 64-pin LQFP packages, the absolute accuracy of channel AN4 may deteriorate by about ±1.5 LSB and the DNL differential nonlinearity error may deteriorate by about ±0.5 LSB.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. The lower-limit frequency of PCLKD is 1 MHz.

Note 4. When using the temperature sensor, use it when AVCC0 = VREFH0.

Correction

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0*3,

VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	25		
Resolution		—	—	10	Bit	
Conversion time*1 (Operation at fPCLKD = 25 MHz)	Permissible signal source impedance (Max.) = 1.5 kΩ	2.0 (1.0)*2	—	—	µs	Sampling in 25 states
Analog input capacitance		—	—	5	pF	
Offset error		—	±1.0	±2.0	LSB	
Full-scale error		—	±1.0	±2.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.0	±3.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.0	LSB	
INL integral nonlinearity error		—	±1.0	±2.0	LSB	

Note: • PCLKD must be set to 40 MHz or lower when HOCO is to be selected as the A/D conversion clock. The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, fullscale error, DNL differential nonlinearity error, and INL integral nonlinearity

error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. When using the temperature sensor, use it when AVCC0 = VREFH0.

Note 4. The characteristics of the channel AN4 on a 64-pinLQFP may inferior to the values on this table; ±1.5LSB in Absolute accuracy, ±0.5LSB in DNL differential nonlinearity error.

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Add ‘Figure 44.xx AVCC to VREFH0 Voltage Range’ at the next to ‘Table 44.35 A/D Conversion Characteristics (1)’.

Figure numbers of 44.61 to 69 should be incremented by 1.

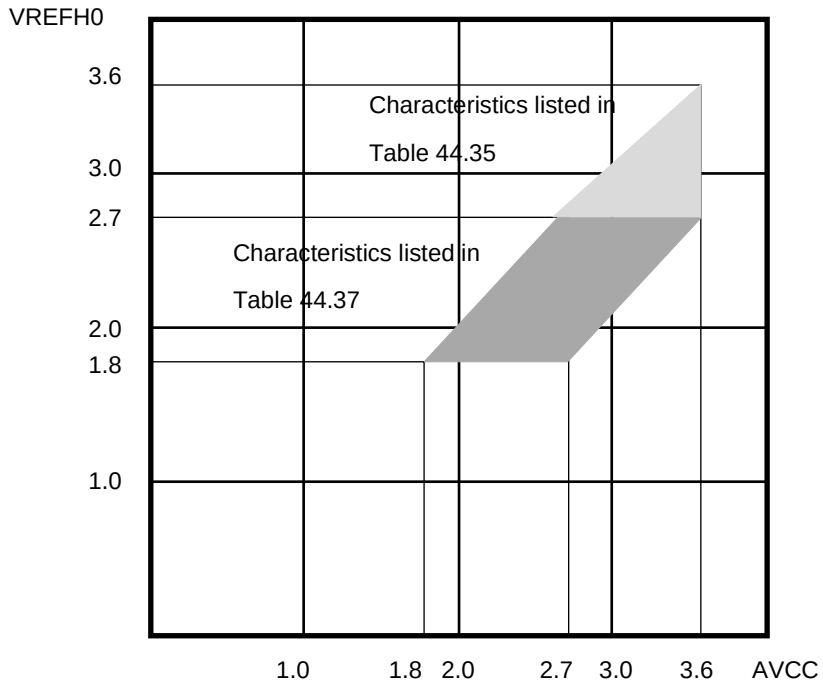

Figure 44.61 AVCC to VREFH0 Voltage Range

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Correct 'Table 44.37 A/D Conversion Characteristics (2)'.

Original

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, **VREFH0 = (AVCC0 – 0.9 V) to AVCC0*4, VREFH0 ≥ 1.8 V,**

VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, **fPCLKD = 1 to 12.5 MHz,** Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	10	bit	
Conversion time*1 (Operation at fPCLKD = 12.5 MHz) ***3**	Permissible signal source impedance (Max.) = 1.5 kΩ	4.0 (2.0)*2	—	—	µs	Sampling in 25 states
Analog input capacitance		—	—	5	pF	
Offset error		—	±1.5	±3.0	LSB	
Full-scale error		—	±1.5	±3.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.0	±4.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.0	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: • **The characteristics include quantization errors and apply when no pin functions other than A/D converter input are used.**

Note: • In 64-pin LQFP packages, the absolute accuracy of channel AN4 may deteriorate by about ±1.5 LSB and the DNL differential nonlinearity error may deteriorate by about ±0.5 LSB.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. **The lower-limit frequency of PCLKD is 1 MHz.**

Note 4. When using the temperature sensor, use it when AVCC0 = VREFH0.

Correction

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, **1.8 V ≤ VREFH0 ≤ 2.7 V, AVCC0-0.9 V ≤ VREFH0 ≤ AVCC0*3,**

VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		**1**	—	**12.5**		
Resolution		—	—	10	bit	
Conversion time*1 (Operation at fPCLKD = 12.5 MHz) ***3**	Permissible signal source impedance (Max.) = 1.5 kΩ	4.0 (2.0)*2	—	—	µs	Sampling in 25 states
Analog input capacitance		—	—	5	pF	
Offset error		—	±1.5	±3.0	LSB	
Full-scale error		—	±1.5	±3.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.0	±4.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.0	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: **The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.**

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. When using the temperature sensor, use it when AVCC0 = VREFH0.

Note 4. The characteristics of the channel AN4 on a 64-pinLQFP may inferior to the values on this table; ±1.5LSB in Absolute accuracy, ±0.5LSB in DNL differential nonlinearity error.