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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-H8*-A436A/E	Rev.	1.00
Title	Corrections to Conditions for Multiplexed Functions of I/O Port Pins		Information Category	Technical Notification		
Applicable Product	H8S/2472, H8S/2463, H8S/2462 Group	Lot No. All lots	Reference Document	H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual (REJ09B0403 Rev.2.00)		

Regarding the conditions for selecting multiplexed functions of the I/O port pins for the H8S/2472, H8S/2463, H8S/2462 Groups, we would like to inform you of the corrections shown below.

1. Object of Corrections

Conditions for multiplexed functions of I/O port pins

2. Corrections

(1) P55/$\overline{\text{IRQ13}}$/SSI (On pages 218 and 301)

[Before correction]

The pin function is switched as shown below according to the RE bit in SSER of the SSU and the P55DDR bit.

RE	0		1
P55DDR	0	1	X
Pin function	P55 input pin $\overline{\text{IRQ13}}$ input pin	P55 output pin	SSI input pin

[Legend] X: Don't care.

[After correction]

The pin function is switched as shown below according to the state of SSU transmission/reception and the P55DDR bit. To use the pin as the SSI input/output pin, clear the P55DDR bit to 0. For details on the SSU transmission/reception, see section 17.4.4, Communication Modes and Pin Functions.

SSU	Not in transmission/reception mode		In transmission/reception mode*
P55DDR	0	1	0
Pin function	P55 input pin $\overline{\text{IRQ13}}$ input pin	P55 output pin	SSI input/output pin

[Legend] * To use the pin as the SSI input/output pin, clear the P55DDR bit to 0. For details on the SSU transmission/reception, see section 17.4.4, Communication Modes and Pin Functions.

(2) P54/$\overline{\text{IRQ12}}$/SSO (On pages 218 and 301)

[Before correction]

The pin function is switched as shown below according to the TE bit in SSER of the SSU and the P54DDR bit.

TE	0		1
P54DDR	0	1	X
Pin function	P54 input pin $\overline{\text{IRQ12}}$ input pin	P54 output pin	SSO output pin

[Legend] X: Don't care.

[After correction]

The pin function is switched as shown below according to the state of SSU transmission/reception and the P54DDR bit. To use the pin as the SSI input/output pin, clear the P54DDR bit to 0. For details on the SSU transmission/reception, see section 17.4.4, Communication Modes and Pin Functions.

SSU	Not in transmission/reception mode		In transmission/reception mode*
P54DDR	0	1	0
Pin function	P54 input pin $\overline{\text{IRQ12}}$ input pin	P54 output pin	SSO input/output pin

[Legend] * To use the pin as the SSI input/output pin, clear the P54DDR bit to 0. For details on the SSU transmission/reception, see section 17.4.4, Communication Modes and Pin Functions.

(3) P67/$\overline{\text{ExIRQ8}}$/SSCK (On pages 224 and 307)

[Before correction]

The pin function is switched as shown below according to the SCKS bit in SSCRH of the SSU and the P67DDR bit.

SCKS	0		1
P67DDR	0	1	X
Pin function	P67 input pin $\overline{\text{ExIRQ8}}$ input pin	P67 output pin	SSCK I/O pin

[Legend] X: Don't care.

[After correction]

The pin function is switched as shown below according to the SSUMS bit in SSCRL of the SSU, the TE and RE bits in SSER, and the P67DDR bit. To use the pin as the SSCK input/output pin, clear the P67DDR bit to 0.

SSUMS	0		1	0	
TE	0		X	1	X
RE	0		X	X	1
P67DDR	0	1	0		
Pin function	P67 input pin $\overline{\text{ExIRQ8}}$ input pin	P67 output pin	SSCK I/O pin		

[Legend] X: Don't care.

(4) P66/$\overline{\text{ExIRQ9}}$/$\overline{\text{SCS}}$ (On pages 224 and 307)

[Before correction]

The pin function is switched as shown below according to the CSS1 and CSS0 bits in SSCRH of the SSU and the P66DDR bit.

CSS1, CSS0	00		01 or 1X
P66DDR	0	1	X
Pin function	P66 input pin $\overline{\text{ExIRQ9}}$ input pin	P66 output pin	$\overline{\text{SCS}}$ I/O pin

[Legend] X: Don't care.

[After correction]

The pin function is switched as shown below according to the SSUMS bit in SSCRL of the SSU, the TE and RE bits in SSER, and the P66DDR bit. To use the pin as the $\overline{\text{SCS}}$ input/output pin, clear the P66DDR bit to 0.

SSUMS	0		1	0	
TE	0		X	1	X
RE	0		X	X	1
P66DDR	0	1	0		
Pin function	P66 input pin $\overline{\text{ExIRQ9}}$ input pin	P66 output pin	$\overline{\text{SCS}}$ I/O pin		

[Legend] X: Don't care.

(5) PB7/EVENT15/RM_RX-ER, PB6/EVENT14/RM_CRS-DV, PB5/EVENT13/RM_REF-CLK
PB4/EVENT12/RM_TX-EN (On page 253, H8S/2472 Group)

[Before correction]

- PB7/EVENT15/RM_RX-ER, PB6/EVENT14/RM_CRS-DV, PB5/EVENT13/RM_REF-CLK PB4/EVENT12/RM_TX-EN

EtherC, E-DMAC	Either of them is stopped			Both of then are stopped
PBnDDR	0		1	X
Event counter	Disabled	Enabled	X	X
Pin function	PBn input pin	EVENTm input pin	PBn output pin	RM_xxxx EtherC I/O pin

[After correction]

- PB7/EVENT15/RM_RX-ER, PB6/EVENT14/RM_CRS-DV, PB5/EVENT13/RM_REF-CLK PB4/EVENT12/RM_TX-EN

EtherC, E-DMAC	Either of them is stopped			Both modules are released from module stop mode
PBnDDR	0		1	X
Event counter*	Disabled	Enabled	X	X
Pin function	PBn input pin	EVENTm input pin	PBn output pin	RM_xxxx EtherC I/O pin

(6) PB3/EVENT11/DB3/RM_RXD1, PB2/EVENT10/DB2/RM_RXD0,
PB1/EVENT9/DB1/RM_TXD1, PB0/EVENT8/DB0/RM_TXD0 (On page 253, H8S/2472 Group)

[Before correction]

• PB3/EVENT11/DB3/RM_RXD1, PB2/EVENT10/DB2/RM_RXD0,
PB1/EVENT9/DB1/RM_TXD1, PB0/EVENT8/DB0/RM_TXD0

EtherC, E-DMAC	Either of them is stopped				Both of then are stopped
PBnDDR	0			1	X
Event counter	Disabled		Enabled	X	X
PBnNCE	0	1	X	X	X
Pin function	PBn input pin		EVENTm input pin	PBn output pin	RM_xxxx EtherC I/O pin

[After correction]

• PB3/EVENT11/DB3/RM_RXD1, PB2/EVENT10/DB2/RM_RXD0,
PB1/EVENT9/DB1/RM_TXD1, PB0/EVENT8/DB0/RM_TXD0

EtherC, E-DMAC	Either of them is stopped				Both modules are released from module stop mode
PBnDDR	0			1	X
Event counter	Disabled		Enabled	X	X
PBnNCE	0	1	X	X	X
Pin function	PBn input pin		EVENTm input pin	PBn output pin	RM_xxxx EtherC I/O pin

(7) PF1/RS9/MDC, PF0/RS8/MDIO (On page 271, H8S/2472 Group)

[Before correction]

• PF1/RS9/MDC, PF0/RS8/MDIO

EtherC, E-DMAC	Ether of them is stopped		Both of them are stopped
PFnDDR	0	1	X
Pin function	PFn input pin	PFn output pin	MDC output pin/ MDIO input/output pin

[Legend] n = 1, 0

X: Don't care.

[After correction]

• PF1/RS9/MDC

EtherC, E-DMAC	Either of them is stopped		Both modules are released from module stop mode
PF1DDR	0	1	X
Pin function	PF1 input pin	PF1 output pin	MDC output pin

[Legend] X: Don't care.

• PF0/RS8/MDIO

To use as the MDIO input/out pin, clear the PF0DDR bit to 0.

EtherC, E-DMAC	Either of them is stopped		Both modules are released from module stop mode
PF0DDR	0	1	0
Pin function	PF0 input pin	PF0 output pin	MDIO input/output pin

(8) PB7/EVENT15/RM_RX-ER, PB6/EVENT14/RM_CRS-DV, PB5/EVENT13/RM_REF-CLK
PB4/EVENT12/RM_TX-EN (On page 336, H8S/2463 Group and H8S/2462 Group)

[Before correction]

• PB7/EVENT15/RM_RX-ER, PB6/EVENT14/RM_CRS-DV, PB5/EVENT13/RM_REF-CLK
PB4/EVENT12/RM_TX-EN

EtherC, E-DMAC	Either of them is stopped			Both of them are stopped
PBnDDR	0		1	X
Event counter	Disabled	Enabled	X	X
Pin function	PBn input pin	EVENTm input pin	PBn output pin	RM_xxxx EtherC I/O pin

[After correction]

• PB7/EVENT15/RM_RX-ER, PB6/EVENT14/RM_CRS-DV, PB5/EVENT13/RM_REF-CLK
PB4/EVENT12/RM_TX-EN

EtherC, E-DMAC	Either of them is stopped			Both modules are released from module stop mode
PBnDDR	0		1	X
Event counter*	Disabled	Enabled	X	X
Pin function	PBn input pin	EVENTm input pin	PBn output pin	RM_xxxx EtherC I/O pin

(9) PB3/EVENT11/DB3/RM_RXD1, PB2/EVENT10/DB2/RM_RXD0, PB1/EVENT9/DB1/RM_TXD1,
PB0/EVENT8/DB0/RM_TXD0 (On page 337, H8S/2463 Group and H8S/2462 Group)

[Before correction]

• PB3/EVENT11/DB3/RM_RXD1, PB2/EVENT10/DB2/RM_RXD0, PB1/EVENT9/DB1/RM_TXD1,
PB0/EVENT8/DB0/RM_TXD0

EtherC, E-DMAC	Either of them is stopped				Both of them are stopped
PBnDDR	0			1	X
Event counter	Disabled		Enabled	X	X
PBnNCE	0	1	X	X	X
Pin function	PBn input	DBn input	EVENTm input	PBn output pin	RM_xxxx EtherC I/O pin

[After correction]

• PB3/EVENT11/DB3/RM_RXD1, PB2/EVENT10/DB2/RM_RXD0, PB1/EVENT9/DB1/RM_TXD1,
PB0/EVENT8/DB0/RM_TXD0

EtherC, E-DMAC	Either of them is stopped				Module stop mode is cleared in both the modules
PBnDDR	0			1	X
Event counter	Disabled		Enabled	X	X
PBnNCE	0	1	X	X	X
Pin function	PBn input	DBn input	EVENTm input	PBn output pin	RM_xxxx EtherC I/O pin

(10) PF1/RS9/MDC (On page 355, H8S/2463 Group and H8S/2462 Group)

• PF1/RS9/MDC

The pin function is switched as shown below according to the combination of the module stop state in the EtherC and e-DMAC and the PF1DDR bit.

[Before correction]

EtherC, E-DMAC	Either of them is stopped		Both of them are stopped
PF1DDR	0	1	X
Pin function	PF1 input pin	PF1 output pin	MDC output pin

[Legend] X: Don't care.

[After correction]

• PF1/RS9/MDC

The pin function is switched as shown below according to the combination of the module stop state in the EtherC and E-DMAC and the PF1DDR bit.

EtherC, E-DMAC	Either of them is stopped		Module stop mode is cleared in both the modules
PF1DDR	0	1	X
Pin function	PF1 input pin	PF1 output pin	MDC output pin

[Legend] X: Don't care.

(11) PF0/RS8/MDIO (On page 355, H8S/2463 Group and H8S/2462 Group)

[Before correction]

(7) PF0/RS0/MDIO

The pin function is switched as shown below according to the combination of the module stop state in the EtherC and e-DMAC and the PF0DDR bit.

EtherC, E-DMAC	Either of them is stopped		Both of them are stopped
PF0DDR	0	1	X
Pin function	PF0 input pin	PF0 output pin	MDIO input/output pin

[Legend] X: Don't care.

[After correction]

(7) PF0/RS8/MDIO

The pin function is switched as shown below according to the combination of the module stop state in the EtherC and E-DMAC and the PF0DDR bit.

To use as the MDIO input/out pin, clear the PF0DDR bit to 0.

EtherC, E-DMAC	Either of them is stopped		Module stop mode is cleared in both the modules
PF0DDR	0	1	0
Pin function	PF0 input pin	PF0 output pin	MDIO input/output pin

[Legend] X: Don't care.