To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Aug.19.2008

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A670A/E	Rev.	1.00
Title	The correction of the SH7730 hardware manual		Information Category	Technical Notification		
Applicable Product	SH7730 Group R8A77301	Lot No. All	Reference Document	SH7730 Group Hardware Manual (REJ09B0359-0100 Rev. 1.00)		

In the SH7730 Group Hardware Manual, we would like to inform you of the correction of the writing error below.

Section 1 Overview

P. 6 Table 1.1 Feature of This LSI Clock pulse generator (CPG)

#Before#

CPU clock (Iϕ): Maximum 266 MHz

SH (SuperHyway) clock (Sϕ): Maximum 133 MHz

Bus clock (Bϕ): Maximum 66 MHz

Peripheral clock (Pϕ): Maximum 33 MHz

#After#

CPU clock (Iϕ): Maximum 266.67 MHz

SH (SuperHyway) clock (Sϕ): Maximum 133.34 MHz

Bus clock (Bϕ): Maximum 66.67 MHz

Peripheral clock (Pϕ): Maximum 33.34 MHz

Section 10 Interrupt Controller (INTC)

P. 250 10.3.1 Interrupt Control Register 0 (ICR0)

#Before#

Bit	Bit Name	Initial Value	R/W	Description
6	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.

#After#

Bit	Bit Name	Initial Value	R/W	Description
6	IRLM2	0	R/W	IRL Pin Mode2 This bit sets the IRQ7 to IRQ4 interrupts. 0: Initial value 1: The IRQ7 to IRQ4 interrupts are in use When the IRQ7 to IRQ4 interrupts are in use, set 1 to this bit. When this bit is set to 0, IRQ7 to IRQ4 pin functions should not be selected by setting the Pin Function Controller (PFC). If not, an interrupt that is not intended may occur. These 4 pins, IRQ7 to IRQ4, cannot be used as pins for 15-level encoded interrupts.

P. 255 10.3.6 Interrupt Mask Register 00 (INTMSK00)

Add this description below in the explanation of this register:

When IRL interrupts in IRL3 to IRL0 pins are in use by setting ICR0.IRLM to 0, the interrupt requests from IRQ3 to IRQ0 pins should be masked by setting IRQ3 to IRQ0 bits of this register to 1.

Section 11 Bus State Controller (BSC)

P. 290 11.4.1 Common Control Register (CMNCR)

#Before#

Bit	Bit Name	Initial Value	R/W	Description
23 to 15	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

#After#

Bit	Bit Name	Initial Value	R/W	Description
23 to 17	-	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DMSTP	0	R/W	Low Power Consumption Mode Low power consumption mode is set by this bit. When this bit is 0, the power consumption is lowered by the transition to the mode to stop the external bus mastership control (BREQ/BACK) circuit. When this bit is 1, the external bus mastership control (BREQ/BACK) is available. 0: BSC is in low power consumption mode 1: BSC is out of low power consumption mode
15	-	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Section 14 Reset and Power-Down Modes

P. 473 14.3.2 Module Stop Register (MSTPCR0) bit 1, 0

#Before#

The write value should always be 1 although the initial value is all 0.

#After#

This bit is always read as 0. The write value should always be 0.

Section 33 Electrical Characteristics

P. 1061 Table 33.6 Maximum Operating Frequencies CPU clock (Iϕ)

#Before#

266MHz

#After#

266.67MHz