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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A0075A/E	Rev.	1.00
Title	Correction for “Serial Peripheral Interface (SPI)” in Synergy S124/S128/S1JA User’s Manual		Information Category	Technical Notification		
Applicable Product	Synergy S124/S128/S1JA Group	Lot No. All lots	Reference Document	-Renesas S124 Group User’s Manual: Hardware R01UM0003EU0130 Rev.1.30 -Renesas S128 Group User’s Manual: Hardware R01UM0005EU0110 Rev.1.10 -Renesas S1JA Group User’s Manual: Hardware R01UM0008EU0140 Rev.1.40		

The errata in the Chapter of “Serial Peripheral Interface (SPI)” are corrected.

The details are shown from the next page.

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Group: S124

Chapter 30. Serial Peripheral Interface (SPI)

Before）

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Table 28.1 SPI specifications (1 of 2)

Parameter	Description
Number of channels	Two channels
SPI transfer functions	• MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals enable serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • Switching of RSPCK polarity • Switching of RSPCK phase.
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB, programmable from divide-by-2 to divide-by-4,096 • In slave mode, the minimum PCLKB clock divided by 4 can be input as RSPCK (maximum RSPCK frequency is PCLKB divided by 4). Width at high level: 2 PCLKB cycles; width at low level: 2 PCLKB cycles

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Table 28.4 Relationship between SPI modes and SPCR settings and description of each mode (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
SSL polarity change function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLKB/4	Up to PCLKB/2	Up to PCLKB/2	Up to PCLKB/4	Up to PCLKB/2

After）

The “Bit rate” in slave mode is corrected as below in Table 28.1.

Table 28.1 SPI specifications (1 of 2)

Parameter	Description
Number of channels	Two channels
SPI transfer functions	• MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals enable serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • Switching of RSPCK polarity • Switching of RSPCK phase.
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB, programmable from divide-by-2 to divide-by-4,096 • In slave mode, the minimum PCLKB clock divided by 6 can be input as RSPCK (maximum RSPCK frequency is PCLKB divided by 6). Width at high level: 3 PCLKB cycles; width at low level: 3 PCLKB cycles

The “Max transfer rate” in slave mode is corrected as below in Table 28.4.

Table 28.4 Relationship between SPI modes and SPCR settings and description of each mode (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
SSL polarity change function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLKB/6	Up to PCLKB/2	Up to PCLKB/2	Up to PCLKB/6	Up to PCLKB/2

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Group: S128

Chapter 30. Serial Peripheral Interface (SPI)

Before）

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Table 31.1 SPI specifications (1 of 2)

Parameter	Description
Number of channels	Two channels
SPI transfer functions	• MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals enable serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • Switching of RSPCK polarity • Switching of RSPCK phase.
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB, programmable from divide-by-2 to divide-by-4,096 • In slave mode, the minimum PCLKB clock divided by 4 can be input as RSPCK (maximum RSPCK frequency is PCLKB divided by 4). Width at high level: 2 PCLKB cycles; width at low level: 2 PCLKB cycles

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Table 31.4 Relationship between SPI modes and SPCR settings and description of each mode (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
SSL polarity change function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLKB/4	Up to PCLKB/2	Up to PCLKB/2	Up to PCLKB/4	Up to PCLKB/2

After）

The “Bit rate” in slave mode is corrected as below in Table 31.1.

Table 31.1 SPI specifications (1 of 2)

Parameter	Description
Number of channels	Two channels
SPI transfer functions	• MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals enable serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • Switching of RSPCK polarity • Switching of RSPCK phase.
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB, programmable from divide-by-2 to divide-by-4,096 • In slave mode, the minimum PCLKB clock divided by 6 can be input as RSPCK (maximum RSPCK frequency is PCLKB divided by 6). Width at high level: 3 PCLKB cycles; width at low level: 3 PCLKB cycles

The “Max transfer rate” in slave mode is corrected as below in Table 31.4.

Table 31.4 Relationship between SPI modes and SPCR settings and description of each mode (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
SSL polarity change function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLKB/6	Up to PCLKB/2	Up to PCLKB/2	Up to PCLKB/6	Up to PCLKB/2

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Group: S1JA

Chapter 30. Serial Peripheral Interface (SPI)

Before）

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Table 30.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • Switching of RSPCK polarity • Switching of RSPCK phase.
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKB clock divided by 4 can be input as RSPCK (the maximum RSPCK frequency is that of PCLKB divided by 4) Width at high level: 2 PCLKB cycles Width at low level: 2 PCLKB cycles.

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Table 30.4 Relationship between SPCR settings and SPI modes (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
SSLn0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 signals	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLKB/4	Up to PCLKB/2	Up to PCLKB/2	Up to PCLKB/4	Up to PCLKB/2

After）

The “Bit rate” in slave mode is corrected as below in Table 30.1.

Table 30.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • Switching of RSPCK polarity • Switching of RSPCK phase.
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKB clock divided by 6 can be input as RSPCK (the maximum RSPCK frequency is that of PCLKB divided by 6) Width at high level: 3 PCLKB cycles Width at low level: 3 PCLKB cycles.

The “Max transfer rate” in slave mode is corrected as below in Table 30.4.

Table 30.4 Relationship between SPCR settings and SPI modes (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
SSLn0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 signals	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Transfer rate	Up to PCLKB/6	Up to PCLKB/2	Up to PCLKB/2	Up to PCLKB/6	Up to PCLKB/2

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