

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0131A/E	Rev.	1.00
Title	Correction of LCD Electrical characteristics description		Information Category	Technical Notification		
Applicable Product	RA2A2 Group	Lot No.	Reference Document	RA2A2 Group User's Manual: Hardware Rev.1.20 (R01UH1005EJ0120)		
		All				

Correction of 41.13.3 Internal Voltage Boosting Method (VL2 Reference) description in the user's manual as below.

(Before)

Table 41.77 Internal voltage boosting method LCD characteristics (3) (2 of 2)

Conditions: VCC = AVCC = VL2 (Max) + 0.1 to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions	
LCD output voltage variation range	VL2	C1 to C4*1 = 0.47 μ F	VLCD*2 = 0x84	1.94	2.02	2.11	V	—
			VLCD = 0x85	2.00	2.09	2.18	V	—
			VLCD = 0x86	2.07	2.16	2.25	V	—
			VLCD = 0x87	2.13	2.22	2.32	V	—
			VLCD = 0x88	2.19	2.29	2.39	V	—
			VLCD = 0x89	2.26	2.36	2.46	V	—
			VLCD = 0x8A	2.32	2.42	2.53	V	—
			VLCD = 0x8B	2.39	2.49	2.59	V	—
			VLCD = 0x8C	2.45	2.56	2.66	V	—
			VLCD = 0x8D	2.51	2.62	2.73	V	—
			VLCD = 0x8E	2.58	2.69	2.80	V	—
			VLCD = 0x8F	2.64	2.76	2.87	V	—
			VLCD = 0x90	2.70	2.82	2.94	V	—
			VLCD = 0x91	2.77	2.89	3.01	V	—
			VLCD = 0x92	2.83	2.96	3.08	V	—
			VLCD = 0x93	2.90	3.02	3.15	V	—
			VLCD = 0x94	2.96	3.09	3.22	V	—
			VLCD = 0x95	3.02	3.15	3.29	V	—
			VLCD = 0x96	3.09	3.22	3.35	V	—
VLCD = 0x97	3.15	3.29	3.42	V	—			
VLCD = 0x98	3.21	3.35	3.49	V	—			
VLCD = 0x99	3.28	3.42	3.56	V	—			
VLCD = 0x9A	3.34	3.49	3.63	V	—			
Two-thirds output voltage	VL4*5	C1 to C4*1 = 0.47 μ F	$\frac{2}{3} \times V_{L2} - 6\%$	$\frac{2}{3} \times V_{L2}$	$\frac{2}{3} \times V_{L2} + 6\%$	V	—	
Reference voltage setup time*3	tVL2S	—	10	—	—	ms	Figure 41.51	
Voltage boost wait time*4	tVLWT	—	500	—	—	ms	Figure 41.51	

(After)

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VLCD = 0x99	3.28	3.42	3.56	V	—			
VLCD = 0x9A	3.34	3.49	3.63	V	—			
3/2 output voltage	VL4*5	C1 to C4*1 = 0.47 μF	3/2 × VL2 - 6%	3/2 × VL2	3/2 × VL2 + 6%	V	—	
Reference voltage setup time*3	tVL2S	—	10	—	—	ms	Figure 41.51	
Voltage boost wait time*4	tVLWT	—	500	—	—	ms	Figure 41.51	