Date: May 17, 2024

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0111A/E	Rev.	1.00
Title	Correction initial and write value of LPOPT register in Low Power Modes.		Information Category	Technical Notification		
Applicable Product	RA2L1 Group RA2E1 Group RA2E2 Group RA2E3 Group RA2A2 Group	Lot No. All lots	Reference Document	-Renesas RA2L1 Group User's Manual: Hardware R01UH0853EJ0140 Rev.1.40 -Renesas RA2E1 Group User's Manual: Hardware R01UH0852EJ0140 Rev.1.40 -Renesas RA2E2 Group User's Manual: Hardware R01UH0919EJ0130 Rev.1.30 -Renesas RA2E3 Group User's Manual: Hardware R01UH0992EJ0110 Rev.1.10 -Renesas RA2A2 Group User's Manual: Hardware R01UH1005EJ0110 Rev.1.10		

Correction of errata regarding initial and write value of LPOPT register bit 6 in Low Power Modes.

The details are shown from the next page.

Group:RA2L1

10. Low Power Modes

Correct errata initial and write value for LPOPT register bit 6 in 10.2.16 LPOPT : Lower Power Operation Control Register.

Before

10.2.16 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	LPOPTEN	Lower Power Operation Enable 0: All lower power counter measure disable 1: All lower power counter measure enable	R/W

After

10.2.16 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	—	This bit is read as 1. The write value should be 1.	R/W
7	LPOPTEN	Lower Power Operation Enable 0: All lower power counter measure disable 1: All lower power counter measure enable	R/W

Appendix 3. I/O Registers

Correct errata Reset value for LPOPT register in Table 3.4 Register description (2 of 15).

Before

Table 3.4 Register description (2 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
BUS	—	—	—	BUSMCNTSYS	Master Bus Control Register SYS	0x1008	16	R/W	0x0000	0xFFFF
BUS	—	—	—	BUSMCNTDMA	Master Bus Control Register DMA	0x100C	16	R/W	0x0000	0xFFFF
BUS	—	—	—	BUS3ERRADD	Bus Error Address Register 3	0x1820	32	R	0x00000000	0x00000000
BUS	—	—	—	BUS3ERRSTAT	BUS Error Status Register 3	0x1824	8	R	0x00	0xFE
BUS	—	—	—	BUS4ERRADD	Bus Error Address Register 4	0x1830	32	R	0x00000000	0x00000000
BUS	—	—	—	BUS4ERRSTAT	BUS Error Status Register 4	0x1834	8	R	0x00	0xFE
DTC	—	—	—	DTCCR	DTC Control Register	0x00	8	R/W	0x08	0xFF
DTC	—	—	—	DTCVBR	DTC Vector Base Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
DTC	—	—	—	DTCST	DTC Module Start Register	0x0C	8	R/W	0x00	0xFF
DTC	—	—	—	DTCSTS	DTC Status Register	0x0E	16	R	0x0000	0xFFFF
ICU	8	0x1	0-7	IRQCR%s	IRQ Control Register	0x000	8	R/W	0x00	0xFF
ICU	—	—	—	NMICR	NMI Pin Interrupt Control Register	0x100	8	R/W	0x00	0xFF
ICU	—	—	—	NMIER	Non-Maskable Interrupt Enable Register	0x120	16	R/W	0x0000	0xFFFF
ICU	—	—	—	NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	R/W	0x0000	0xFFFF
ICU	—	—	—	NMISR	Non-Maskable Interrupt Status Register	0x140	16	R	0x0000	0xFFFF
ICU	—	—	—	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	—	—	—	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	—	—	—	SELSR0	SYS Event Link Setting Register	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
DBG	—	—	—	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
DBG	—	—	—	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	—	—	—	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	—	—	—	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	—	—	—	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	—	—	—	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	—	—	—	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	—	—	—	MOSCCR	Main Clock Oscillator Control Register	0x032	8	R/W	0x01	0xFF
SYSC	—	—	—	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	—	—	—	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	—	—	—	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	—	—	—	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	—	—	—	OSTDCR	Oscillation Stop Detection Control Register	0x040	8	R/W	0x00	0xFF
SYSC	—	—	—	OSTDSR	Oscillation Stop Detection Status Register	0x041	8	R/W	0x00	0xFF
SYSC	—	—	—	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x00	0xFF

After

Table 3.4 Register description (2 of 15)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
BUS	—	—	—	BUSMCNTSYS	Master Bus Control Register SYS	0x1008	16	R/W	0x0000	0xFFFF
BUS	—	—	—	BUSMCNTDMA	Master Bus Control Register DMA	0x100C	16	R/W	0x0000	0xFFFF
BUS	—	—	—	BUS3ERRADD	Bus Error Address Register 3	0x1820	32	R	0x00000000	0x00000000
BUS	—	—	—	BUS3ERRSTAT	BUS Error Status Register 3	0x1824	8	R	0x00	0xFE
BUS	—	—	—	BUS4ERRADD	Bus Error Address Register 4	0x1830	32	R	0x00000000	0x00000000
BUS	—	—	—	BUS4ERRSTAT	BUS Error Status Register 4	0x1834	8	R	0x00	0xFE
DTC	—	—	—	DTCCR	DTC Control Register	0x00	8	R/W	0x08	0xFF
DTC	—	—	—	DTCVBR	DTC Vector Base Register	0x04	32	R/W	0x00000000	0xFFFFFFFF
DTC	—	—	—	DTCST	DTC Module Start Register	0x0C	8	R/W	0x00	0xFF
DTC	—	—	—	DTCSTS	DTC Status Register	0x0E	16	R	0x0000	0xFFFF
ICU	8	0x1	0-7	IRQCR%s	IRQ Control Register	0x000	8	R/W	0x00	0xFF
ICU	—	—	—	NMICR	NMI Pin Interrupt Control Register	0x100	8	R/W	0x00	0xFF
ICU	—	—	—	NMIER	Non-Maskable Interrupt Enable Register	0x120	16	R/W	0x0000	0xFFFF
ICU	—	—	—	NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	R/W	0x0000	0xFFFF
ICU	—	—	—	NMISR	Non-Maskable Interrupt Status Register	0x140	16	R	0x0000	0xFFFF
ICU	—	—	—	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	—	—	—	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	—	—	—	SELSR0	SYS Event Link Setting Register	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
DBG	—	—	—	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
DBG	—	—	—	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	—	—	—	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	—	—	—	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	—	—	—	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	—	—	—	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	—	—	—	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	—	—	—	MOSCCR	Main Clock Oscillator Control Register	0x032	8	R/W	0x01	0xFF
SYSC	—	—	—	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	—	—	—	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	—	—	—	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	—	—	—	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	—	—	—	OSTDCR	Oscillation Stop Detection Control Register	0x040	8	R/W	0x00	0xFF
SYSC	—	—	—	OSTDSR	Oscillation Stop Detection Status Register	0x041	8	R/W	0x00	0xFF
SYSC	—	—	—	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x40	0xFF

Group:RA2E1

10. Low Power Modes

Correct errata initial and write value for LPOPT register bit 6 in 10.2.14 LPOPT : Lower Power Operation Control Register.

Before

10.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W

After

10.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	—	This bit is read as 1. The write value should be 1.	R/W

Appendix 3. I/O Registers

Correct errata Reset value for LPOPT register in Table 3.4 Register description (2 of 13).

Before

Table 3.4 Register description (2 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ICU	-	-	-	NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMISR	Non-Maskable Interrupt Status Register	0x140	16	R	0x0000	0xFFFF
ICU	-	-	-	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	-	-	-	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	-	-	-	SELSR0	SYS Event Link Setting Register	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	-	-	-	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	-	-	-	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	-	-	-	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	-	-	-	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	MOSCCR	Main Clock Oscillator Control Register	0x032	8	R/W	0x01	0xFF
SYSC	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDCR	Oscillation Stop Detection Control Register	0x040	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDSR	Oscillation Stop Detection Status Register	0x041	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x00	0xFF

After

Table 3.4 Register description (2 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ICU	-	-	-	NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	R/W	0x0000	0xFFFF
ICU	-	-	-	NMISR	Non-Maskable Interrupt Status Register	0x140	16	R	0x0000	0xFFFF
ICU	-	-	-	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	-	-	-	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	-	-	-	SELSR0	SYS Event Link Setting Register	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	-	-	-	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	-	-	-	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	-	-	-	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	-	-	-	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	MOSCCR	Main Clock Oscillator Control Register	0x032	8	R/W	0x01	0xFF
SYSC	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDCR	Oscillation Stop Detection Control Register	0x040	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDSR	Oscillation Stop Detection Status Register	0x041	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x40	0xFF

Group:RA2E2

10. Low Power Modes

Correct errata initial and write value for LPOPT register bit 6 in 10.2.14 LPOPT : Lower Power Operation Control Register.

Before

10.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	LPOPTEN	Lower Power Operation Enable 0: All lower power counter measure disable 1: All lower power counter measure enable	R/W

After

10.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	—	This bit is read as 1. The write value should be 1.	R/W
7	LPOPTEN	Lower Power Operation Enable 0: All lower power counter measure disable 1: All lower power counter measure enable	R/W

Appendix 3. I/O Registers

Correct errata Reset value for LPOPT register in Table 3.4 Register description (3 of 11).

Before

Table 3.4 Register description (3 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SYSC	-	-	-	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x00	0xFF

After

Table 3.4 Register description (3 of 11)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
SYSC	-	-	-	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x40	0xFF

Group:RA2E3

10. Low Power Modes

Correct errata initial and write value for LPOPT register bit 6 in 10.2.14 LPOPT : Lower Power Operation Control Register.

Before

10.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	LPOPTEN	Lower Power Operation Enable 0: All lower power counter measure disable 1: All lower power counter measure enable	R/W

After

10.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	—	This bit is read as 1. The write value should be 1.	R/W
7	LPOPTEN	Lower Power Operation Enable 0: All lower power counter measure disable 1: All lower power counter measure enable	R/W

Appendix 3. I/O Registers

Correct errata Reset value for LPOPT register in Table 3.4 Register description (3 of 13).

Before

Table 3.4 Register description (3 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ICU	-	-	-	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	-	-	-	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	-	-	-	SELSR0	SYS Event Link Setting Register	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	-	-	-	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	-	-	-	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	-	-	-	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	-	-	-	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	MOSCCR	Main Clock Oscillator Control Register	0x032	8	R/W	0x01	0xFF
SYSC	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDCR	Oscillation Stop Detection Control Register	0x040	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDSR	Oscillation Stop Detection Status Register	0x041	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x00	0xFF

After

Table 3.4 Register description (3 of 13)

Peripheral name	Dim	Dim inc.	Dim index	Register name	Description	Address offset	Size	R/W	Reset value	Reset mask
ICU	-	-	-	WUPEN	Wake Up Interrupt Enable Register	0x1A0	32	R/W	0x00000000	0xFFFFFFFF
ICU	-	-	-	IELEN	ICU event Enable Register	0x1C0	8	R/W	0x00	0xFF
ICU	-	-	-	SELSR0	SYS Event Link Setting Register	0x200	16	R/W	0x0000	0xFFFF
ICU	32	0x4	0-31	IELSR%s	ICU Event Link Setting Register %s	0x300	32	R/W	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTR	Debug Status Register	0x00	32	R	0x00000000	0xFFFFFFFF
CPU_DBG	-	-	-	DBGSTOPCR	Debug Stop Control Register	0x10	32	R/W	0x00000003	0xFFFFFFFF
SYSC	-	-	-	SBYCR	Standby Control Register	0x00C	16	R/W	0x0000	0xFFFF
SYSC	-	-	-	MSTPCRA	Module Stop Control Register A	0x01C	32	R/W	0xFFBFFFFF	0xFFFFFFFF
SYSC	-	-	-	SCKDIVCR	System Clock Division Control Register	0x020	32	R/W	0x04000404	0xFFFFFFFF
SYSC	-	-	-	SCKSCR	System Clock Source Control Register	0x026	8	R/W	0x01	0xFF
SYSC	-	-	-	MEMWAIT	Memory Wait Cycle Control Register for Code Flash	0x031	8	R/W	0x00	0xFF
SYSC	-	-	-	MOSCCR	Main Clock Oscillator Control Register	0x032	8	R/W	0x01	0xFF
SYSC	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	R/W	0x00	0xFE
SYSC	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	R/W	0x00	0xFF
SYSC	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	R	0x00	0xFE
SYSC	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDCR	Oscillation Stop Detection Control Register	0x040	8	R/W	0x00	0xFF
SYSC	-	-	-	OSTDSR	Oscillation Stop Detection Status Register	0x041	8	R/W	0x00	0xFF
SYSC	-	-	-	LPOPT	Lower Power Operation Control Register	0x04C	8	R/W	0x40	0xFF

Group:RA2A2

10. Low Power Modes

Correct errata initial and write value for LPOPT register bit 6 in 11.2.14 LPOPT : Lower Power Operation Control Register.

Before

11.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	LPOPTEN	Lower Power Operation Enable 0: All lower power counter measure disable 1: All lower power counter measure enable	R/W

After

11.2.14 LPOPT : Lower Power Operation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x04C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPOPTEN	—	—	—	BPFCLKDIS	DCLKDIS[1:0]		MPUDIS
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MPUDIS	MPU Clock Disable Control Stop the MPU operate clock (valid only when LPOPTEN = 1) 0: MPU operates as normal 1: MPU operate clock stops (MPU function disable).	R/W
2:1	DCLKDIS[1:0]	Debug Clock Disable Control 0 0: Debug clock does not stop Others: Debug clock stops (valid only when LPOPT.LPOPTEN = 1)	R/W
3	BPFCLKDIS	BPF Clock Disable Control Stop the Flash register R/W clock (valid only when LPOPT.LPOPTEN = 1) 0: Flash register R/W clock operates as normal 1: Flash register R/W clock stops.	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	—	This bit is read as 1. The write value should be 1.	R/W
7	LPOPTEN	Lower Power Operation Enable 0: All lower power counter measure disable 1: All lower power counter measure enable	R/W