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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-V85-A032A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice V850E2/MN4 Description in the Hardware User's Manual Rev.4.00		Information Category	Technical Notification		
Applicable Product	V850E2/MN4 • μPD70F3510F1-HN6-A • μPD70F3512F1-HN6-A • μPD70F3514F1-HN6-A • μPD70F3515F1-HN6-A	Lot No. All lot	Reference Document	User's Manual : Hardware R01UH0011EJ0400 Rev.4.00		

This document describes misstatements found in the V850E2/MN4 hardware user's manual Rev. 4.00 (R01UH0011EJ0400).

No.1 Location : 37.6.2 External bus interface on page 2375

< Description addition >

The meaning of the symbols indicated on the figures at the timing of SRAM access.

Primary memory controller

Symbol	Meaning
TDW	Number of wait cycles specified by the DWC0 register
TW	Number of wait cycles inserted by P_WAIT
TDH	Number of wait cycles specified by the DHC register
TI	Number of idle states specified by the ICC0, ICC1 register

Secondary memory controller

Symbol	Meaning
TDW	Number of wait cycles specified by the SSMCn.DWn[3:0] bits
TW	Number of wait cycles inserted by S_WAIT
TDH	Number of wait cycles specified by the SSMCn.WWn[3:0] bits
TASW	Number of wait cycles specified by the SSMCn.ACn[3:0] bits
TI	Number of idle states specified by the SSMCn.IWn[3:0] bits

No.2 Location : (10) Secondary memory controller, SRAM write access timing on the page 2390

< Incorrect >

Item	Symbol	MIN.	MAX.	Unit
S_xxWR and S_WR low-level width	tWWRL	(w + wDH + 1)T - 10		ns

< Correct >

Item	Symbol	MIN.	MAX.	Unit
S_xxWR and S_WR low-level width	tWWRL	(w + wD + 1)T - 10		ns

No.3 Location : (10) Secondary memory controller, SRAM write access timing on the page 2390

< Incorrect >

Item	Symbol	MIN.	MAX.	Unit
Data output setup time (to S_xxWR and S_WR↑)	tSODWR	(w + wDH + 1)T - 10		ns

< Correct >

Item	Symbol	MIN.	MAX.	Unit
Data output setup time (to S_xxWR and S_WR↑)	tSODWR	(w + wD + 1)T - 10		ns