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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A033A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/L1C Descriptions in the User's Manual: Hardware Rev. 2.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/L1C Group	Lot No. All lots	Reference Document	RL78/L1C User's Manual: Hardware Rev. 2.00 R01UH0409EJ0200 (Feb. 2014)		

This document describes misstatements found in the RL78/L1C User's Manual: Hardware Rev. 2.00 (R01UH0409EJ0200).

Corrections

Applicable Item	Applicable Page	Contents
3.3.4 Special function registers (SFRs) Table 3 - 8 SFR List	Pages 82 and 83	Incorrect descriptions revised
6.3.3 Timer mode register mn (TMRmn) Figure 6 - 17 Format of Timer mode register mn (TMRmn) (4/4)	Page 248	Incorrect descriptions revised
5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)	Page 186	Incorrect descriptions revised
15.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 14-74. and Figure 14-76.)	Pages 663 and 665	Incorrect descriptions revised
15.6.3 SNOOZE mode function	Page 688	Incorrect descriptions revised
15.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 15-95., Figure 15-96. and Figure 15-96.)	Pages 690, 691 and 693	Incorrect descriptions revised
17.4.5.3 DTC Transfers (D0FIFO and D1FIFO Ports)	Page 895	Incorrect descriptions revised
21.4.3 Multiple interrupt servicing Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing	Page 1029	Incorrect descriptions revised
34.6.1 34.6.1 A/D converter characteristics	Page 1221	Specifications changed
34.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 1234	Content change
35.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 1294	Content change

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0409EJ0200	
1	3.3.4 Special function registers (SFRs) Table 3 - 8 SFR List		Pages 82 and 83	Page 3 and 4
2	6.3.3 Timer mode register mn (TMRmn) Figure 6 - 17 Format of Timer mode register mn (TMRmn) (4/4)		Page 248	Page 5
3	5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)		Page 186	Page 6
4	15.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 14-74. and Figure 14-76.)		Pages 663 and 665	Page 7 and 8
5	15.6.3 SNOOZE mode function		Page 688	Page 9
6	15.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 15-95., Figure 15-96. and Figure 15-96.)		Pages 690, 691 and 693	Page 10 to 12
7	17.4.5.3 DTC Transfers (D0FIFO and D1FIFO Ports)		Page 895	Page 13
8	21.4.3 Multiple interrupt servicing Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing		Page 1029	Page 14
9	34.6.1 34.6.1 A/D converter characteristics		Page 1221	Page 16 and 17
10	34.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		Page 1234	Page 18
11	35.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		Page 1294	Page 20

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/L1C Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A033A/E	Sep. 17, 2014	First edition issued Corrections No.1 to No.11 revised (this document)

1. 3.3.4 Special function registers (SFRs) Table 3 - 7 SFR List (Page 82 and 83)

Incorrect:

Table 3-7. SFR List (1/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
(omitted)								
FFF10H	Serial data register 00	TXD0/ SIO00	SDR00	R/W	–	√	√	0000H
FFF11H		–			–	–		
FFF12H	Serial data register 01	RXD0	SDR01	R/W	–	√	√	0000H
FFF13H		–			–	–		
FFF14H	Serial data register 12	**TXD3**	SDR12	R/W	–	√	√	0000H
FFF15H		**SIO30**			–	–		
FFF16H	Serial data register 13	RXD3	SDR13	R/W	–	√	√	0000H
FFF17H		–			–	–		
(omitted)								

Correct:

Table 3-7. SFR List (1/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
(omitted)								
FFF10H	Serial data register 00	TXD0/ SIO00	SDR00	R/W	–	√	√	0000H
FFF11H		–			–	–		
FFF12H	Serial data register 01	RXD0	SDR01	R/W	–	√	√	0000H
FFF13H		–			–	–		
FFF14H	Serial data register 12	TXD3/ SIO30	SDR12	R/W	–	√	√	0000H
FFF15H					–	–		
FFF16H	Serial data register 13	RXD3	SDR13	R/W	–	√	√	0000H
FFF17H		–			–	–		
(omitted)								

Incorrect:

Table 3-7. SFR List (2/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
(omitted)								
FFF44H	Serial data register 02	TXD1/ SIO10	SDR02	R/W	–	√	√	0000H
FFF45H		–			–	–		
FFF46H	Serial data register 03	RXD1	SDR03	R/W	–	√	√	0000H
FFF47H		–			–	–		
FFF48H	Serial data register 10	**TXD2**	SDR10	R/W	–	√	√	0000H
FFF49H		**SIO20**			–	–		
FFF4AH	Serial data register 11	RXD2	SDR11	R/W	–	√	√	0000H
FFF4BH		–			–	–		
(omitted)								

Correct:

Table 3-7. SFR List (2/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
(omitted)								
FFF44H	Serial data register 02	TXD1/ SIO10	SDR02	R/W	–	√	√	0000H
FFF45H		–			–	–		
FFF46H	Serial data register 03	RXD1	SDR03	R/W	–	√	√	0000H
FFF47H		–			–	–		
FFF48H	Serial data register 10	TXD2/ SIO20	SDR10	R/W	–	√	√	0000H
FFF49H		–			–	–		
FFF4AH	Serial data register 11	RXD2	SDR11	R/W	–	√	√	0000H
FFF4BH		–			–	–		
(omitted)								

2. 6.3.3 Timer mode register mn (TMRmn)
Figure 6 - 17 Format of Timer mode register mn (TMRmn) (4/4)(p.248)

Incorrect:

Operation mode (Value set by the MDmn3 to MDmn1 bits (see the table above))	MDmn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 2 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation Note 3. **At that time, interrupt is also generated.**
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

Correct:

Operation mode (Value set by the MDmn3 to MDmn1 bits (see the table above))	MDmn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 2 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation Note 3. At that time, interrupt is not generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

3. 5.3.9 High-speed on-chip oscillator trimming register (HIOTRM) (Page 186)

Incorrect:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-14. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined [Note] R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
			•			
			•			
			•			
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remark1. The HIOTRM register can be used to adjust the high-speed on-chip oscillator clock to an accuracy within about 0.05%.

Remark2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

Correct:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-14. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined [Note] R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
			•			
			•			
			•			
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register holds a six-bit value used to adjust the high-speed on-chip oscillator with an increment of 1 corresponding to an increase of frequency by about 0.05%.

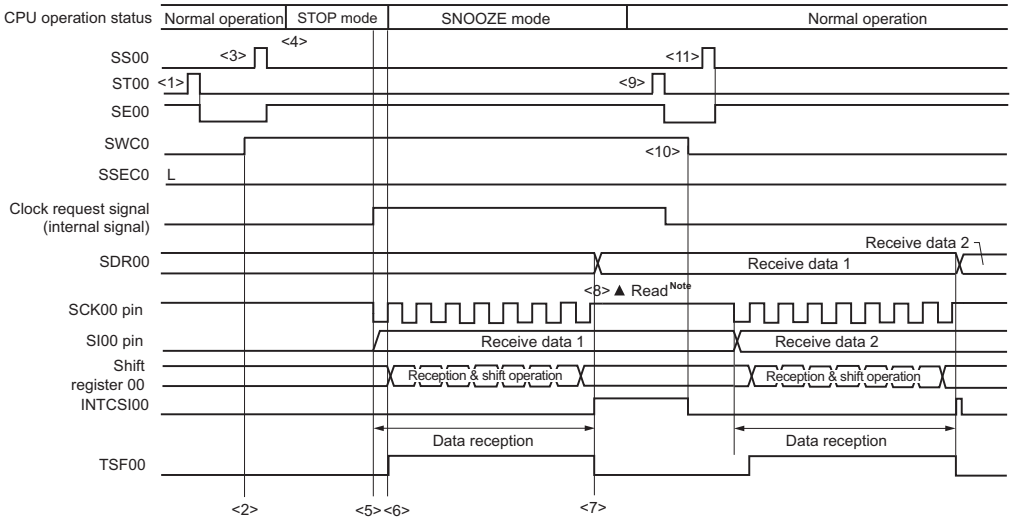
Remark 2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

4. 15.5.7 SNOOZE mode function

Timing Chart of SNOOZE Mode Operation (Figure 15-74. and Figure 15-76.) (Pages 663 and 665)

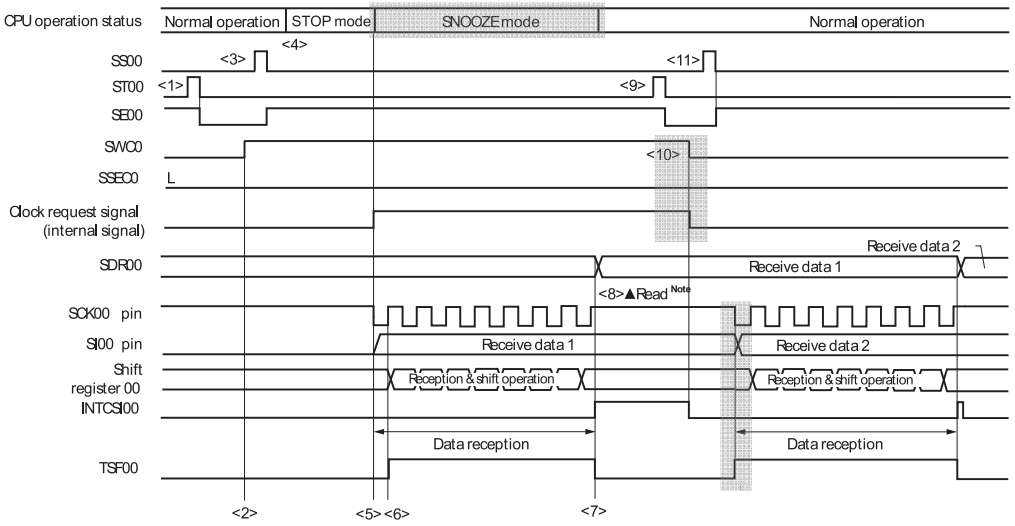
It is correction of "CPU operation status", "Clock request signal (internal signal)" and "TSF00" in this Figure.

Incorrect:
Figure 15-74. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:
Figure 15-74. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)

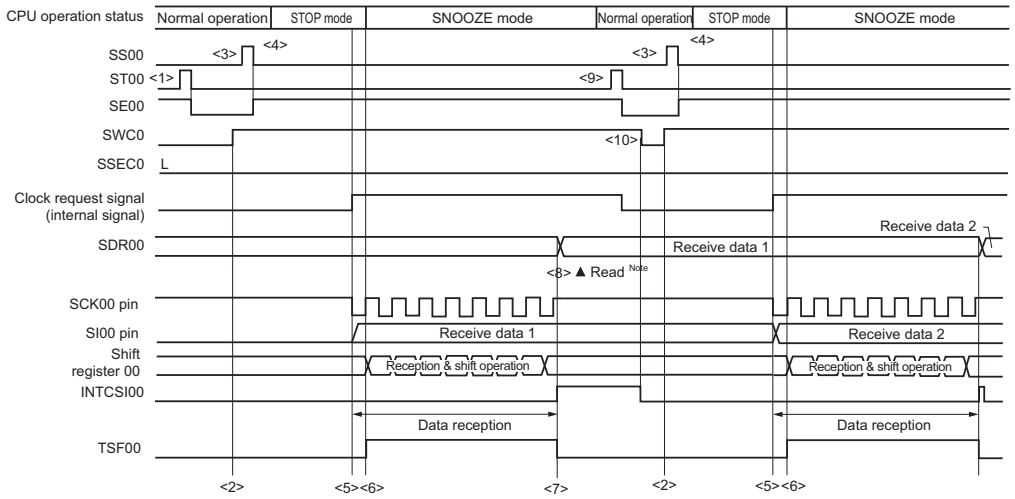


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)” and “INTCSI00” in this Figure.

Incorrect:

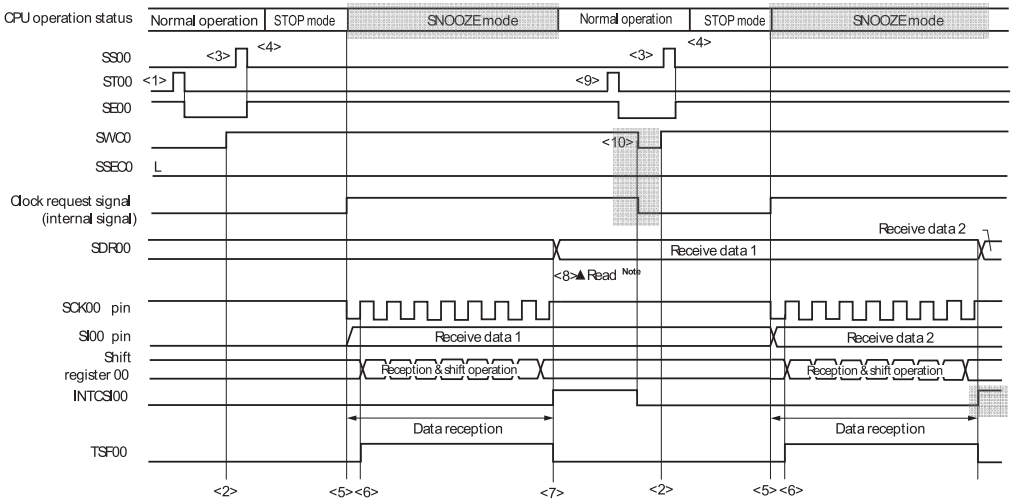
Figure 15-76. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:

Figure 15-76. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

5. 15.6.3 SNOOZE mode function (Page 688)

Incorrect:

15.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

Cautions 4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Correct:

15.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

Cautions 4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

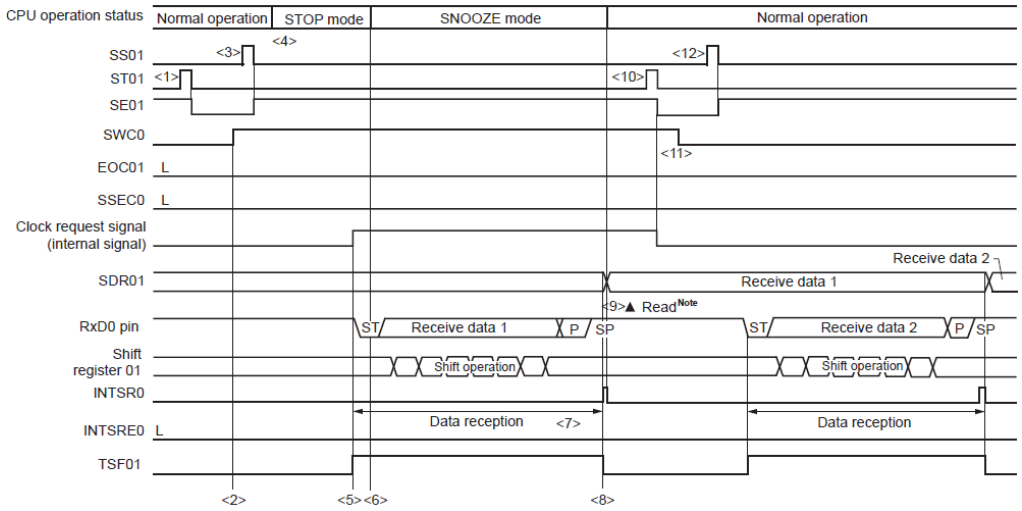
Cautions 5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note, however, that transfer through the UART channel may not start and the CPU may remain in the SNOOZE mode if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may not be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

6. 15.6.3 SNOOZE mode function
Timing Chart of SNOOZE Mode Operation (Figure 15-95, Figure 15-96 and Figure 15-98) (Pages 690, 691 and 693)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

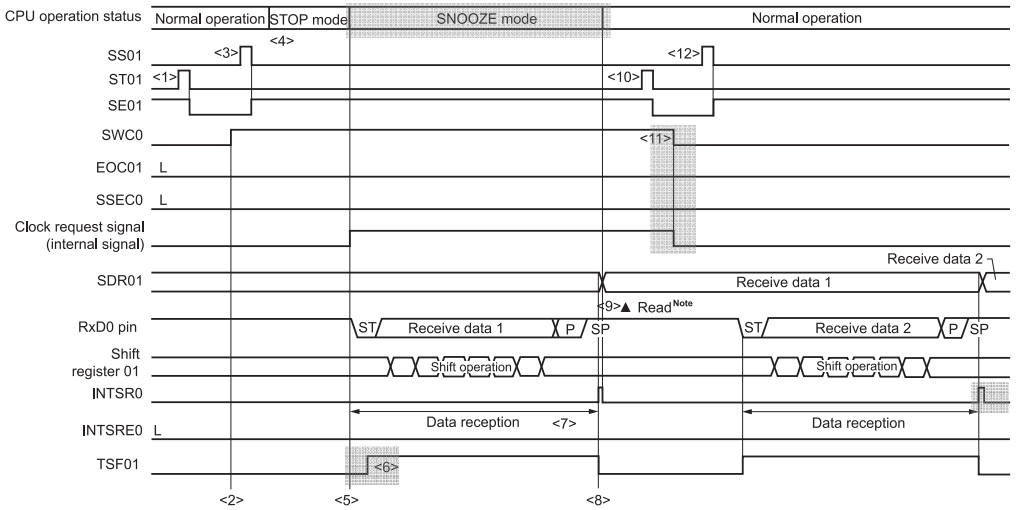
Figure 15-95. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)



(omitted)

Correct:

Figure 15-95. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)

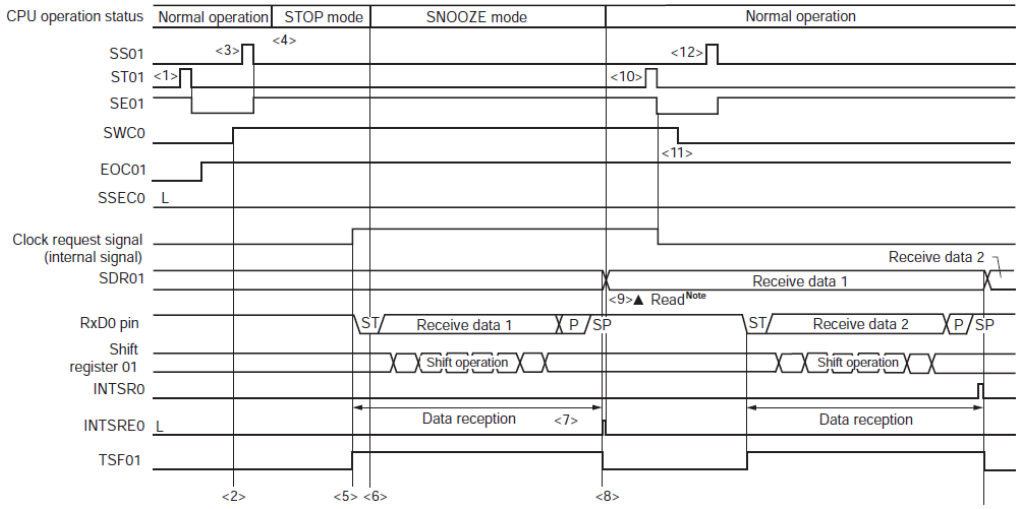


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

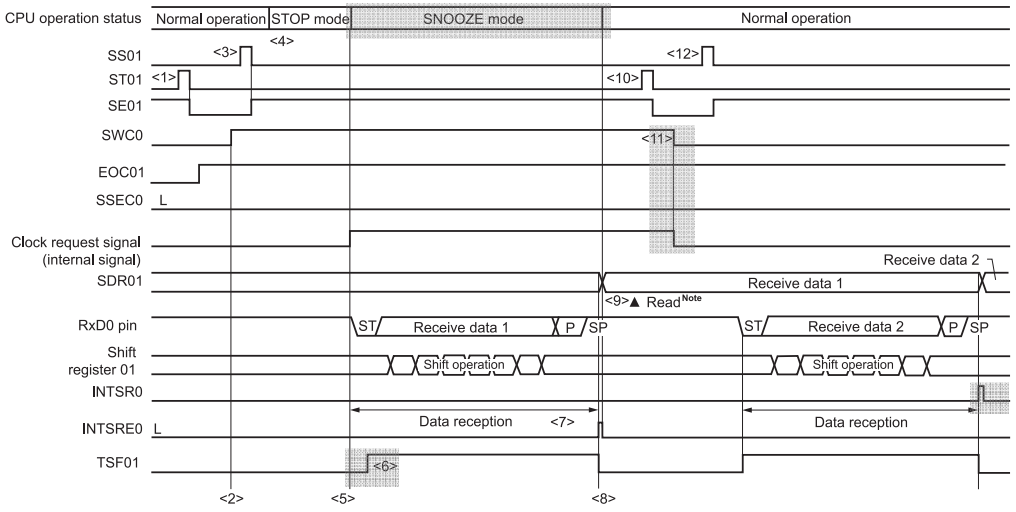
Figure 15-96. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)



(omitted)

Correct:

Figure 15-96. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)

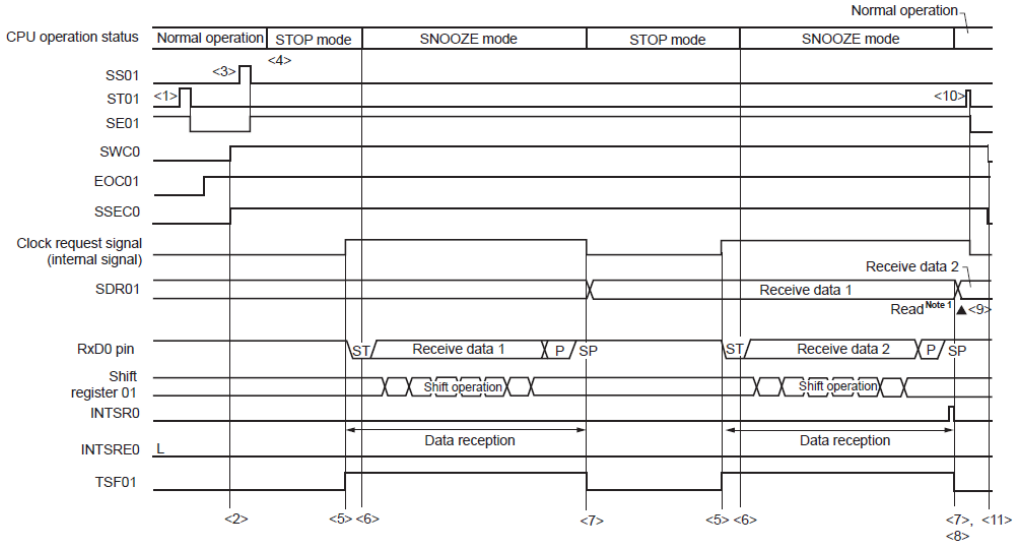


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

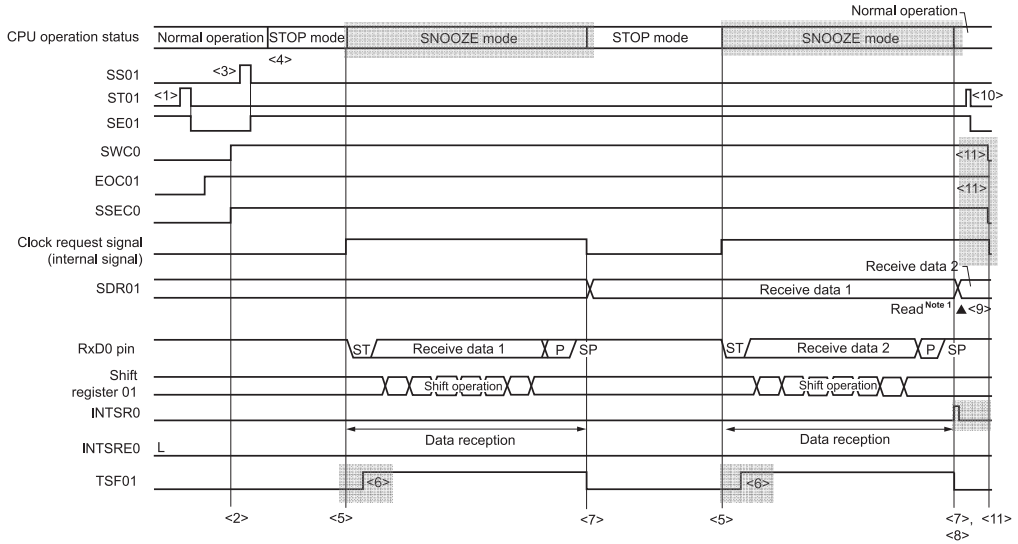
Figure 15-98. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

Correct:

Figure 15-98. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

7. 17.4.5.3 DTC Transfers (D0FIFO and D1FIFO Ports) Table 17 - 22 DTC Settings(p.895)

Old:

Table 17 - 22 DTC Settings

	Cycle steal transfer	Block transfer
DTCCRj	MODE = 0 (Use this setting in normal mode.) SAMOD = FIFO read direction: 0, FIFO write direction: 1 DAMOD = FIFO read direction: 1, FIFO write direction: 0 (Fix the address of the FIFO side.) CHNE = 0 (Disable chain transfers.) Specify the setting according to the setting of Sz = MBW. Setting other bits is invalid due to normal mode	
DTBLSj (DTC block size)	01H (Sz = 0: 1 byte/Sz = 1: 2 bytes)	Sz = 0: Max. Packet Size Sz = 1: Max. Packet Size/2
DTCCTj	Any value (Max. 256 times)	Any value (Max. 256 times)

New:

Table 17 - 22 DTC Settings

	Cycle steal transfer	Block transfer
DTCCRj	MODE = 0 (Use this setting in normal mode.) SAMOD = FIFO read direction: 0, FIFO write direction: 1 DAMOD = FIFO read direction: 1, FIFO write direction: 0 (Fix the address of the FIFO side.) CHNE = 0 (Disable chain transfers.) Specify the setting according to the setting of Sz = MBW. Setting other bits is invalid due to normal mode	
DTBLSj (DTC block size)	01H (Sz = 0: 1 byte/Sz = 1: 2 bytes)	Sz = 0: Max. Packet Size Sz = 1: Max. Packet Size/2
DTCCTj	Any value (Max. 256 times)	Any value (Max. 256 times)
DTDARj (Destination address)	FIFO Read direction: Data transfer destination address FIFO Write direction : D0FIFOD00/D1FIFOD00	
DTSARj (Source address)	FIFO Read direction : D0FIFOD00/D1FIFOD00 FIFO Write direction: Data transfer source address	

Caution: j=D0FIFO/D1FIFO are assigned to activation source (0~23)
For details of DTC setting, see CHAPTER 19 DATA TRANSFER CONTROLLER

8. 34.6.1 A/D converter characteristics(p.1221)

Voltage Range of A/D conversion was extended.

Old:

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

(T_A = –40 to +85°C, 2.7 V ≤ AV_{REFP} ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V, HALT mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				12	bit
Overall error[Notes 1, 2, 3]	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	3.375			μs
Zero-scale error[Notes 1, 2, 3]	E_{ZS}	12-bit resolution		±1.3	±3.2	LSB
Full-scale error[Notes 1, 2, 3]	E_{FS}	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error[Notes 1, 2, 3]	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error[Notes 1, 2, 3]	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Notes 1. TYP. Value is the average value at AV_{DD} = AV_{REFP} = 3 V and T_A = 25°C. MAX. value is the average value ±3σ at normalized distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

Cautions 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.

In addition, separate the reference voltage line of AV_{REFP} from the other power lines to keep it free from the influences of noise.

2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27 and P150 to P154.

New:

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI12

(T_A = –40 to +85°C, 2.4 V ≤ AV_{REFP} ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V, HALT mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				12	bit
Overall error Notes 1, 2, 3	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	3.375			μs
Zero-scale error Notes 1, 2, 3	E_{ZS}	12-bit resolution		±1.3	±3.2	LSB
Full-scale error Notes 1, 2, 3	E_{FS}	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error Notes 1, 2, 3	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error Notes 1, 2, 3	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Notes 1. TYP. Value is the average value at AV_{DD} = AV_{REFP} = 3 V and T_A = 25°C. MAX. value is the average value ±3σ at normalized distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

Cautions 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.

In addition, separate the reference voltage line of AV_{REFP} from the other power lines to keep it free from the influences of noise.

2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27 and P150 to P154.

9.34.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1234)

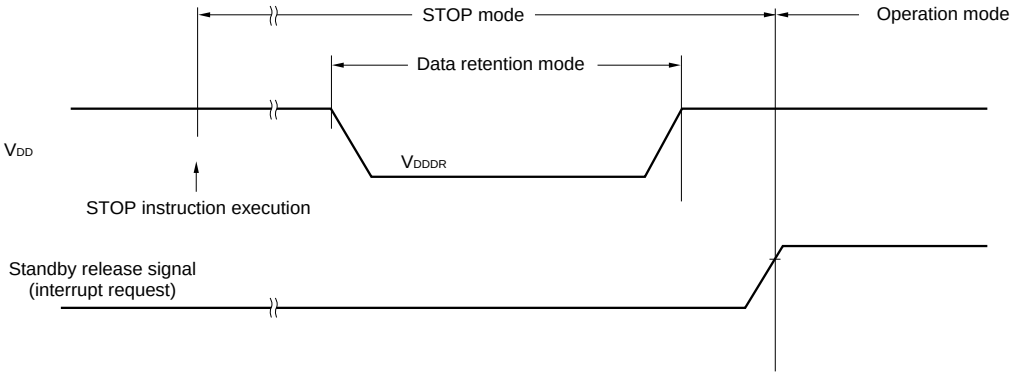
Old:

34.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



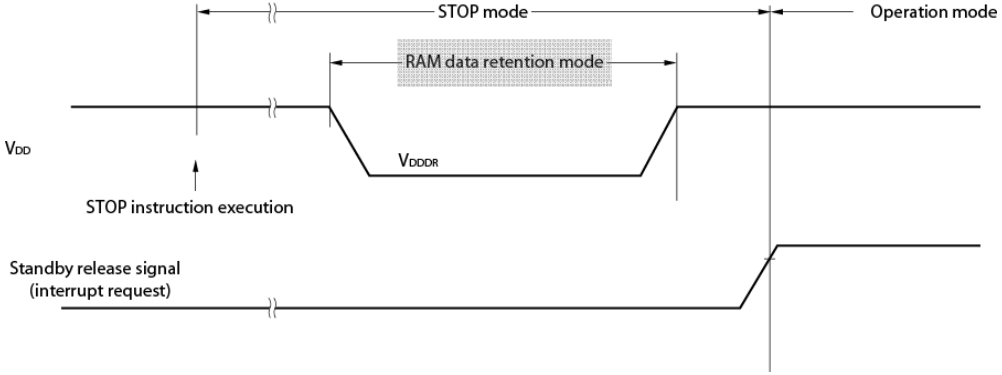
New:

34.9 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		3.6	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



10. 35.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1294)

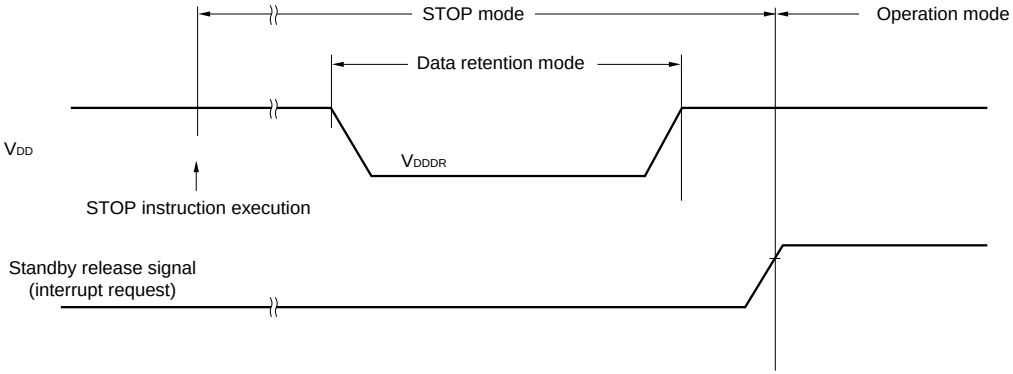
Old:

35.9 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



New:

35.9 RAM Data Retention Characteristics

(T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		3.6	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.