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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A016A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/L12 Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/L12 Group R5F10Rxxx	Lot No. All lots	Reference Document	RL78/L12 User's Manual: Hardware Rev. 1.00 R01UH0330EJ0100 (Jan. 2013)		

This document describes misstatements found in the RL78/L12 User's Manual: Hardware Rev. 1.00 (R01UH0330EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
3.1.3 Internal data memory space	Page 60	Specifications extended
12.6.3 SNOOZE mode function	Page 490	Specifications changed
19.3.2 STOP mode	Pages 746, 747	Incorrect descriptions revised
19.3.3 SNOOZE mode	Page 749	Incorrect descriptions revised
23.3.6 Invalid memory access detection function	Page 797	Incorrect descriptions revised
Figure 25-3 Format of Option Byte (000C2H)	Page 810	Specifications extended
26.4.3 Procedure for accessing data flash memory	Page 823	Incorrect descriptions revised
30.3.1 Pin characteristics	Pages 867, 868	Incorrect descriptions revised
30.3.2 Supply current characteristics	Pages 872 to 877	Incorrect descriptions revised
30.4 AC Characteristics	Page 878	Specifications extended
30.5.1 Serial array unit	Pages 881 to 899	Incorrect descriptions revised
30.5.2 Serial interface IICA	Pages 900 to 902	Incorrect descriptions revised
30.6.1 A/D converter characteristics	Pages 903 to 905	Specifications extended
30.6.2 Temperature sensor/internal reference voltage characteristics	Page 905	Incorrect descriptions revised
30.6.3 POR circuit characteristics	Page 905	Incorrect descriptions revised
30.6.5 Supply voltage rise time	Page 907	Specifications added
30.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 912	Specifications extended
ELECTRICAL SPECIFICATIONS (G: T_A = −40 to +105°C)	New	Specifications extended

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0330EJ0100	
1	3.1.3 Internal data memory space		Page 60	Page 3
2	12.6.3 SNOOZE mode function		Page 490	Pages 4 and 5
3	19.3.2 STOP mode		Pages 746, 747	Page 6
4	19.3.3 SNOOZE mode		Page 749	Page 7
5	23.3.6 Invalid memory access detection function		Page 797	Pages 8 and 9
6	Figure 25-3 Format of Option Byte (000C2H)		Page 810	Page 10
7	26.4.3 Procedure for accessing data flash memory		Page 823	Page 11,12
8	30.3.1 Pin characteristics		Pages 867, 868	Page 13
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13	30.6.1 A/D converter characteristics		Pages 903 to 905	Page 13
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17	30.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		Page 912	Page 14
18	ELECTRICAL SPECIFICATIONS (G: T_A = −40 to +105°C)		New	Page 14

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/L12 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A016A/E	Jan.10.2014	First edition issued Corrections No.1 to No.18 revised (This document)

1. 3.1.3 Internal data memory space

Incorrect:

Cautions 2. The internal RAM in the following products cannot be used as stack area when using the self-programming function and data flash function.

R5F10Rx8 (x = B, F, G, J): FFE20H to FFEDFH, FFB00H to FFC89H
R5F10RxA (x = B, F, G, J, L): FFE20H to FFEDFH, FFB00H to FFC89H
R5F10RxC (x = B, F, G, J, L): FFE20H to FFEDFH, FF900H to FFC89H

Correct:

Cautions 2. While self-programming is being executed or rewriting the data flash, do not allocate the RAM address which is used in stack, data buffer, the branch of vectored interrupt servicing, or the transfer destination or source by DTC in the address between FFE20H to FFEDFH.

3. The RAM area in the products listed below cannot be used when using the self-programming function or rewriting the data flash, because they are used by libraries.

R5F10Rx8 (x = B, F, G,J) : FFB00H to FFC89H
R5F10RxA (x = B, F, G,J, L) : FFB00H to FFC89H
R5F10RxC (x = B, F, G,J, L) : FF900H to FFC89H

2. 12.6.3 SNOOZE mode function

Incorrect:
SNOOZE mode makes UART operate reception by RxDq pin input detection while the STOP mode. Normally UART stops communication in the STOP mode. But, using the SNOOZE mode makes reception UART operate unless the CPU operation by detecting RxDq pin input.

When using the SNOOZE mode function, set the SWCm bit of serial standby control register m (SSCm) to 1 just before switching to the STOP mode.

Cautions: 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for f_{CLK}.
2. The maximum transfer rate when using UARTq in the SNOOZE mode is 9600 bps.

Correct:
SNOOZE mode makes UART operate reception by RxDq pin input detection while the STOP mode. Normally UART stops communication in the STOP mode. But, using the SNOOZE mode makes reception UART operate unless the CPU operation by detecting RxDq pin input.

When using UARTq in SNOOZE mode, execute the following settings before entering STOP mode (Refer to Flowcharts of SNOOZE mode operation in Figure 12-93 and Figure 12-95).
- **In SNOOZE mode, UART reception baud rate must be set differently from normal operation. Refer to Table 12-3 to set registers SPSm and SDRmn [15:9].**
- **Set bits EOCmn and SSECmn to enable or disable the error interrupt (INTSRE0) when a communication error occurs.**
- **Set the SWCm bit in the serial standby control register m (SSCm) to 1 just before entering STOP mode. After initialization, set the SSm1 bit to 1 in the serial channel start register m (SSm).**

When the MCU detects the RxDq pin edge input (input the start bit) after entering STOP mode, the UART reception is started.

Cautions: 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.
2. The transfer rate in SNOOZE mode is 4800 bps only.
3. When the SWCm bit is 1, UARTq can be used only when the reception is started in STOP mode. If UARTq is used with other SNOOZE function or interrupts concurrently and the reception is started in state other than STOP mode as described below, the UARTq cannot receive data correctly and may cause a framing error or parity error.
•The case the UARTq reception is started from the moment the SWCm bit is set to 0 before the MCU enters STOP mode
•The case the UARTq reception is started in SNOOZE mode
•The case the UARTq reception is started from the moment the MCU exits STOP mode and enters normal mode using interrupts before the SWCm bit is set to 0

4. When the SSECm bit is 1, if a parity error, framing error, or overrun error occurs, flags PEFmn, FEFmn, or OVFmn is not set, nor an error interrupt (INTSREq) is generated. To set the SSECm bit to 1, clear flags PEFmn, FEFmn, and OVFmn before setting the SWC0 bit to 1, and read bits 7 to 0 (RxDq) in the SDRm1 register.

Table 12-3 UART Reception Baud Rate Setting in SNOOZE Mode

High-speed on-chip oscillator (f_{IH})	UART reception baud rate in SNOOZE mode			
	Baud rate: 4800 bps			
	Operating clock (f_{MCK})	SDRmn [15:9]	Maximum acceptable value	Minimum acceptable value
24 MHz ± 1.0% (note)	$f_{CLK}/2^5$	79	1.60%	−2.18%
16 MHz ± 1.0% (note)	$f_{CLK}/2^4$	105	2.27%	−1.53%
12 MHz ± 1.0% (note)	$f_{CLK}/2^4$	79	1.60%	−2.19%
8 MHz ± 1.0% (note)	$f_{CLK}/2^3$	105	2.27%	−1.53%
6 MHz ± 1.0% (note)	$f_{CLK}/2^3$	79	1.60%	−2.19%
4 MHz ± 1.0% (note)	$f_{CLK}/2^2$	105	2.27%	−1.53%
3 MHz ± 1.0% (note)	$f_{CLK}/2^2$	79	1.60%	−2.19%
2 MHz ± 1.0% (note)	$f_{CLK}/2^1$	105	2.27%	−1.54%
1 MHz ± 1.0% (note)	$f_{CLK}/2^0$	105	2.27%	−1.57%

Note: When the high-speed on-chip oscillator clock accuracy is at ± 1.5% or 2.0%, the acceptable range is limited as follows:
- f_{IH} ± 1.5%: Subtract 0.5% from the maximum acceptable value of f_{IH} ± 1.0%, and add 0.5% to the minimum acceptable value of f_{IH} ± 1.0%.
- f_{IH} ± 2.0%: Subtract 1.0% from the maximum acceptable value of f_{IH} ± 1.0%, and add 1.0% to the minimum acceptable value of f_{IH} ± 1.0%.

Remarks: Maximum and minimum acceptable values in the above table are the baud rate acceptable values in UART reception. Make sure to set the baud rate for transmission within this range.

3. 19.3.2 STOP mode

Incorrect:

Figure 19-5 STOP Mode Release by Interrupt Request Generation (1/2)

(1) When high-speed system clock (X1 oscillation) is used as CPU clock

(omitted)

Notes: 2. Wait time for STOP mode release

- **High-speed system clock (X1 oscillation): 3-clock**

(2) When high-speed system clock (external clock input) is used as CPU clock

(3) When high-speed on-chip oscillator clock is used as CPU clock

(omitted)

Notes: 2.**Supply of the clock is stopped: 19.08 to 32.99 µs**

Wait

- When vectored interrupt servicing is carried out: 7 clocks
- When vectored interrupt servicing is not carried out: 1 clock

Correct:

Figure 19-5 STOP Mode Release by Interrupt Request Generation (1/2)

(1) When high-speed system clock (X1 oscillation) is used as CPU clock

(omitted)

Notes:2. STOP mode release time

Supply of the clock is stopped: 18 µs to "whichever is longer 65 µs or the oscillation stabilization time"

Wait

- When vectored interrupt servicing is carried out: 10 to 11 clocks
- When vectored interrupt servicing is not carried out: 4 to 5 clocks

Remark: The time to stop clock supply varies depending on the temperature conditions and STOP mode time.

(2) When high-speed system clock (external clock input) is used as CPU clock

(3) When high-speed on-chip oscillator clock is used as CPU clock

(omitted)

Notes: 2. STOP mode release time

Supply of the clock is stopped: 18 to 65 µs

Wait

- When vectored interrupt servicing is carried out: 7 clocks
- When vectored interrupt servicing is not carried out: 1 clock

Remark: The time to stop clock supply varies depending on the temperature conditions and STOP mode time.

4. 19.3.3 SNOOZE mode

Incorrect:

In SNOOZE mode transition, wait status to be only following time.

From STOP to SNOOZE

HS (High-speed main) mode: 18.96 to 28.95 µs
LS (Low-speed main) mode: 20.24 to 28.95µs
LV (Low-voltage main) mode: 20.98 to 28.95 µs

From SNOOZE to normal operation

- **When vectored interrupt servicing is carried out:**
  HS (High-speed main) mode: 6.79 to 12.4 µs + 7 clocks
  LS (Low-speed main) mode: 2.58 to 7.8 µs + 7 clocks
  LV (Low-voltage main) mode: 12.45 to 17.3 µs + 7 clocks
- **When vectored interrupt servicing is not carried out:**
  HS (High-speed main) mode: 6.79 to 12.4 µs + 1 clock
  LS (Low-speed main) mode: 2.58 to 7.8 µs + 1 clock
  LV (Low-voltage main) mode: 12.45 to 17.3 µs + 1 clock

Correct:

The MCU transits from STOP mode to SNOOZE mode or from SNOOZE mode to normal operation after time shown below elapses.

Transit time from STOP mode to SNOOZE mode: 18 to 65 µs
Remark: The transit time from STOP mode to SNOOZE mode varies depending on the temperature conditions and STOP mode time.

Transit time from SNOOZE mode to normal operation:

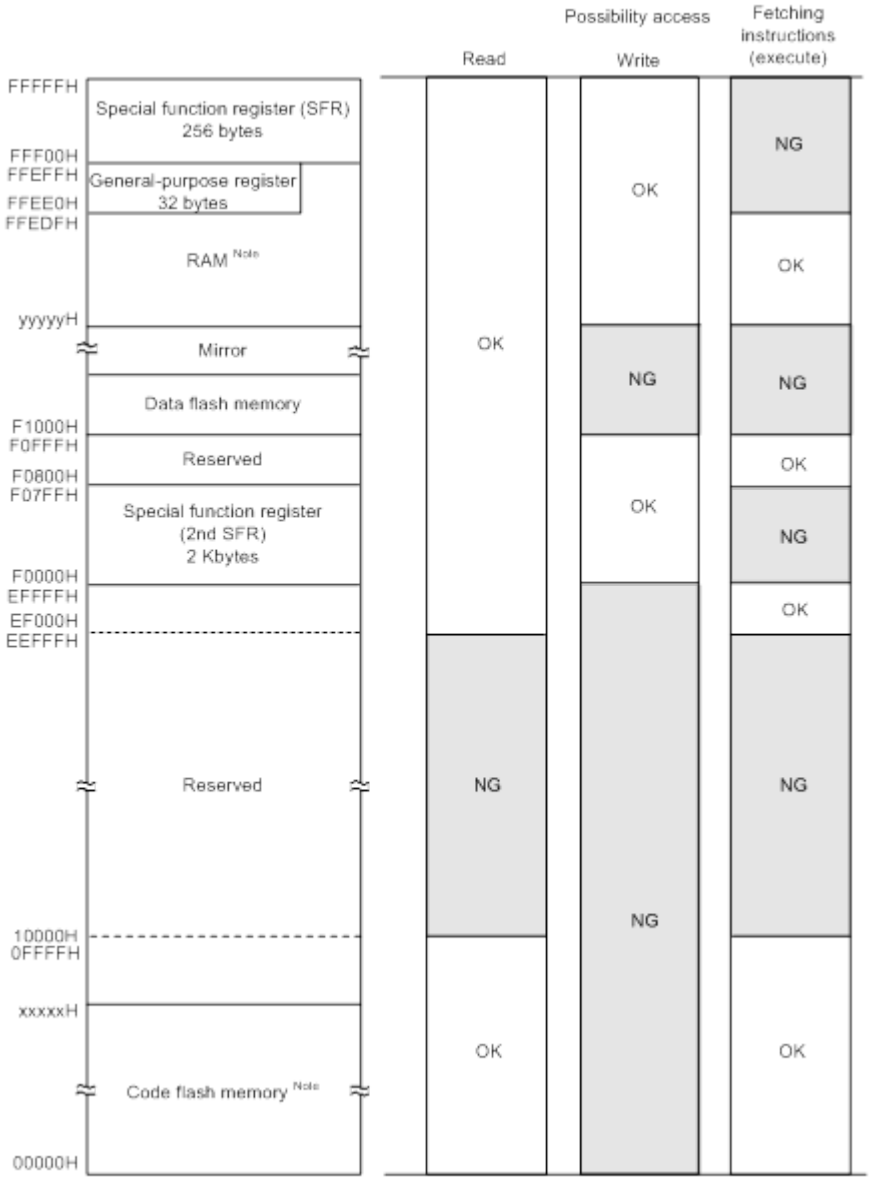
- **When vectored interrupt servicing is carried out:**
  HS (High-speed main) mode: "4.99 to 9.44 µs" + 7 clocks
  LS (Low-speed main) mode: "1.10 to 5.08 µs" + 7 clocks
  LV (Low-voltage main) mode: "16.58 to 25.40 µs" + 7 clocks

- **When vectored interrupt servicing is not carried out:**
  HS (High-speed main) mode: "4.99 to 9.44 µs" + 1 clock
  LS (Low-speed main) mode: "1.10 to 5.08 µs" + 1 clock
  LV (Low-voltage main) mode: "16.58 to 25.40 µs" + 1 clock

5. 23.3.6 Invalid memory access detection function

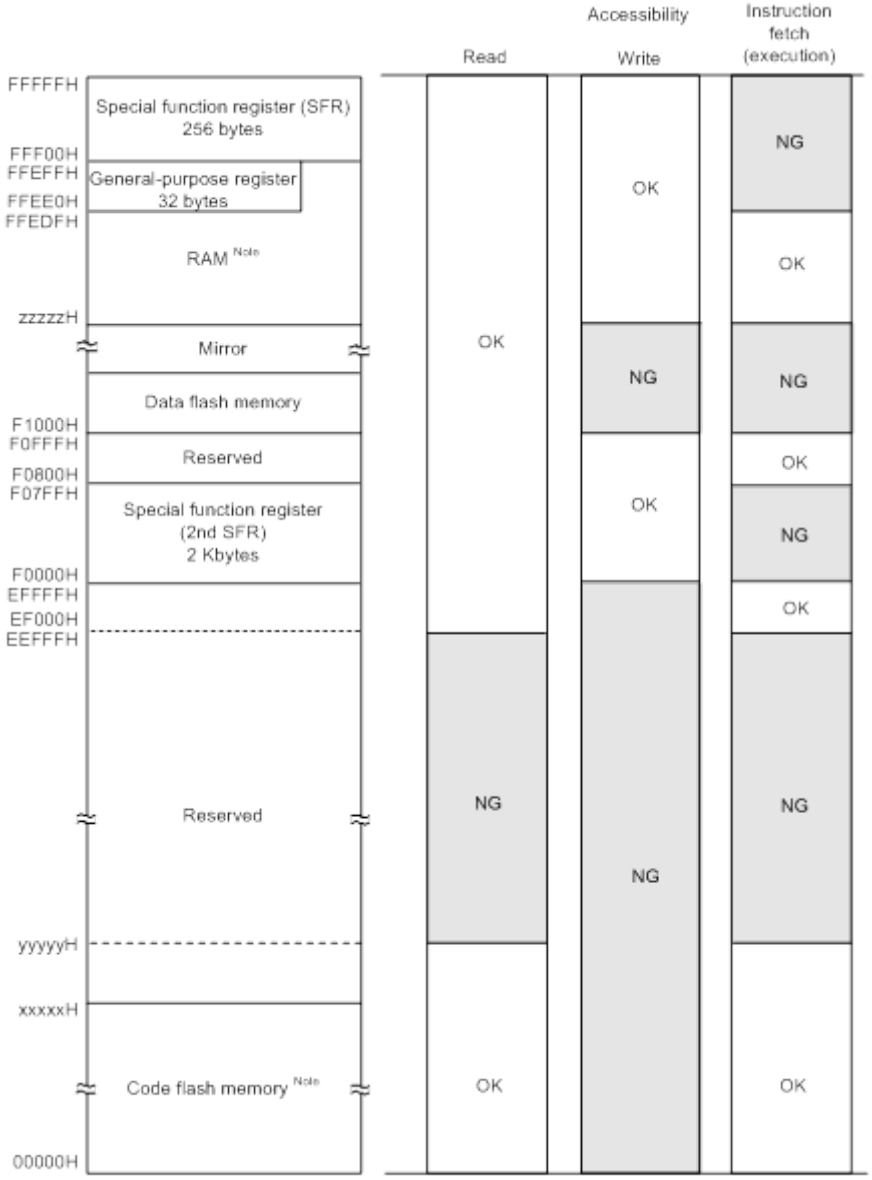
Incorrect:

Figure 23-10 Invalid access detection area



Correct:

Figure 23-10 Invalid access detection area



Note: Code flash memory and RAM address of each product are as follows.

Products	Code flash memory (00000H to xxxxxH)	RAM (yyyyyH to FFEFFH)
R5F10Rx8 (x = B, F, G, J)	8192 × 8 bit (00000H to 01FFFH)	1024 × 8 bit (FFB00H to FFEFFH)
R5F10RxA (x = B,F, G, J, L)	16384 × 8 bit (00000H to 03FFFH)	1024 × 8 bit (FFB00H to FFEFFH)
R5F10RxC (x = B, F, G, J, L)	32768 × 8 bit (00000H to 07FFFH)	1536 × 8 bit (FF900H to FFEFFH)

Note: Code flash memory area, RAM area, and the detected lowest address of each product are as follows.

Products	Code flash memory (00000H to xxxxxH)	RAM (zzzzzH to FFEFFH)	Detected lowest address for read/instruction fetch (execution) (yyyyyH)
R5F10Rx8 (x = B, F, G, J)	8192 × 8 bit (00000H to 01FFFH)	1024 × 8 bit (FFB00H to FFEFFH)	10000H
R5F10RxA (x = B, F, G, J, L)	16384 × 8 bit (00000H to 03FFFH)	1024 × 8 bit (FFB00H to FFEFFH)	10000H
R5F10Rx8 (x = B, F, G, J)	8192 × 8 bit (00000H to 01FFFH)	1024 × 8 bit (FFB00H to FFEFFH)	80000H

6. Figure 25-3 Format of Option Byte (000C2H)

Old:

Figure 25-3 Format of Option Byte (000C2H)

Address: 000C2H

7	6	5	4	3	2	1	0
CMODE1	C5MODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 24 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
1	0	1	1	4 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

Caution: Be sure to set 10B to bits 5 and 4.

New:

Figure 25-3. Format of Option Byte (000C2H)

Address: 000C2H note

7	6	5	4	3	2	1	0
CMODE1	C5MODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 24 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
0	**0**	**1**	**0**	**6 MHz**
1	0	1	1	4 MHz
0	**0**	**1**	**1**	**3 MHz**
1	**1**	**0**	**1**	**2 MHz**
1	1	0	1	1 MHz
Other than above				Setting prohibited

Caution: Be sure to set 10B to bits 5 and 4.

7. 26.4.3 Procedure for accessing data flash memory

Incorrect:

The data flash memory is initially stopped after a reset ends and cannot be accessed (read or programmed). To
access the memory, perform the following procedure:

<1> Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).
<2> Wait for the setup to finish for software timer. etc.
The time setup takes differs for each main clock mode.
<Setup time for each main clock mode>
• HS (High-speed main): 5μs
• LS (Low-speed main): 720 ns
• LV (Low-voltage main): 10μs

<3> After the wait, the data flash memory can be accessed.

Cautions 1. Accessing the data flash memory is not possible during the setup time.
2. Before executing a STOP instruction during the setup time, temporarily clear DFLEN to 0.

Correct:

The data flash memory is stopped after a reset ends. To access the data flash, make initial settings according to the

following procedure.

<1> Set bit 0 (DFLEN) of the data flash control register (DFLCTL) to 1.
<2> Wait for the setup to finish for software timer, etc.
The time setup takes differs for each flash operation mode for the main clock.
<Setup time for each flash operation mode>
• HS (High speed main): 5 μs
• LS (Low speed main): 720 ns
• LV (Low voltage main): 10 μs
<3> After the wait, the data flash memory can be accessed.

Cautions 1. Accessing the data flash memory is not possible during the setup time.
2. Transition to the STOP mode is not possible during the setup time. To enter the STOP mode during the setup time, clear DFLEN to 0 and then execute the STOP instruction.
3. The high-speed on-chip oscillator should be kept operating during data flash rewrite. If it is kept stopping, operate the high-speed on-chip oscillator clock (HIOSTOP = 0) and execute the data flash library after 30 μs have elapsed.

After initialized, the data flash memory can be read by using a CPU instruction or can be read/written by using a data

flash library.

If the DMA controller operates when the data flash memory is accessed, however, follow one of these procedures:

(A) Suspending/forcibly terminating DMA transfer

Before reading the data flash memory, suspend DMA transfer of all the channels used.

After setting the DWAITn bit to 1, however, wait at least for the duration of three clocks (fCLK) before reading the

data flash memory. After reading the data flash memory, lift the suspension of transfer by clearing the DWAITn bit to 0.

Or, forcibly terminate DMA transfer in accordance with the procedure in 15.5.5 Forced termination by software

before reading the data flash memory. Resume DMA transfer after the data flash memory has been read.

(B) Access the data flash memory by using the newest data flash library.

(C) Insertion of NOP

Insert an NOP instruction immediately before the instruction that reads the data flash memory.

<Example>

```
MOVW HL,!addr16 ; Reads RAM.
NOP ; Insert NOP instruction before reading data flash memory.
MOV A,[DE] ; Read data flash memory.
```

If a high-level language such as C is used, however, the compiler may generate two instructions for one code. In

this case, the NOP instruction is not inserted immediately before the data flash memory read instruction.

Therefore, read the data flash memory by (A) or (B) above.

Remarks 1. n: DMA channel number (n = 0, 1)

2. fCLK: CPU/peripheral hardware clock frequency

8. 30.3.1 Pin characteristics

Incorrect:
Fixed typo in Note 2 in pages 867 and 868.

Correct:
Refer to pages 7 and 8 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS”.

9. 30.3.2 Supply current characteristics

Incorrect:
Fixed typo in Notes and typical values of I_{DD2} and I_{DD3} in pages 872 to 877.

Correct:
Refer to pages 12 to 17 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS”.

10. 30.4 AC Characteristics

Old:
Specifications of the external system clock frequency and external system clock input high-level width, low-level width in page 878 extended.

New:
Refer to page 18 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS”.

11. 30.5.1 Serial array unit

Incorrect:
Fixed typo in 30.5.1 Serial array unit in pages 881 to 899.

Correct:
Refer to pages 24 to 44 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS”.

12. 30.5.2 Serial interface IICA

Incorrect:
Fixed typo in 30.5.2 Serial interface IICA in pages 900 to 902.

Correct:
Refer to pages 45 to 49 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS”.

13. 30.6.1 A/D converter characteristics

Old:

Specifications in 30.6.1 A/D converter characteristics in pages 903 to 905 extended.

New:

Refer to pages 50 to 53 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS”.

14. 30.6.2 Temperature sensor/internal reference voltage characteristics

Incorrect:
Fixed typo in 30.6.2 Temperature Sensor/Internal Reference Voltage Characteristics in page 905.

Correct:
Refer to page 54 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS”.

15. 30.6.3 POR circuit characteristics

Incorrect:
Fixed typo in 30.6.3 POR circuit characteristics in page 905.

Correct:
Refer to page 54 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS”.

16. 30.6.5 Supply voltage rise time

Old:
Specifications in Supply Voltage Rise Time in page 907 added.

New:
Refer to page 56 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS”.

17. 30.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

Old:
Specifications in Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics in page 912 extended.

New:
Refer to page 61 in Technical Update Exhibit 1 “Chapter 30 ELECTRICAL SPECIFICATIONS (A, D: T_A = −40 to + 85°C)”.

18. ELECTRICAL SPECIFICATIONS (G: T_A = −40 to +105°C)

Old:
Specifications in ELECTRICAL SPECIFICATIONS (G: T_A = −40 to +105°C) extended.

New:
Refer to Technical Update Exhibit 2 “Chapter 31 ELECTRICAL SPECIFICATIONS”.

CHAPTER 30 ELECTRICAL SPECIFICATIONS

This chapter describes the electrical specifications for the products "A: Consumer applications (T_A = −40 to +85°C)", and "G: Industrial applications (T_A when using the RL78 microcontrollers at −40 to +85°C)".

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV_{DD}, or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.1.6 Pins for each product (pins other than port pins).

30.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/3)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} = EV_{DD}	−0.5 to +6.5	V
	EV_{DD}	V_{DD} = EV_{DD}	−0.5 to +6.5	V
	EV_{SS}		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127,P140 to P147	−0.3 to EV_{DD} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60, P61 (N-ch open-drain)	−0.3 to EV_{DD} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{I3}	P20, P21, P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	−0.3 to EV_{DD} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	P20, P21	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI23	−0.3 to EV_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V
	V_{AI2}	ANI0, ANI1	−0.3 to V_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS} is the reference voltage.

Absolute Maximum Ratings (T_A = 25°C) (2/3)

Parameter	Symbols	Conditions			Ratings	Unit
LCD voltage	V_{L1}	V_{L1} voltage[Note 1]			−0.3 to +2.8 and −0.3 to V_{L4} +0.3	V
	V_{L2}	V_{L2} voltage[Note 1]			−0.3 to V_{L4} +0.3 [Note 2]	V
	V_{L3}	V_{L3} voltage[Note 1]			−0.3 to V_{L4} +0.3 [Note 2]	V
	V_{L4}	V_{L4} voltage[Note 1]			−0.3 to +6.5	V
	V_{LCAP}	CAPL, CAPH voltage[Note 1]			−0.3 to V_{L4} +0.3 [Note 2]	V
	V_{LOUT}	COM0 to COM7, SEG0 to SEG38, COMEXP output voltage	External resistance division	Other than memory-type liquid crystal mode	−0.3 to V_{DD} +0.3 [Note 2]	V
				Memory-type liquid crystal mode	−0.3 to V_{L4} +0.3 [Note 2]	
			Capacitor split		−0.3 to V_{DD} +0.3 [Note 2]	
			Internal voltage boosting		−0.3 to V_{L4} +0.3 [Note 2]	

Notes
1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.
2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS} is the reference voltage.

Absolute Maximum Ratings (T_A = 25°C) (3/3)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	−70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	−100	mA
	I_{OH2}	Per pin	P20, P21	−0.5	mA
		Total of all pins		−1	mA
Output current, low	I_{OL1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
	I_{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

30.2 Oscillator Characteristics

30.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} ≤ 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.7 V	1.0		8.0	
		1.6 V ≤ V_{DD} <1.8 V	1.0		4.0	
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only the permissible deviation of the oscillator frequencies. Refer to **AC Characteristics** for instruction execution time. Inquire with the resonator manufacturer to perform an evaluation on the actual circuit and check the oscillator characteristics before use.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 or XT1 oscillator, refer to **5.4 System Clock Oscillator**.

30.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	–1		+1	%
			1.6 V ≤ V_{DD} ≤ 1.8 V	–5		+5	%
		–40 to –20 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	–1.5		+1.5	%
			1.6 V ≤ V_{DD} ≤1.8 V	–5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for instruction execution time.

30.3 DC Characteristics

30.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				–10.0 [Note 2]	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% [Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			–40.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–8.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			–4.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			–2.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% [Note 3])	4.0 V ≤ EV_{DD} ≤ 5.5 V			–60.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–15.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			–8.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			–4.0	mA
		Total of all pins (When duty = 70% [Note 3])				–100.0	mA
	I_{OH2}	P20, P21	Per pin			–0.1	mA
			Total of all pins	1.6 V ≤ V_{DD} ≤ 5.5 V		–0.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD}, EV_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA
Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≈ –8.7 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P10, P12, P15, P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				20.0 Note 2	mA
		Per pin for P60, P61				15.0 Note 2	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			4.5	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 (When duty = 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			10.0	mA
		Total of all pins (When duty = 70% Note 3)				150.0	mA
	I_{OL2}	P20, P21	Per pin			0.4	mA
			Total of all pins	1.6 V ≤ V_{DD} ≤ 5.5 V		0.8	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS} and V_{SS} pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL input buffer 1.6 V ≤ EV_{DD} < 3.3 V	1.50		EV_{DD}	V
	V_{IH3}	P20, P21		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60, P61		0.7EV_{DD}		EV_{DD}	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV_{DD}	V
	V_{IL2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20, P21		0		0.3V_{DD}	V
	V_{IL4}	P60, P61		0		0.3EV_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of P10, P12, P15, P17 is EV_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –10 mA	EV_{DD}–1.5			V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	EV_{DD}–0.7			V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –2.0 mA	EV_{DD}–0.6			V
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	EV_{DD}–0.5			V
			1.6 V ≤ EV_{DD} < 5.5 V, I_{OH1} = –1.0 mA	EV_{DD}–0.5			V
	V_{OH2}	P20, P21	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = –100 μA	V_{DD}–0.5			V
Output voltage, low	V_{OL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 20 mA			1.3	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ EV_{DD} < 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20, P21	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V ≤ EV_{DD} < 5.5 V, I_{OL3} = 1.0 mA			0.4	V

Caution P10, P12, P15, P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (5/5)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V_I = EV_{DD}				1	μA
	I_{LIH2}	P20, P21, P137, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V_I = EV_{SS}				−1	μA
	I_{LIL2}	P20, P21, P137, $\overline{\text{RESET}}$	V_I = V_{SS}				−1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
On-chip pull-up resistance	R_{U1}	V_I = EV_{SS}	SEGxx port					
				2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V	10	20	100	kΩ
				1.6 V ≤ EV_{DD} = V_{DD} < 2.4 V	10	30	100	kΩ
	R_{U2}		Ports other than above (Except for P60, P61, and P130)		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

30.3.2 Supply current characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(1/3)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		mA
					Normal operation	V_{DD} = 5.0 V		3.3	5.0	mA
						V_{DD} = 3.0 V		3.3	5.0	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.5	3.7	mA
						V_{DD} = 3.0 V		2.5	3.7	mA
			LS (low-speed main) mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	mA
			LV (low-voltage main) mode Note 5	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.7	mA
						V_{DD} = 2.0 V		1.2	1.7	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	mA
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = –40°C	Normal operation	Square wave input		3.5	4.9	μA
						Resonator connection		3.6	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		3.6	4.9	μA
						Resonator connection		3.7	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		3.7	5.5	μA
						Resonator connection		3.8	5.6	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		3.8	6.3	μA
						Resonator connection		3.9	6.4	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		4.1	7.7	μA
						Resonator connection		4.2	7.8	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash programming.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1), not including the current flowing into RTC, 12-bit interval timer, WDT, and LCD controller/driver.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(2/3)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.44	1.28	mA
					V_{DD} = 3.0 V		0.44	1.28	mA
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.40	1.00	mA
					V_{DD} = 3.0 V		0.40	1.00	mA
			LS (low-speed main) mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		260	530	μA
					V_{DD} = 2.0 V		260	530	μA
			LV (low-voltage main) mode Note 7	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		420	640	μA
					V_{DD} = 2.0 V		420	640	μA
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
			LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
				f_{MX} = 8 MHz Note 3, V_{DD} = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = –40C	Square wave input		0.31	0.57	μA
					Resonator connection		0.50	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.37	0.57	μA
					Resonator connection		0.56	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.46	1.17	μA
					Resonator connection		0.65	1.36	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.57	1.97	μA
					Resonator connection		0.76	2.16	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		0.85	3.37	μA
					Resonator connection		1.04	3.56	μA
	I_{DD3} Note 6	STOP mode Note 8	T_A = –40°C				0.17	0.50	μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.32	1.10	μA
			T_A = +70°C				0.43	1.90	μA
			T_A = +85°C				0.71	3.30	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash programming.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When operating real-time clock (RTC) and setting ultra-low current consumption (AMPHS1 = 1), not including the current flowing into 12-bit interval timer, WDT, LCD controller/driver.

6. The current flowing into RTC, 12-bit interval timer, WDT are not included.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{MAIN} is stopped			0.08		μA
12-bit inteval timer operating current	I_{IT} Notes 1, 2, 4				0.08		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.24		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 7				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8				2.00	12.20	mA
LCD operating current	I_{LCD1} Notes 11, 12	External resistance division method	V_{DD} = EV_{DD} = 5.0 V, V_{L4} = 5.0 V		0.04	0.2	μA
	I_{LCD2} Note 11	Internal voltage boosting method	V_{DD} = EV_{DD} = 5.0 V, V_{L4} = 5.1 V (VLCD = 12H)		1.12	3.7	μA
			V_{DD} = EV_{DD} = 3.0 V, V_{L4} = 3.0 V (VLCD = 04H)		0.63	2.2	μA
	I_{LCD3} Note 11	Capacitor split method	V_{DD} = EV_{DD} = 3.0 V, V_{L4} = 3.0 V		0.12	0.5	μA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	
		CSI/UART operation			0.70	0.84	

(**Note**, **Caution** and **Remark** are lisited on the next page)

Notes 1. Current flowing to the V_{DD}.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the RTC (not including the operating current of the low-speed on-chip oscillator and XT1 oscillator). The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, or I_{DD2} and I_{RTC} when RTC is operating in operation mode or HALT mode. Add I_{FIL} to the above value when using the low-speed on-chip oscillator. The operating current of the RTC is included when I_{DD2} operates with the subsystem clock.

4. Current flowing only to the 12-bit interval timer (not including the operating current of the low-speed on-chip oscillator and XT1 oscillator). The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, or I_{DD2} and I_{IT} when the 12-bit interval timer is operating in operation mode or HALT mode. Add I_{FIL} to the above value when using the low-speed on-chip oscillator.

5. Current flowing only to the WDT (including the operating current of the low-speed on-chip oscillator). The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, or I_{DD2} and I_{WDT} when the WDT is operating in operation mode or HALT mode. Add I_{FIL} to the above value when using the low-speed on-chip oscillator.

6. Current flowing only to the A/D converter. The supply current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter is operating in operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is operating.

8. Current flowing during data flash programming.

9. Current flowing during self-programming.

10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode.**

11. Current flowing only to the LCD controller/driver. The supply current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2} or I_{LCD3}) to the supply current (I_{DD1}, or I_{DD2}) when the LCD controller/driver is operating in operation mode or HALT mode. Not including the current that flows to the LCD panel.

The TYP. value and MAX. value are following conditions.

- When f_{SUB} is selected for system clock, LCD clock = 128 Hz (LCDC0 = 07H)
- 4-Time-Slice, 1/3 Bias Method

12. Not including the current that flows to the external divider resistor when the external resistance division method is used.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

30.4 AC Characteristics

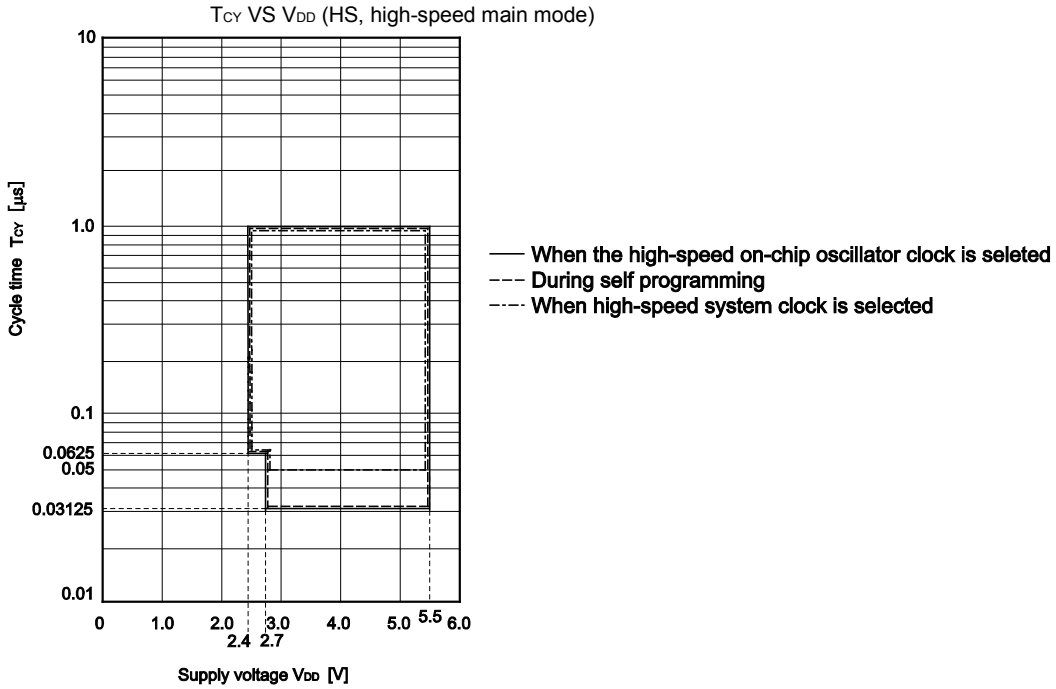
30.4.1 Basic operation

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

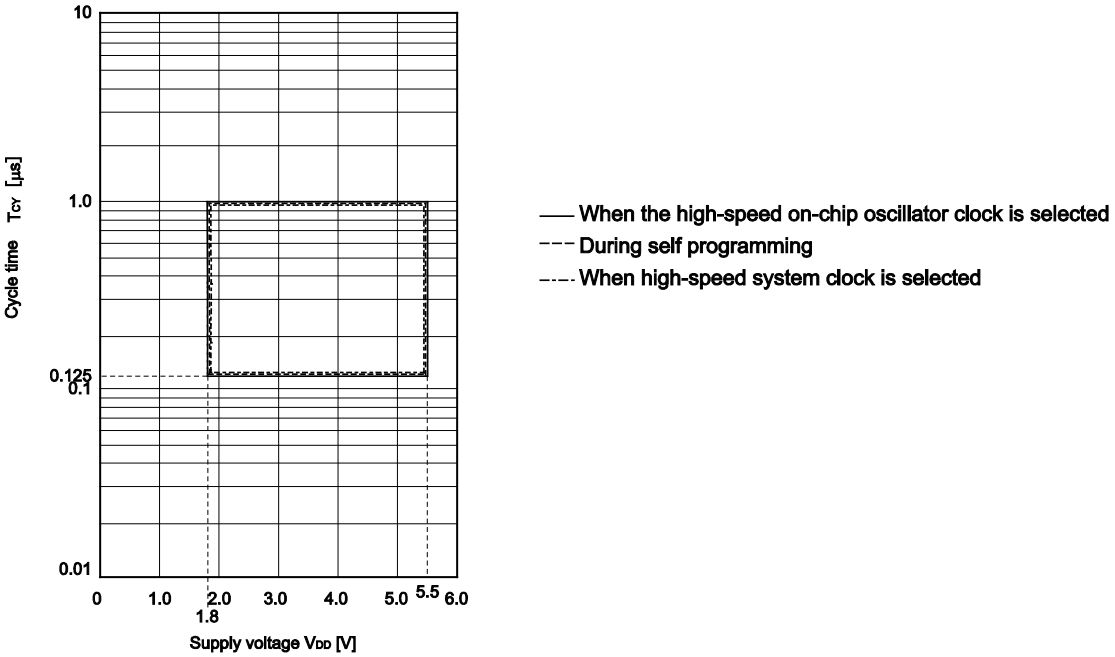
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
		Subsystem clock (f_{SUB}) operation		1.8 V ≤ V_{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (low-voltage main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16	MHz
		1.8 V ≤ V_{DD} < 2.4 V			1.0		8	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4	MHz
	f_{EXS}				32		35	kHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
		1.8 V ≤ V_{DD} < 2.4 V			60			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns
TO00 to TO07 output frequency	f_{TO}	HS (high-speed main) mode		4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
				2.4 V ≤ EV_{DD} < 2.7 V			4	MHz
		LS (low-speed main) mode		1.8 V ≤ EV_{DD} ≤ 5.5 V			4	MHz
		LV (low-voltage main) mode		1.6 V ≤ EV_{DD} ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
				2.4 V ≤ EV_{DD} < 2.7 V			4	MHz
		LS (low-speed main) mode		1.8 V ≤ EV_{DD} ≤ 5.5 V			4	MHz
		LV (low-voltage main) mode		1.8 V ≤ EV_{DD} ≤ 5.5 V			4	MHz
				1.6 V ≤ EV_{DD} < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0		1.6 V ≤ V_{DD} ≤ 5.5 V	1			μs
		INTP1 to INTP7		1.6 V ≤ EV_{DD} ≤ 5.5 V	1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR3		1.8 V ≤ EV_{DD} ≤ 5.5 V	250			ns
				1.6 V ≤ EV_{DD} < 1.8 V	1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

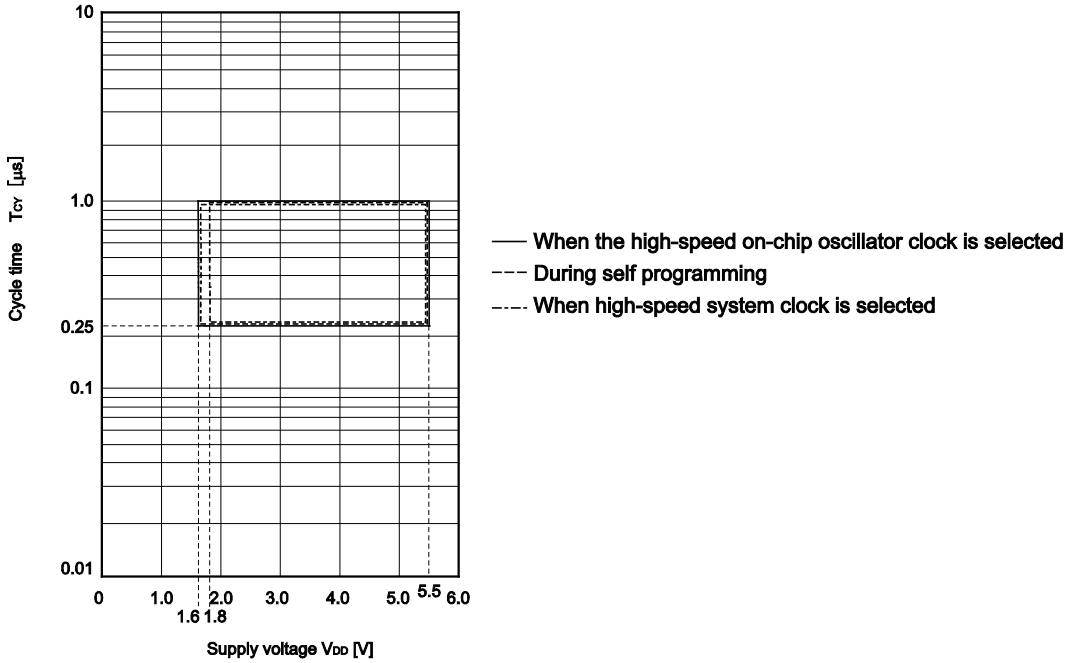
Minimum instruction executing time when the CPU is operating with the main system clock



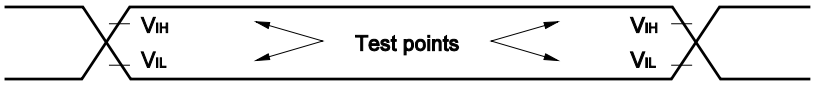
T_{CY} VS V_{DD} (LS, low-speed main mode)



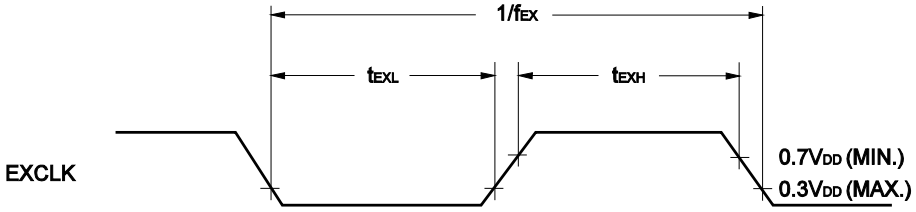
T_{CY} VS V_{DD} (LV, low-voltage main mode)



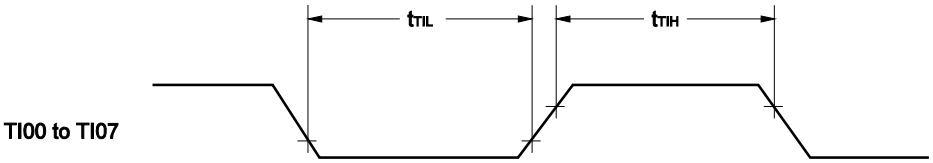
AC Timing Test Points

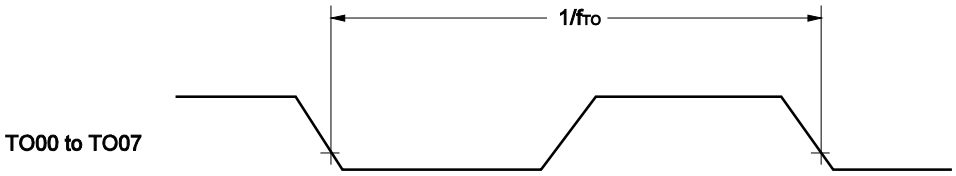


External System Clock Timing

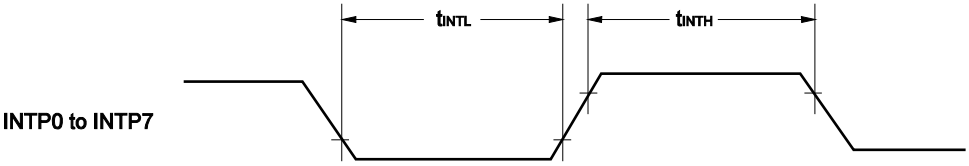


TI/TO Timing

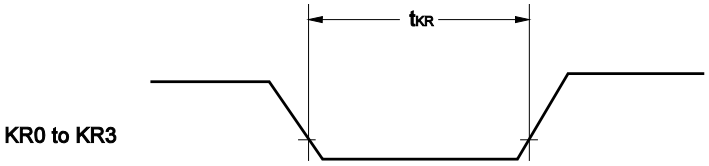




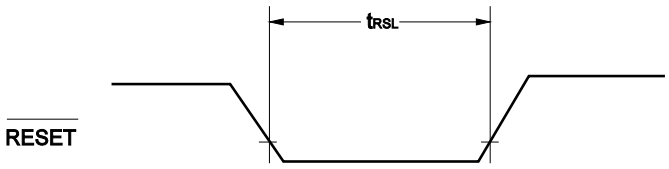
Interrupt Request Input Timing



Key Interrupt Input Timing

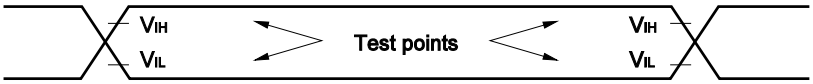


$\overline{\text{RESET}}$ Input Timing



30.5 Peripheral Functions Characteristics

AC Timing Test Points



30.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		4.0		1.3		0.6	Mbps
		1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V				f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2				1.3		0.6	Mbps
		1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V						f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2						0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. CPU/peripheral hardware clock (f_{CLK}) in each operating mode is as below.

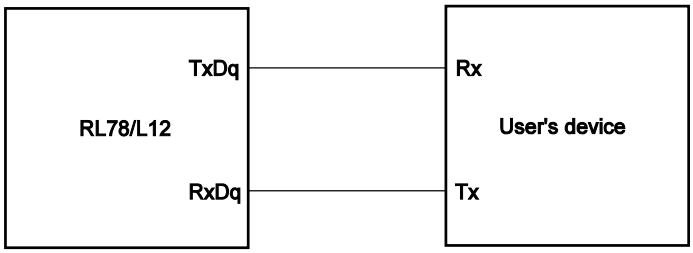
HS (high-speed main) mode: f_{CLK} = 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: f_{CLK} = 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

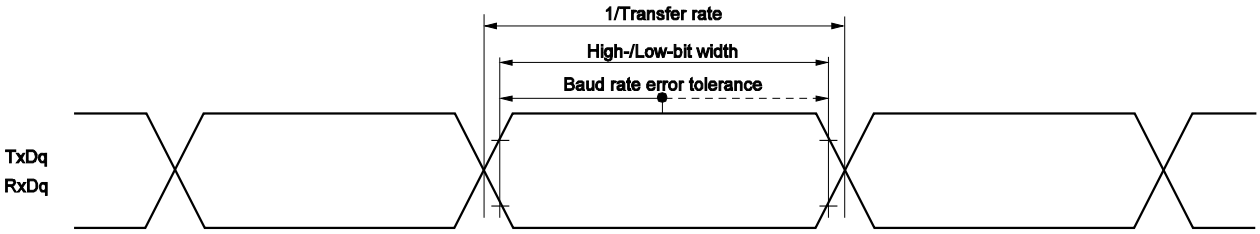
LV (low-voltage main) mode: f_{CLK} = 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0), g: PIM and POM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(2) During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$... internal clock output)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{SCKp}$ cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 5.5 V	167 Note 1		500 Note 1		1000 Note 1		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	250 Note 1		500 Note 1		1000 Note 1		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V			500 Note 1		1000 Note 1		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V					1000 Note 1		ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	t_{KCY1}/2 –12		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V	t_{KCY1}/2 –18		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	t_{KCY1}/2 –38		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V			t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V					t_{KCY1}/2 –100		ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 5.5 V	44		110		110		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	75		110		110		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V			110		110		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V					220		ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI1}	2.4 V ≤ EV_{DD} ≤ 5.5 V	19		19		19		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V			19		19		
		1.6 V ≤ EV_{DD} ≤ 5.5 V					19		
Delay time from $\overline{SCKp}$↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4, 2.4 V ≤ EV_{DD} ≤ 5.5 V		25		25		25	ns
		C = 30 pF Note 4, 1.8 V ≤ EV_{DD} ≤ 5.5 V				25		25	
		C = 30 pF Note 4, 1.6 V ≤ EV_{DD} ≤ 5.5 V						25	

Notes 1. For CSI00, set a cycle of 2/f_{MCK} or longer. For CSI01, set a cycle of 4/f_{MCK} or longer.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time become "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	**t_{KCY2}**	**4.0 V ≤ EV_{DD} ≤ 5.5 V**	**20 MHz < f_{MCK}**	**8/f_{MCK}**						**ns**
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V	16 MHz < f_{MCK}	8/f_{MCK}						ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 5.5 V		6/f_{MCK} and 500		6/f_{MCK}		6/f_{MCK}		ns
		1.8 V ≤ EV_{DD} < 2.4 V				6/f_{MCK}		6/f_{MCK}		ns
		1.6 V ≤ EV_{DD} < 1.8 V						6/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 –7		t_{KCY2}/2 –7		t_{KCY2}/2 –7		ns
		2.7 V ≤ EV_{DD} < 4.0 V		t_{KCY2}/2 –8		t_{KCY2}/ –8		t_{KCY2}/2 –8		ns
		2.4 V ≤ EV_{DD} < 2.7 V		t_{KCY2}/2 –18		t_{KCY2}/2 –18		t_{KCY2}/2 –18		ns
		1.8 V ≤ EV_{DD} < 2.4 V				t_{KCY2}/2 –18		t_{KCY2}/2 –18		ns
		1.6 V ≤ EV_{DD} < 1.8 V						t_{KCY2}/2 –66		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		2.4 V ≤ EV_{DD} < 2.7 V		1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		
		1.8 V ≤ EV_{DD} < 2.4 V				1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.6 V ≤ EV_{DD} < 1.8 V						1/f_{MCK} +40		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}	2.4 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.8 V ≤ EV_{DD} < 2.4 V				1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.6 V ≤ EV_{DD} < 1.8 V						1/f_{MCK}+ 250		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	4.0 V ≤ EV_{DD} ≤ 5.5 V		2/f_{MCK} +44		2/f_{MCK} +110		2/f_{MCK} +110	ns
			2.7 V ≤ EV_{DD} < 4.0 V		2/f_{MCK} +44		2/f_{MCK} +110		2/f_{MCK} +110	ns
			2.4 V ≤ EV_{DD} < 2.7 V		2/f_{MCK} +75		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.8 V ≤ EV_{DD} < 2.4 V				2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.6 V ≤ EV_{DD} < 1.8 V						2/f_{MCK}+ 220	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time become "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SOp output lines.

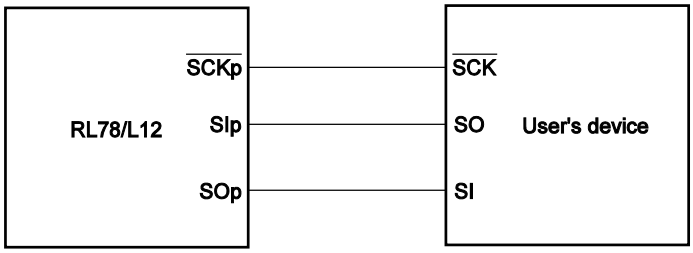
4. Transfer rate in the SNOOZE mode is MAX.1 Mbps.

Caution Select the normal input buffer for the SIp pin and $\overline{SCKp}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

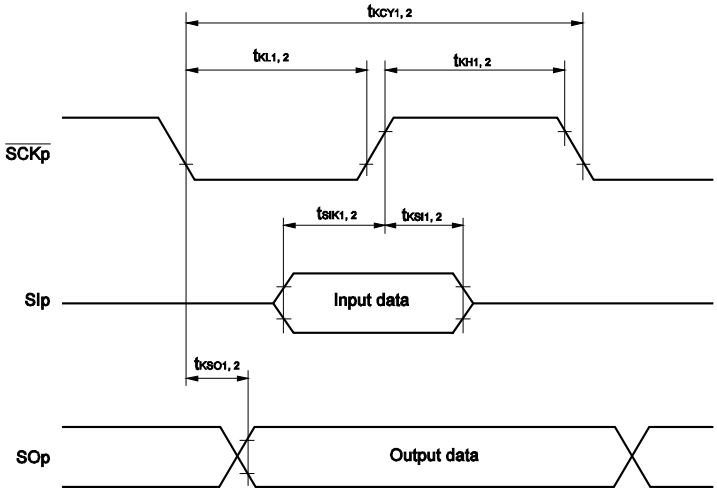
Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0),
n: Channel number (n = 0, 1), g: PIM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

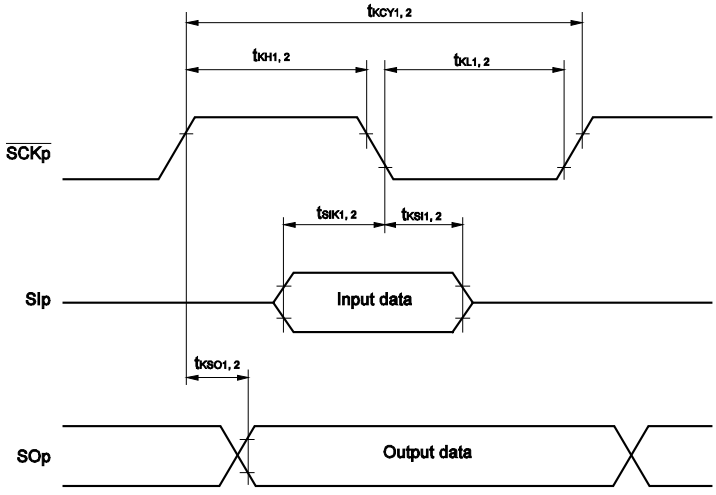
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01)

2. m: Unit number, n: Channel number (mn = 00, 01)

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0		1.3		0.6	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0		1.3		0.6	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0		1.3		0.6	Mbps
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V					f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3				1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. Use it with EV_{DD}≥V_b.

3. CPU/peripheral hardware clock (f_{CLK}) in each operating mode is as below.

HS (high-speed main) mode: f_{CLK} = 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: f_{CLK} = 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

LV (low-voltage main) mode: f_{CLK} = 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Note 1**		**Note 1**		**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Note 3**		**Note 3**		**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ V_b = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			**Note 6**		**Note 6**		**Note 6**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ V_b = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V					**Notes 5, 6**		**Notes 5, 6**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V				0.43 Note 7		0.43 Note 7	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Use it with $EV_{DD} \geq V_b$.

6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

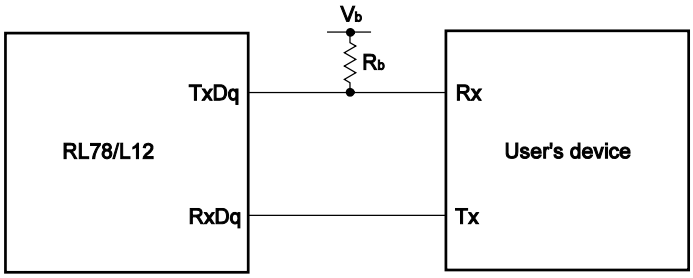
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

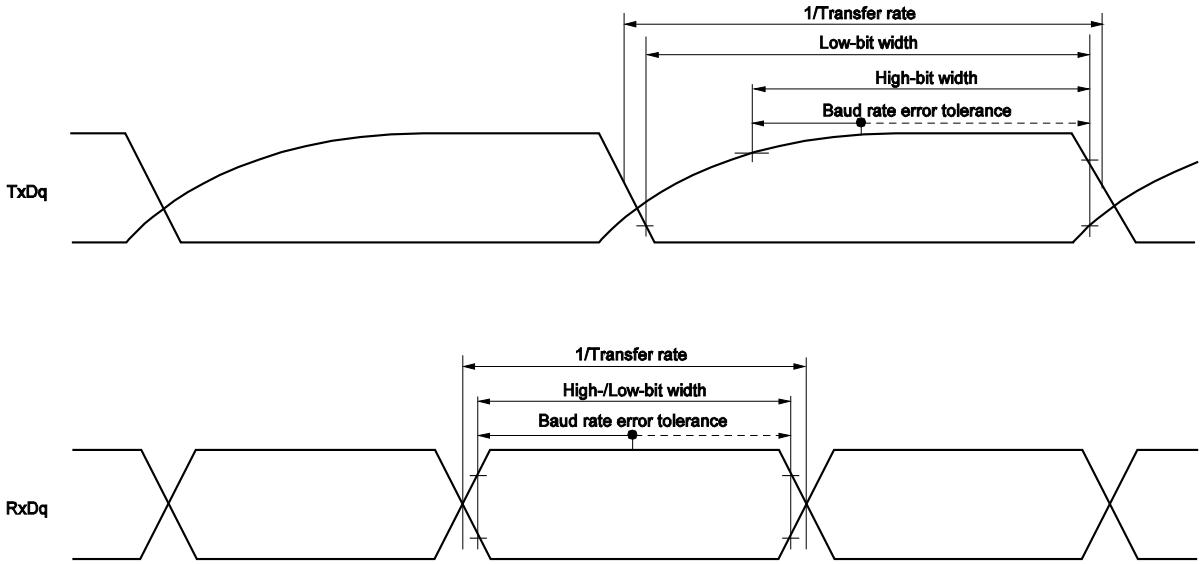
7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

2. q: UART number (q = 0), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

(5) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200 Note 1		1150 Note 1		1150 Note 1		ns
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300 Note 1		1150 Note 1		1150 Note 1		ns
$\overline{\text{SCKp}}$ high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 –50		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 –120		t_{KCY1}/2 –120		t_{KCY1}/2 –120		ns
$\overline{\text{SCKp}}$ low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 –7		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 –10		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 2	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		479		ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 2	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note 2	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns
SIp setup time (to $\overline{\text{SCKp}}$↓) Note 3	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		23		110		110		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		33		110		110		ns
SIp hold time (from $\overline{\text{SCKp}}$↓) Note 3	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from $\overline{\text{SCKp}}$↑ to SOp output Note 3	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			10		10		10	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10		10		10	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

Notes 1. For CSI00, set a cycle of 2/f_{MCK} or longer. For CSI01, set a cycle of 4/f_{MCK} or longer.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

3. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance, C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{SCKp}$ cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note], C_b = 30 pF, R_b = 5.5 kΩ			1150		1150		ns
$\overline{SCKp}$ high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 –75		t_{KCY1}/2 –75		t_{KCY1}/2 –75		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 –170		t_{KCY1}/2 –170		t_{KCY1}/2 –170		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 –458		t_{KCY1}/2 –458		t_{KCY1}/2 –458		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note], C_b = 30 pF, R_b = 5.5 kΩ				t_{KCY1}/2 –458		t_{KCY1}/2 –458		ns
$\overline{SCKp}$ low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 –12		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 –18		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 –50		t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note], C_b = 30 pF, R_b = 5.5 kΩ				t_{KCY1}/2 –50		t_{KCY1}/2 –50		ns

Note Use it with EV_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to **52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and SCKp $\overline{\text{pin}}$ by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.**

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS(low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to $\overline{SCKp}$↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			479		479		ns
SIp hold time (from $\overline{SCKp}$↑) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			19		19		ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		483		483		483	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ				483		483	ns
SIp setup time (to $\overline{SCKp}$↓) Note 2	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	110		110		110		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			110		110		ns
SIp hold time (from $\overline{SCKp}$↓) Note 2	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			19		19		ns
Delay time from $\overline{SCKp}$↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ				25		25	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

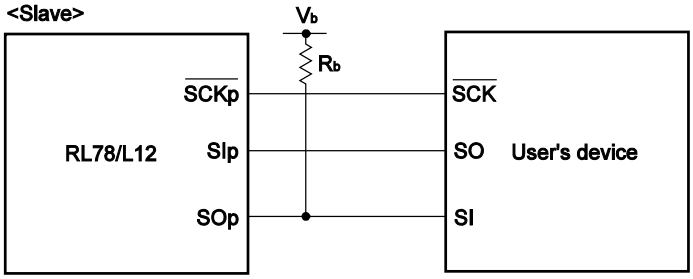
Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. Use it with $EV_{DD} \geq V_b$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

CSI mode connection diagram (during communication at different potential)

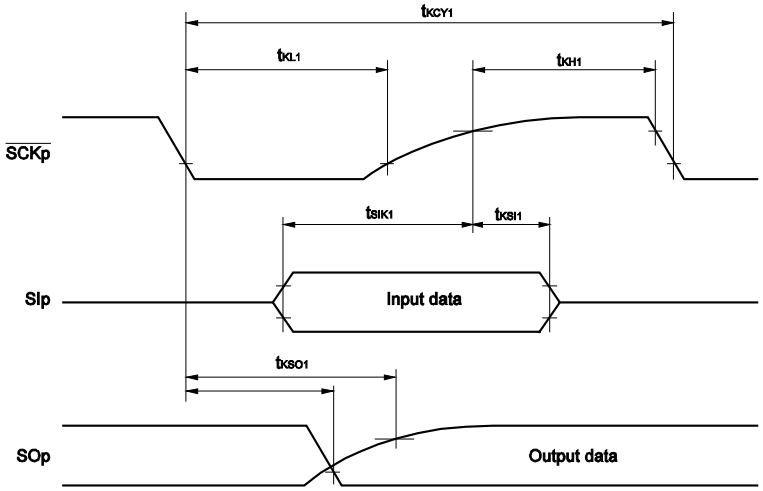


Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance, C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

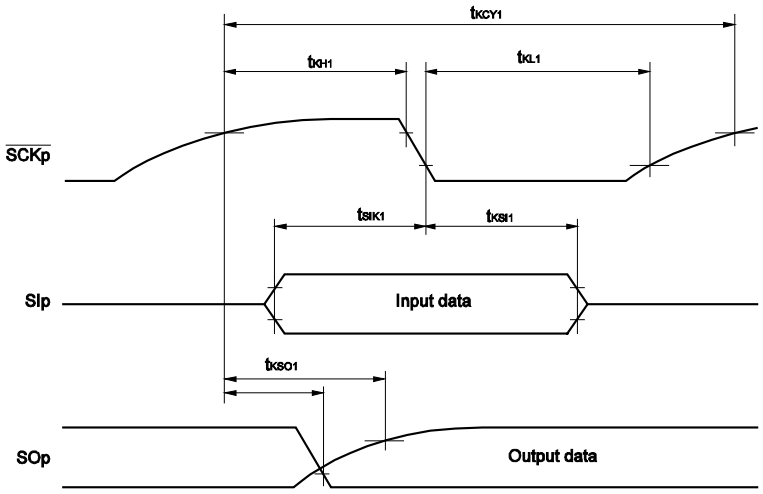
2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS(low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{SCKp}$ cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}						ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}						ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}				ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}						ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}						ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}						ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}				ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}						ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}						ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}						ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}				ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	4 MHz < f_{MCK} ≤ 8 MHz			16/f_{MCK}				ns
			f_{MCK} ≤ 4 MHz			10/f_{MCK}		10/f_{MCK}		ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 –12		t_{KCY2}/2 –50		t_{KCY2}/2 –50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 –18		t_{KCY2}/2 –50		t_{KCY2}/2 –50		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 –50		t_{KCY2}/2 –50		t_{KCY2}/2 –50		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2				t_{KCY2}/2 –50		t_{KCY2}/2 –50		ns
SIp setup time (to $\overline{SCKp}$↑) Note 3	t_{SIK2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		2.7 V ≤ EV_{DD} < 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2				1/f_{MCK} +30		1/f_{MCK} +30		ns
SIp hold time (from $\overline{SCKp}$↑) Note 3	t_{KSI2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		2.7 V ≤ EV_{DD} < 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2				1/f_{MCK} +31		1/f_{MCK} +31		ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 4	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} +120		2/f_{MCK} +573		2/f_{MCK} +573	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} +214		2/f_{MCK} +573		2/f_{MCK} +573	ns
		2.4 V ≤ EV_{DD} < 4.0 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} +573		2/f_{MCK} +573		2/f_{MCK} +573	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ					2/f_{MCK} +573		2/f_{MCK} +573	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

Notes 1. Transfer rate in the SNOOZE mode is MAX. 1 Mbps.

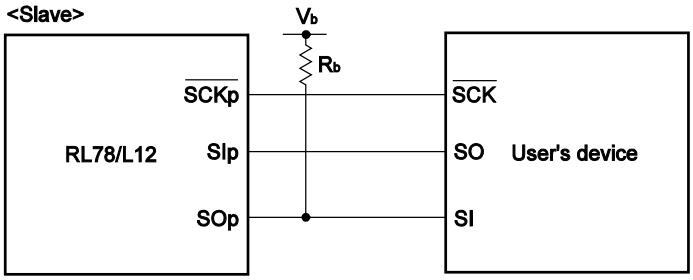
2. Use it with $EV_{DD} \geq V_b$.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time become "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and $\overline{SCKp}$ pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

CSI mode connection diagram (during communication at different potential)

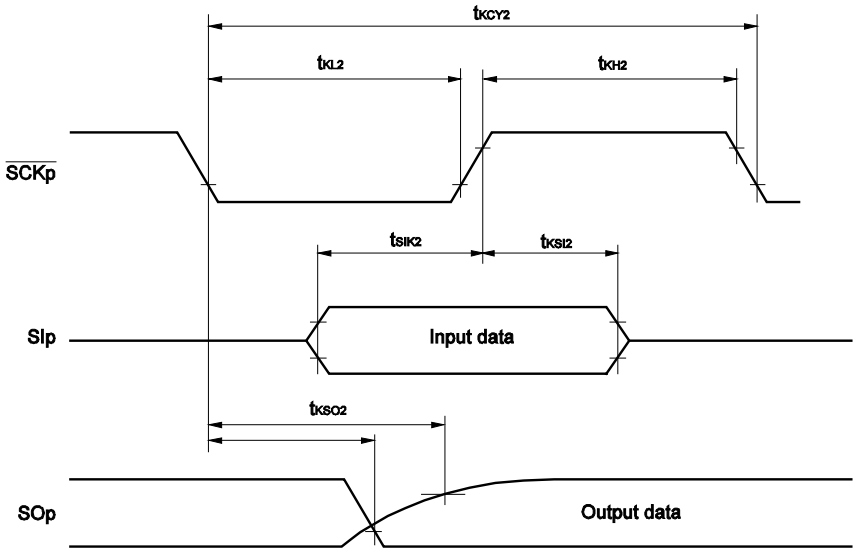


Remarks 1. R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

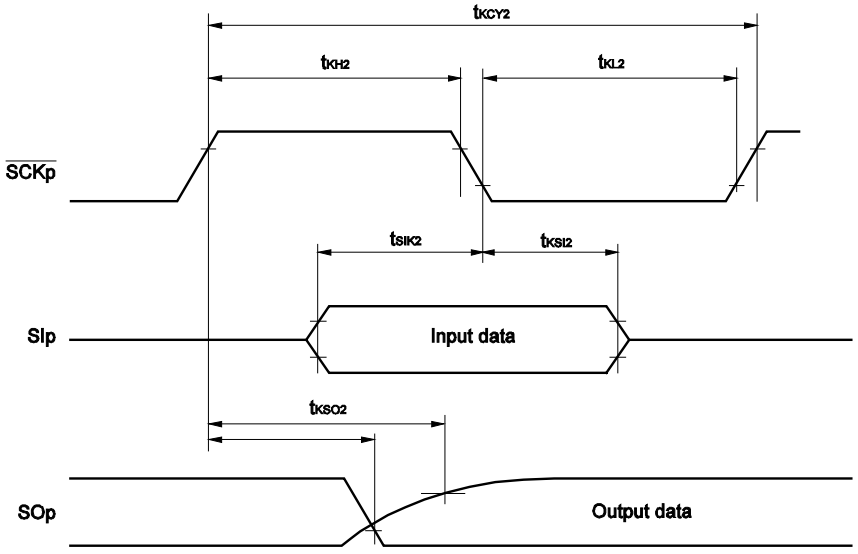
2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

30.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	kHz
			2.4 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	
			1.8 V ≤ EV_{DD} ≤ 5.5 V			0	100	0	100	
			1.6 V ≤ EV_{DD} ≤ 5.5 V					0	100	
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				4.7		4.7		
		1.6 V ≤ EV_{DD} ≤ 5.5 V						4.7		
Hold time [Note 1]	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				4.0		4.0		
		1.6 V ≤ EV_{DD} ≤ 5.5 V						4.0		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				4.7		4.7		
		1.6 V ≤ EV_{DD} ≤ 5.5 V						4.7		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				4.0		4.0		
		1.6 V ≤ EV_{DD} ≤ 5.5 V						4.0		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				250		250		
		1.6 V ≤ EV_{DD} ≤ 5.5 V						250		
Data hold time (transmission) [Note 2]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	
		1.8 V ≤ EV_{DD} ≤ 5.5 V				0	3.45	0	3.45	
		1.6 V ≤ EV_{DD} ≤ 5.5 V						0	3.45	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				4.0		4.0		
		1.6 V ≤ EV_{DD} ≤ 5.5 V						4.0		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				4.7		4.7		
		1.6 V ≤ EV_{DD} ≤ 5.5 V						4.7		

(**Note** and **Remark** are listed on the next page.)

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode (T_A = −40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	0	400	kHz
			2.4 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	0	400	
			1.8 V ≤ EV_{DD} ≤ 5.5 V			0	400	0	400	
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				0.6		0.6		
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				0.6		0.6		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				1.3		1.3		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				0.6		0.6		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		100		100		100		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		100		100		100		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				100		100		
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	
		1.8 V ≤ EV_{DD} ≤ 5.5 V				0	0.9	0	0.9	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				0.6		0.6		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		
		1.8 V ≤ EV_{DD} ≤ 5.5 V				1.3		1.3		

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I^2C fast mode plus (T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0	1000	−		−		kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.26		−		−		μs
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.26		−		−		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.5		−		−		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.26		−		−		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		50		−		−		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0	0.45	−		−		μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.26		−		−		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.5		−		−		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

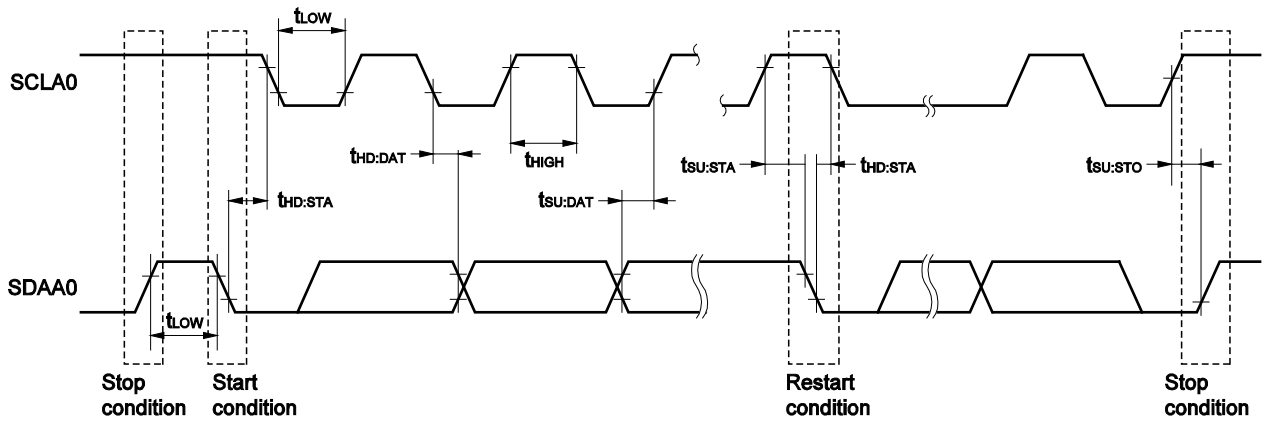
2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Caution When bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1, the above value can be applied. Make sure that the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, and V_{OL1}) satisfy the redirected values.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



30.6 Analog Characteristics

30.6.1 A/D converter characteristics

A/D converter characteristics column

Input channel/Reference voltage	Reference voltage (+) = AV_{REFP} Reference voltage (−) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (−) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (−) = AV_{REFM}
ANI0 to ANI1	–	Refer to 30.6.1 (3)	Refer to 30.6.1 (4)
ANI16 to ANI23	Refer to 30.6.1 (2)		
Internal reference voltage Temperature sensor output voltage	Refer to 30.6.1 (1)		–

(1) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target: internal reference voltage, temperature sensor output voltage

(T_A = –40 to +85°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution target: internal reference voltage output, temperature sensor output voltage, HS (high-speed main) mode	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]			±0.50	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]			±0.50	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]			±5.0	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 4]			±2.0	LSB
Analog input voltage	V_{AIN}	Internal reference voltage output 2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode		V_{BGR} [Note 5]			V
		Temperature sensor output voltage 2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode		V_{TMPS25} [Note 5]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} is smaller than V_{DD} (AV_{REFP} < V_{DD}), the MAX. values are as follows:
Overall error: Add or subtract 1.0 LSB to or from the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error or full-scale error: Add or subtract 0.05%FSR to or from the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error or differential linearity error: Add or subtract 0.5 LSB to or from the MAX. value when AV_{REFP} = V_{DD}.

4. These are values when setting the conversion time as 57 μs (MIN.) and 95μs (MAX.).

5. Refer to 30.6.2 Temperature sensor/internal reference voltage characteristics.

(2) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target: ANI16 to ANI23

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4		1.2	±8.5	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±2.5	LSB
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} is smaller than V_{DD} (AV_{REFP} < V_{DD}), the MAX. values are as follows:
   Overall error: Add or subtract 4.0 LSB to or from the MAX. value when AV_{REFP} = V_{DD}.
   Zero-scale error or full-scale error: Add or subtract 0.20%FSR to or from the MAX. value when AV_{REFP} = V_{DD}.
   Integral linearity error or differential linearity error: Add or subtract 2.0 LSB to or from the MAX. value when AV_{REFP} = V_{DD}.

4. These are values when setting the conversion time as 57 μs (MIN.) and 95μs (MAX.).

(3) When $AV_{REF(+)} = V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF(-)} = V_{SS}$ (ADREFM = 0), target: ANI0, ANI1, ANI16 to ANI23, internal reference voltage, temperature sensor output voltage

(T_A = –40 to +85°C, 1.6 V ≤ $EV_{DD} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS}$ = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±10.5	LSB
Conversion time	tCONV	10-bit resolution	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution target: internal reference voltage, temperature sensor output voltage HS (high-speed main) mode	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V Note 3			±6.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V Note 3			±2.5	LSB
Analog input voltage	VAIN	ANI0, ANI1		0		V_{DD}	V
		ANI16 to ANI23		0		EV_{DD}	V
		Internal reference voltage output, 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		V_{BGR} Note 4			V
		Temperature sensor output voltage, 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		V_{TMPS25} Note 4			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. These are values when setting the conversion time as 57 μs (MIN.) and 95μs (MAX.).

4. Refer to 30.6.2 Temperature sensor/internal reference voltage characteristics.

(4) When $AV_{REF(+)}$ = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target : ANI0, ANI16 to ANI23

(T_A = –40 to +85°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V) (HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 30.6.2 Temperature sensor/internal reference voltage characteristics.

4. When the reference voltage (–) = VSS, the MAX. values are as follows:

Zero-scale error: Add or subtract 0.35%FSR to or from the MAX. value when the reference voltage (–) = AV_{REFM}.

Integral linearity error: Add or subtract 0.5 LSB to or from the MAX. value when the reference voltage (–) = AV_{REFM}.

Integral linearity error or differential linearity error: Add or subtract 0.2 LSB to or from the MAX. value when the reference voltage (–) = AV_{REFM}.

30.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +85°C, 2.4 V ≤ = EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (HS (high-speed main) mode)

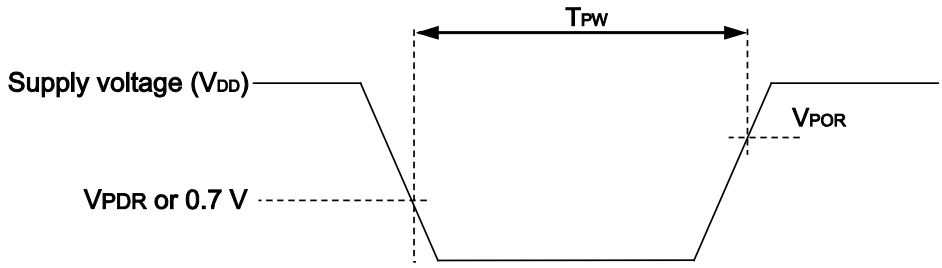
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

30.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width Note	T_{PW}		300			μs

Note: Minimum pulse width is required to power-on reset when V_{DD} is smaller than V_{PDR}. When RL78 microcontroller is in STOP mode, or the main system clock (f_{MAIN}) is stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC), the minimum pulse width is required to power-on reset from when V_{DD} falls below 0.7 V and until V_{DD} exceeds V_{POR}.



30.6.4 LVD circuit characteristics

(T_A = –40 to +85°C, $V_{PDR} \le EV_{DD} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDA0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0, falling reset voltage			1.60	1.63	1.66	V
	V_{LVDA1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVDA3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V_{LVDB1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V_{LVDC1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V_{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

30.6.5 Supply voltage rise time

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}				54	V/ms

Caution Make sure to retain an internal reset status by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range described in 30.4 AC Characteristics.

30.7 LCD Characteristics

30.7.1 Resistance division method

(1) Static display mode

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD} Note	V

Note 5.5 V (MAX.) when driving a memory-type liquid crystal (the MLCDEN bit of the MLCD register = 1).

30.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4[Note 1] = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4[Note 1] = 0.47 μF		2 V_{L1} −0.1	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4[Note 1] = 0.47 μF		3 V_{L1} −0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time[Note 2]	t_{VWAIT1}			5			ms
Voltage boost wait time[Note 3]	t_{VWAIT2}	C1 to C4[Note 1] = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 μF±30 %

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1} Note 4	C1 to C5 Note 1 = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 μF		2 V_{L1}–0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 μF		3 V_{L1}–0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4} Note 4	C1 to C5 Note 1 = 0.47 μF		4 V_{L1}–0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 μF±30 %

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

4. Make sure to set V_{L4} to 5.5 V or less.

30.7.3 Capacitor split method

1/3 bias method

(T_A = –40 to +85°C, 2.2 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 μF[Note 2]		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 μF[Note 2]	2/3 V_{L4} −0.1	2/3 V_{L4}	2/3 V_{L4} +0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 μF[Note 2]	1/3 V_{L4} −0.1	1/3 V_{L4}	1/3 V_{L4} +0.1	V
Capacitor split wait time[Note 1]	t_{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L4} and GND

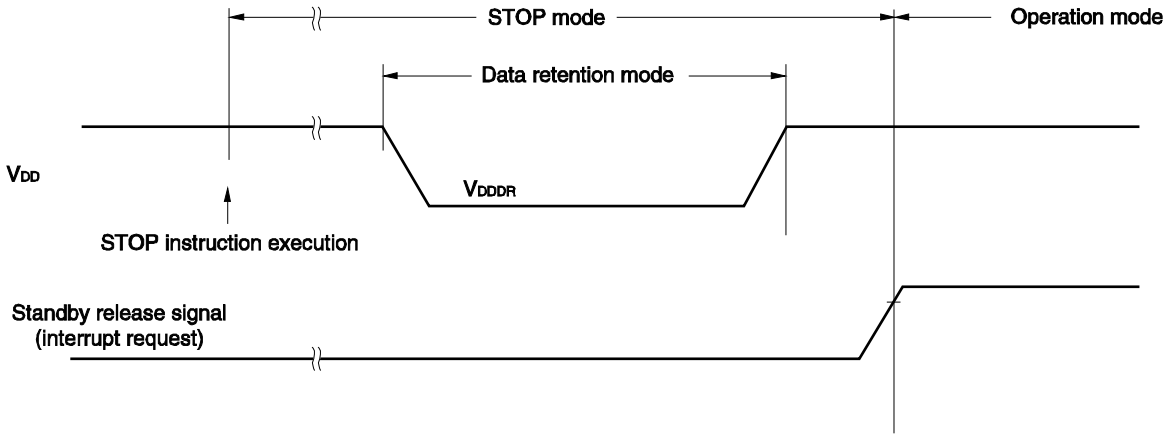
C1 = C2 = C3 = C4 = 0.47 μF ± 30 %

30.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



30.9 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years	T_A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year	T_A = 25°C		1,000,000		
		Retained for 5 years	T_A = 85°C	100,000			
		Retained for 20 years	T_A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.
2. When using flash memory programmer and Renesas Electronics self programming library
3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

30.10 Dedicated Flash Memory Programmer Communication (UART)

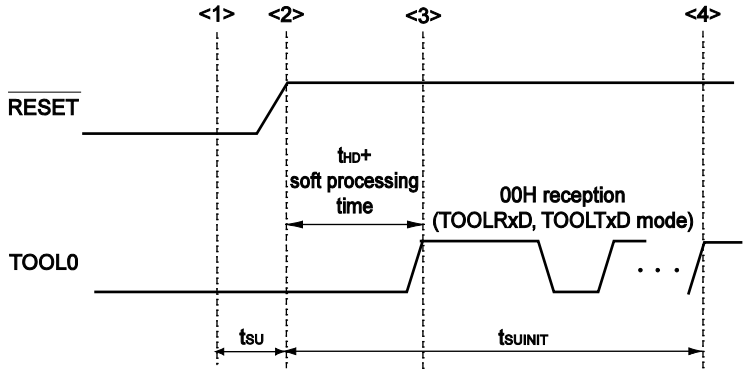
(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		When flash memory is programming	115,200		1,000,000	bps

30.11 Timing for Switching Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a pin reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the pin reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a pin reset ends	t_{SU}	POR and LVD reset must end before the pin reset ends.	10			μs
How long the TOOL0 pin is kept at the low level after an external reset ends (except flash memory firmware processing time)	t_{HD}	POR and LVD reset must end before the pin reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The pins reset ends. (POR and LVD reset must end before the pin reset ends.)

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and completion of the baud rate setting

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the reset ends.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends (MIN. 10 μs)

t_{HD}: How long the TOOL0 pin is kept at the low level after an external reset ends (except flash memory firmware processing time)

CHAPTER 31 ELECTRICAL SPECIFICATIONS

This chapter describes the electrical specifications for the products "G: Industrial applications (T_A = −40 to +105°C)".

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV_{DD}, or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.1.6 Pins for each product (pins other than port pins).

4. Please contact Renesas Electronics sales office for derating of operation under TA = +85°C to+105°C. Derating is the systematic reduction of load for the sake of improved reliability

There are following differences between the products "G: Industrial applications (T_A = −40 to +105°C)" and the products "A: Consumer applications or G: Industrial applications (T_A when using the RL78 microcontrollers at −40 to +85°C)".

Patameter	Application	
	A: Consumer applications, and G: Industrial applications (T_A when using RL78 at −40 to +85°C)	G: Industrial applications
Operating ambient temperature	T_A = −40 to +85°C	T_A = −40 to +105°C
Operation mode Operating voltage range	HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 24 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 4 MHz	HS (high-speed main) mode only: 2.7 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 24 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 16 MHz
High-speed on-chip osciilator clock accuracy	1.8 V ≤ V_{DD} ≤ 5.5 V ±1.0% @ T_A = −20 to +85ºC ±1.5% @ T_A = −40 to −20ºC 1.6 V ≤ V_{DD} ≤ 1.8 V ±5.0% @ T_A = −20 to +85ºC ±5.5% @ T_A = −40 to −20ºC	2.4 V ≤ V_{DD} ≤ 5.5 V ±2.0% @ T_A = +85 to +105ºC ±1.0% @ T_A = −20 to +85ºC ±1.5% @ T_A = −40 to −20ºC
Serial array unit	UART CSI00: f_{CLK}/2 (supporting 16 Mbps), f_{CLK}/4 CSI01 Simplified I^2C communication	UART CSI00: f_{CLK}/4 CSI01 Simplified I^2C communication
IICA	Standard mode Fast mode Fast mode plus	Standard mode Fast mode
Voltage detector	Rising detection voltage: 1.67 to 4.06 V (14 levels) Falling detection voltage: 1.63 to 3.98 V (14 levels)	Rising detection voltage: 2.61 to 4.06 V (8 levels) Falling detection voltage: 2.55 to 3.98 V (8 levels)

Remark: The electrical characteristics of the products “G: Industrial applications (T_A = −40 to +105°C)” are different from those of the products “A: Consumer applications (T_A = −40 to +85°C) or G: Industrial applications (T_A when using RL78 at −40 to +85°C)”. For details, refer to **31.1** to **31.10**.

31.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/3)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} = EV_{DD}	−0.5 to +6.5	V
	EV_{DD}	V_{DD} = EV_{DD}	−0.5 to +6.5	V
	EV_{SS}		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	**V_{I1}**	**P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127,P140 to P147**	**−0.3 to EV_{DD} +0.3 and −0.3 to V_{DD} +0.3 Note 2**	**V**
	V_{I2}	P60, P61 (N-ch open-drain)	−0.3 to EV_{DD} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{I3}	P20, P21, P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	−0.3 to EV_{DD} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	P20, P21	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI23	−0.3 to EV_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V
	V_{AI2}	ANI0, ANI1	−0.3 to V_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute **maximum rating of the REGC pin. Do not use this pin with voltage applied to it.**

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS} is the reference voltage.

Absolute Maximum Ratings (T_A = 25°C) (2/3)

Parameter	Symbols	Conditions			Ratings	Unit
LCD voltage	V_{L1}	V_{L1} voltage[Note 1]			−0.3 to +2.8 and −0.3 to V_{L4} +0.3	V
	V_{L2}	V_{L2} voltage[Note 1]			−0.3 to V_{L4} +0.3 [Note 2]	V
	V_{L3}	V_{L3} voltage[Note 1]			−0.3 to V_{L4} +0.3 [Note 2]	V
	V_{L4}	V_{L4} voltage[Note 1]			−0.3 to +6.5	V
	V_{LCAP}	CAPL, CAPH voltage[Note 1]			−0.3 to V_{L4} +0.3 [Note 2]	V
	V_{LOUT}	COM0 to COM7, SEG0 to SEG38, COMEXP output voltage	External resistance division	Other than memory-type liquid crystal mode	−0.3 to V_{DD} +0.3 [Note 2]	V
				Memory-type liquid crystal mode	−0.3 to V_{L4} +0.3 [Note 2]	
			Capacitor split		−0.3 to V_{DD} +0.3 [Note 2]	
			Internal voltage boosting		−0.3 to V_{L4} +0.3 [Note 2]	

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS} is the reference voltage.

Absolute Maximum Ratings (T_A = 25°C) (3/3)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	−70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	−100	mA
	I_{OH2}	Per pin	P20, P21	−0.5	mA
		Total of all pins		−1	mA
Output current, low	I_{OL1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
	I_{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

31.2 Oscillator Characteristics

31.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} ≤ 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only the permissible deviation of the oscillator frequencies. Refer to **AC Characteristics** for instruction execution time. Inquire with the resonator manufacturer to perform an evaluation on the actual circuit and check the oscillator characteristics before use.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 or XT1 oscillator, refer to **5.4 System Clock Oscillator**.

31.2.2 On-chip oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1		+1	%
		–40 to –20°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1.5		+1.5	%
		+85 to + 105°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for instruction execution time.

31.3 DC Characteristics

31.3.1 Pin characteristics

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				–3.0 Note 2	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–30.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–8.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			–4.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			–30.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			–15.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			–8.0	mA
		Total of all pins (When duty = 70% Note 3)				–60.0	mA
	I_{OH2}	P20, P21	Per pin			–0.1	mA
			Total of all pins 2.4 V ≤ V_{DD} ≤ 5.5 V			–0.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD}, EV_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA
Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≈ –8.7 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P10, P12, P15, P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147				8.5 Note 2	mA
		Per pin for P60, P61				15.0 Note 2	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			9.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 (When duty = 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty = 70% Note 3)				80.0	mA
	I_{OL2}	P20, P21	Per pin			0.4	mA
			Total of all pins	2.4 V ≤ V_{DD} ≤ 5.5 V		0.8	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS} and V_{SS} pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL input buffer 2.4 V ≤ EV_{DD} < 3.3 V	1.50		EV_{DD}	V
	V_{IH3}	P20, P21		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60, P61		0.7EV_{DD}		EV_{DD}	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV_{DD}	V
	V_{IL2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V ≤ EV_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20, P21		0		0.3V_{DD}	V
	V_{IL4}	P60, P61		0		0.3EV_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of P10, P12, P15, P17 is EV_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	EV_{DD}–0.7			V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –2.0 mA	EV_{DD}–0.6			V
			2.4 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	EV_{DD}–0.5			V
	V_{OH2}	P20, P21	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = –100 μA	V_{DD}–0.5			V
Output voltage, low	V_{OL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			2.4 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20, P21	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			2.4 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V

Caution P10, P12, P15, P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (5/5)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V_I = EV_{DD}				1	μA
	I_{LIH2}	P20, P21, P137, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V_I = EV_{SS}				−1	μA
	I_{LIL2}	P20, P21, P137, $\overline{\text{RESET}}$	V_I = V_{SS}				−1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
On-chip pull-up resistance	R_{U1}	V_I = EV_{SS}	SEGxx port					
			2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V		10	20	100	kΩ
	R_{U2}		Ports other than above (Except for P60, P61, and P130)		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

31.3.2 Supply current characteristics

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(1/3)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		mA
					Normal operation	V_{DD} = 5.0 V		3.3	5.3	mA
						V_{DD} = 3.0 V		3.3	5.3	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.5	3.9	mA
						V_{DD} = 3.0 V		2.5	3.9	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.8	4.7	mA
						Resonator connection		3.0	4.8	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.8	4.7	mA
						Resonator connection		3.0	4.8	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.8	2.8	mA
						Resonator connection		1.8	2.8	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.8	2.8	mA
						Resonator connection		1.8	2.8	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = –40°C	Normal operation	Square wave input		3.5	4.9	μA
						Resonator connection		3.6	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		3.6	4.9	μA
						Resonator connection		3.7	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		3.7	5.5	μA
						Resonator connection		3.8	5.6	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		3.8	6.3	μA
						Resonator connection		3.9	6.4	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		4.1	7.7	μA
						Resonator connection		4.2	7.8	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +105°C	Normal operation	Square wave input		6.4	19.7	μA
						Resonator connection		6.5	19.8	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash programming.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1), not including the current flowing into RTC, 12-bit interval timer, WDT, and LCD controller/driver.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(2/3)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.44	2.3	mA
					V_{DD} = 3.0 V		0.44	2.3	mA
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.40	1.7	mA
					V_{DD} = 3.0 V		0.40	1.7	mA
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.9	mA
					Resonator connection		0.45	2.0	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.9	mA
					Resonator connection		0.45	2.0	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = –40C	Square wave input		0.31	0.57	μA
					Resonator connection		0.50	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.37	0.57	μA
					Resonator connection		0.56	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.46	1.17	μA
					Resonator connection		0.65	1.36	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.57	1.97	μA
					Resonator connection		0.76	2.16	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		0.85	3.37	μA
					Resonator connection		1.04	3.56	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +105°C	Square wave input		3.04	15.37	μA
					Resonator connection		3.23	15.56	μA
	I_{DD3} Note 6	STOP mode Note 8	T_A = –40°C				0.17	0.50	μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.32	1.10	μA
			T_A = +70°C				0.43	1.90	μA
			T_A = +85°C				0.71	3.30	μA
			T_A = +105°C				2.90	15.30	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing to the A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, andthe current flowing during data flash programming.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When operating real-time clock (RTC) and setting ultra-low current consumption (AMPHS1 = 1), not including the current flowing to 12-bit interval timer, WDT, LCD controller/driver.

6. The current flowing into RTC, 12-bit interval timer, WDT are not included.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operatin current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{MAIN} is stopped			0.08		μA
12-bit inteval timer operating current	I_{IT} Notes 1, 2, 4				0.08		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.24		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 7				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8				2.50	12.20	mA
LCD operating current	I_{LCD1} Notes 11, 12	External resistance division method	V_{DD} = EV_{DD} = 5.0 V, V_{L4} = 5.0 V		0.04	0.2	μA
	I_{LCD2} Note 11	Internal voltage boosting method	V_{DD} = EV_{DD} = 5.0 V, V_{L4} = 5.1 V (VLCD = 12H)		1.12	3.7	μA
			V_{DD} = EV_{DD} = 3.0 V, V_{L4} = 3.0 V (VLCD = 04H)		0.63	2.2	μA
	I_{LCD3} Note 11	Capacitor split method	V_{DD} = EV_{DD} = 3.0 V, V_{L4} = 3.0 V		0.12	0.5	μA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	2.04	
		CSI/UART operation			0.70	1.54	

(**Note**, **Caution** and **Remark** are lisited on the next page)

Notes 1. Current flowing to the V_{DD}.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the RTC (not including the operating current of the low-speed on-chip oscillator and XT1 oscillator). The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, or I_{DD2} and I_{RTC} when RTC is operating in operation mode or HALT mode. Add I_{FIL} to the above value when using the low-speed on-chip oscillator. The operating current of the RTC is included when I_{DD2} operates with the subsystem clock.

4. Current flowing only to the 12-bit interval timer (not including the operating current of the low-speed on-chip oscillator and XT1 oscillator). The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, or I_{DD2} and I_{IT} when the 12-bit interval timer is operating in operation mode or HALT mode. Add I_{FIL} to the above value when using the low-speed on-chip oscillator.

5. Current flowing only to the WDT (including the operating current of the low-speed on-chip oscillator). The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, or I_{DD2} and I_{WDT} when the WDT is operating in operation mode or HALT mode. Add I_{FIL} to the above value when using the low-speed on-chip oscillator.

6. Current flowing only to the A/D converter. The supply current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter is operating in operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is operating.

8. Current flowing during data flash programming.

9. Current flowing during self-programming.

10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode.**

11. Current flowing only to the LCD controller/driver. The supply current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2} or I_{LCD3}) to the supply current (I_{DD1}, or I_{DD2}) when the LCD controller/driver is operating in operation mode or HALT mode. Not including the current that flows to the LCD panel.

The TYP. value and MAX. value are following conditions.

- When f_{SUB} is selected for system clock, LCD clock = 128 Hz (LCDC0 = 07H)
- 4-Time-Slice, 1/3 Bias Method

12. Not including the current that flows to the external divider resistor when the external resistance division method is used.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

31.4 AC Characteristics

31.4.1 Basic operation

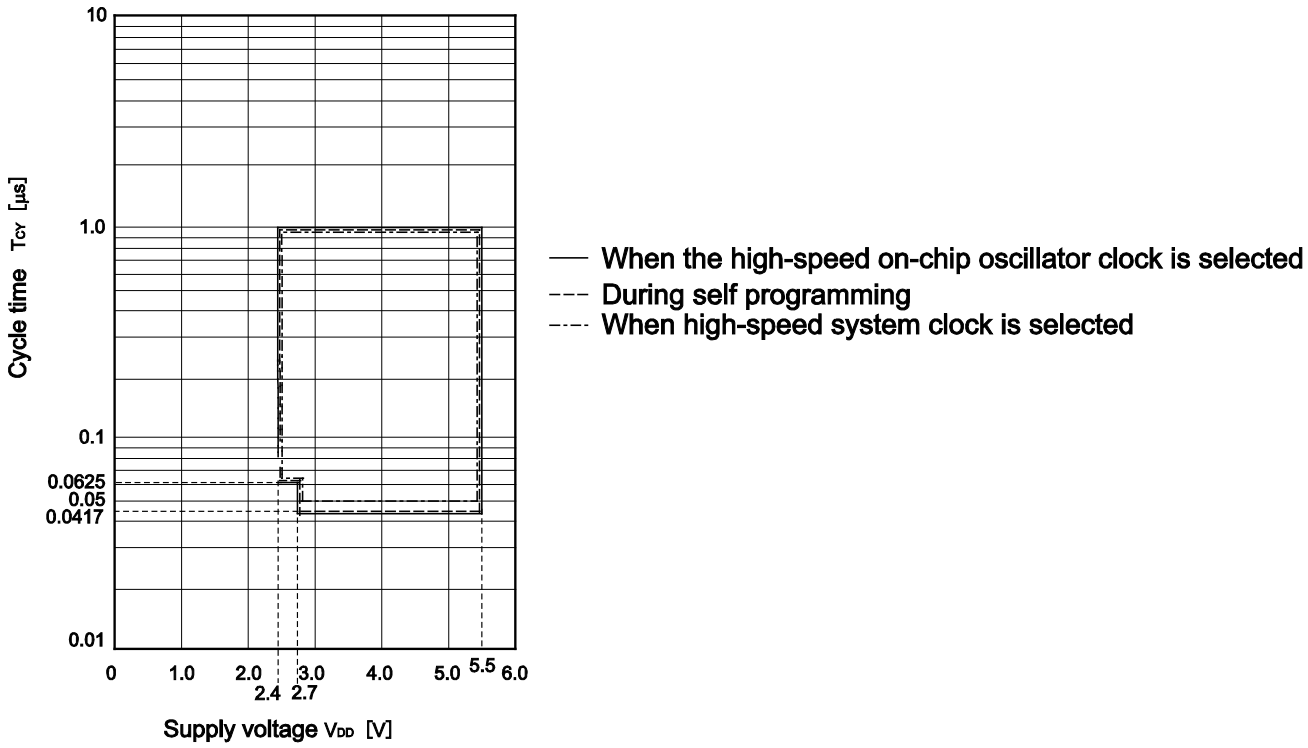
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f_{SUB}) operation		2.4 V ≤ V_{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16	MHz
	f_{EXS}				32		35	kHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns
TO00 to TO07 output frequency	f_{TO}	HS (high-speed main) mode		4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
				2.4 V ≤ EV_{DD} < 2.7 V			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
				2.4 V ≤ EV_{DD} < 2.7 V			4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0		2.4 V ≤ V_{DD} ≤ 5.5 V	1			μs
		INTP1 to INTP7		2.4 V ≤ EV_{DD} ≤ 5.5 V	1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR3		2.4 V ≤ EV_{DD} ≤ 5.5 V	250			ns
$\overline{RESET}$ low-level width	t_{RSL}				10			μs

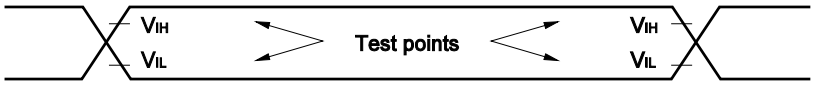
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

Minimum instruction executing time when the CPU is operating with the main system clock

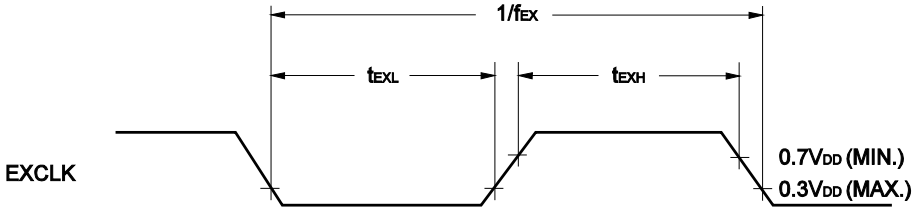
T_{CY} VS V_{DD} (HS, high-speed main mode)



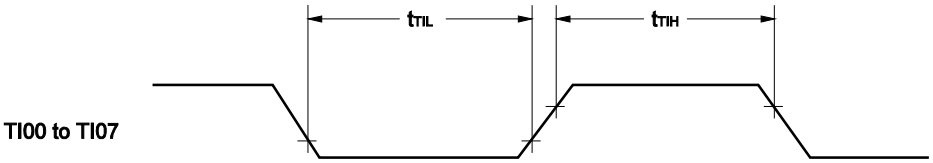
AC Timing Test Points

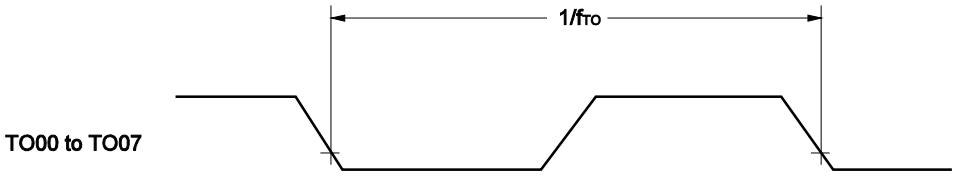


External System Clock Timing

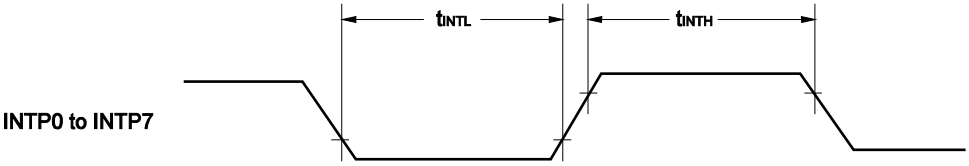


TI/TO Timing

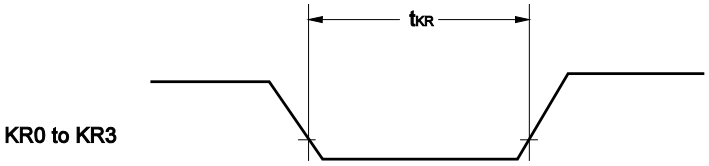




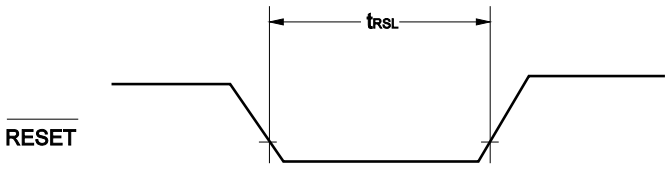
Interrupt Request Input Timing



Key Interrupt Input Timing

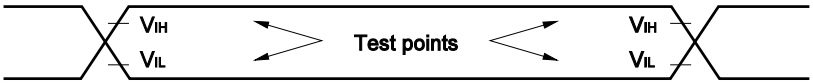


$\overline{\text{RESET}}$ Input Timing



31.5 Peripheral Functions Characteristics

AC Timing Test Points



31.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Transfer rate Note 1				f_{MCK}/12	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

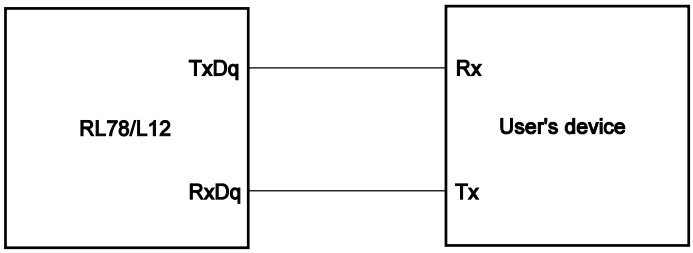
2. CPU/peripheral hardware clock (f_{CLK}) in each operating mode is as below.

HS (high-speed main) mode: f_{CLK} = 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

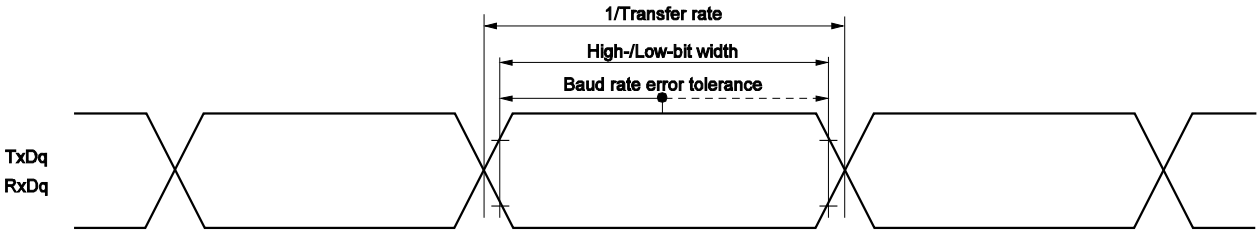
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0), g: PIM and POM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(2) During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$... internal clock output)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
$\overline{SCKp}$ cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 5.5 V		334 Note 1		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		500 Note 1		ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 –24		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 –36		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 –76		ns
SIp setup time (to $\overline{SCKp}$ ↑) Note 2	t_{SIK1}	2.7 V ≤ EV_{DD} ≤ 5.5 V		66		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		113		ns
SIp hold time (from $\overline{SCKp}$ ↑) Note 2	t_{KSI1}	2.4 V ≤ EV_{DD} ≤ 5.5 V		38		ns
Delay time from $\overline{SCKp}$ ↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	2.4 V ≤ EV_{DD} ≤ 5.5 V		50	ns

Notes 1. The value must also be equal to or more than 4/f_{MCK}.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time become "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
$\overline{\text{SCKp}}$ cycle time Note 4	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V	16 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 5.5 V		12/f_{MCK} and 1000		ns
$\overline{\text{SCKp}}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 –14		ns
		2.7 V ≤ EV_{DD} < 4.0 V		t_{KCY2}/2 –16		ns
		2.4 V ≤ EV_{DD} < 2.7 V		t_{KCY2}/2 –36		ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+40		ns
		2.4 V ≤ EV_{DD} < 2.7 V		1/f_{MCK}+60		
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 1	t_{KSI2}	2.4 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK}+62		ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	4.0 V ≤ EV_{DD} ≤ 5.5 V		2/f_{MCK}+66	ns
			2.7 V ≤ EV_{DD} < 4.0 V		2/f_{MCK}+66	ns
			2.4 V ≤ EV_{DD} < 2.7 V		2/f_{MCK}+113	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time become "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SOp output lines.

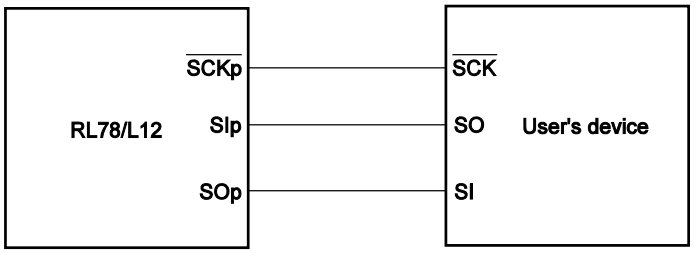
4. Transfer rate in the SNOOZE mode is MAX 1 Mbps.

Caution Select the normal input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

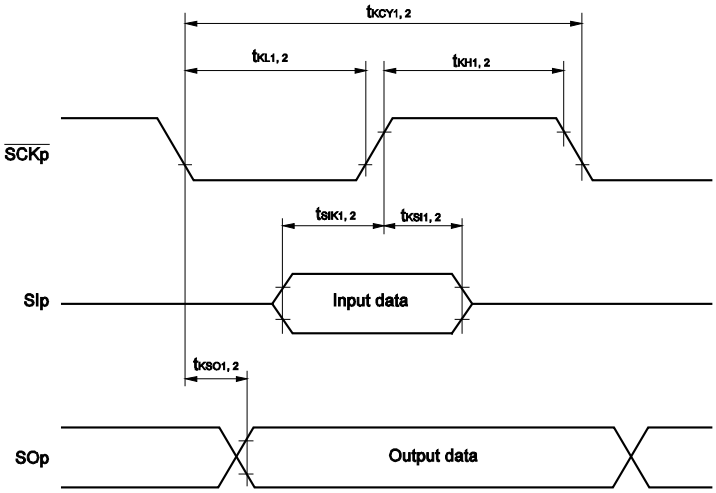
Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0),
n: Channel number (n = 0, 1), g: PIM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

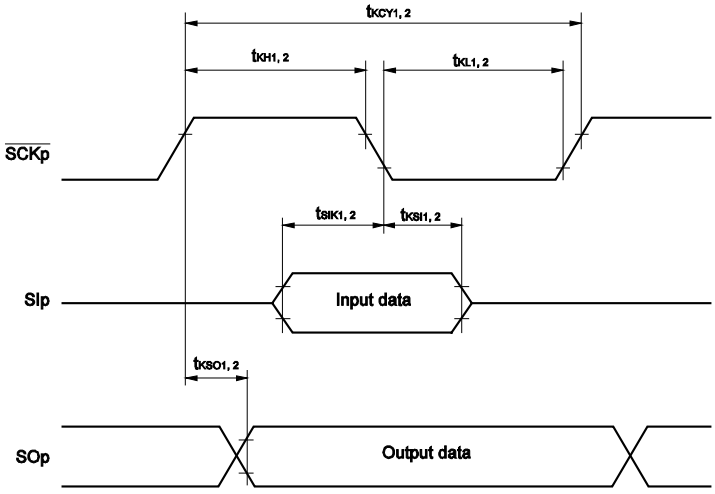
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01)

2. m: Unit number, n: Channel number (mn = 00, 01)

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) mode		Unit
					MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			f_{MCK}/12 Note 1	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			f_{MCK}/12 Note 1	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			f_{MCK}/12 Note 1	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		2.0	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. CPU/peripheral hardware clock (f_{CLK}) in each operating mode is as below.

HS (high-speed main) mode: f_{CLK} = 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) mode		Unit
					MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.0 Note 2	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ V_b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			**Note 5**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ V_b = 1.6 V		0.43 Note 6	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

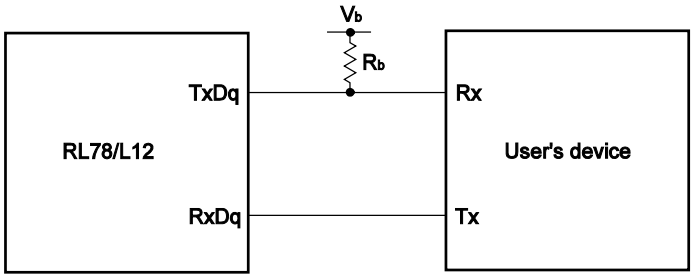
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

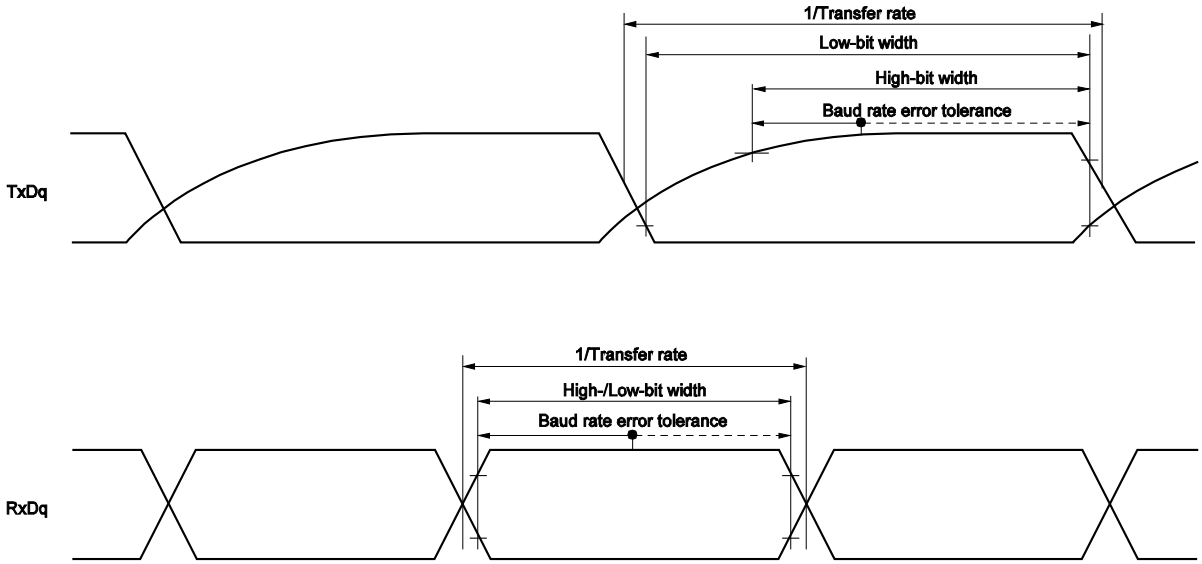
6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

2. q: UART number (q = 0), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
$\overline{SCKp}$ cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	600		ns
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	600		ns
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	2300		ns
$\overline{SCKp}$ high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 –150		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 –340		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 –916		ns
$\overline{SCKp}$ low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 –24		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 –36		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 –100		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SIp setup time (to $\overline{SCKp}$↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	162		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from $\overline{SCKp}$↑) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		200	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		966	ns
SIp setup time (to $\overline{SCKp}$↓) Note 2	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	88		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	88		ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	220		ns
SIp hold time (from $\overline{SCKp}$↓) Note 2	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
Delay time from $\overline{SCKp}$↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		50	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		50	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		50	ns

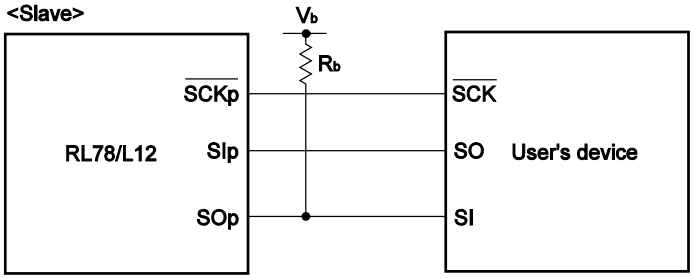
(**Note**, **Caution** and **Remark** are listed on the next page.)

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and $\overline{SCK}$p pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

CSI mode connection diagram (during communication at different potential)

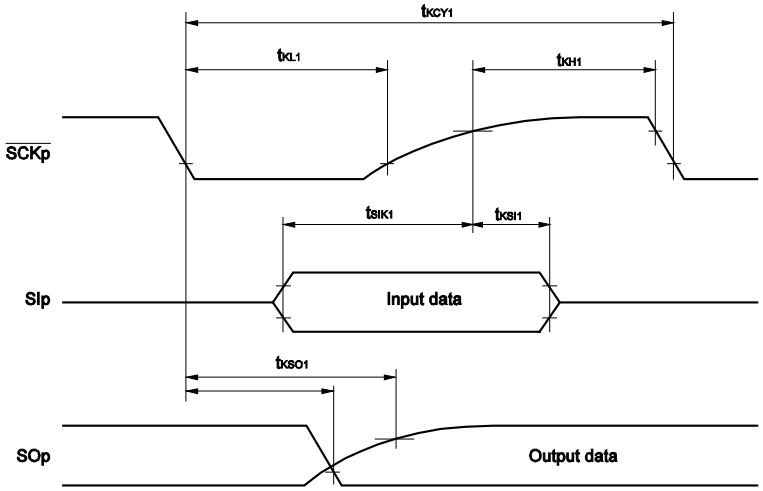


Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance, C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

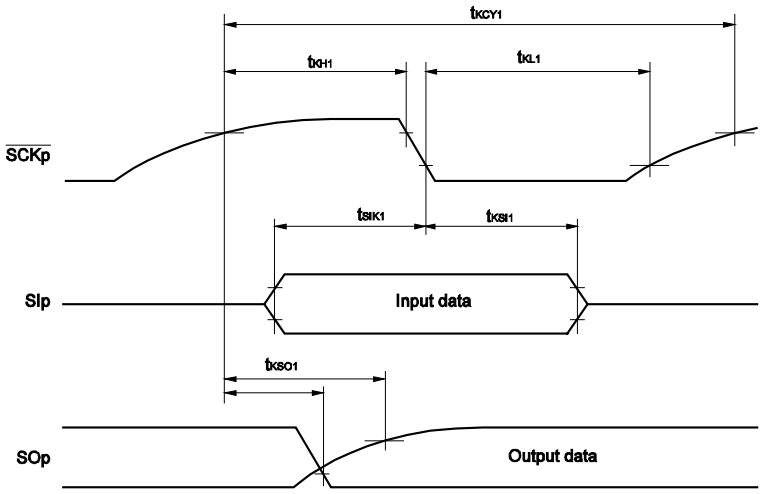
2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	24/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	20/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 −24		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 −36		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 −100		ns
SIp setup time (to SCKp↑) Note 2	t_{SIK2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} +40		ns
		2.7 V ≤ EV_{DD} < 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		1/f_{MCK} +40		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} +60		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} +62		ns
		2.7 V ≤ EV_{DD} < 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		1/f_{MCK} +62		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} +62		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} +240	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} +428	ns
		2.4 V ≤ EV_{DD} < 4.0 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} +1146	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

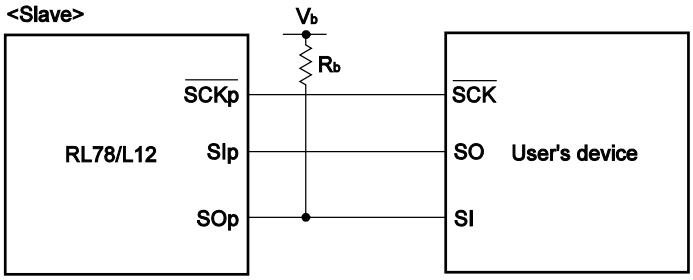
Notes 1. Transfer rate in the SNOOZE mode is MAX. 1 Mbps.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time or SIp hold time become "to $\overline{\text{SCK}}$p↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCK}}$p↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and $\overline{\text{SCK}}$p pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For details about V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is specified.

CSI mode connection diagram (during communication at different potential)

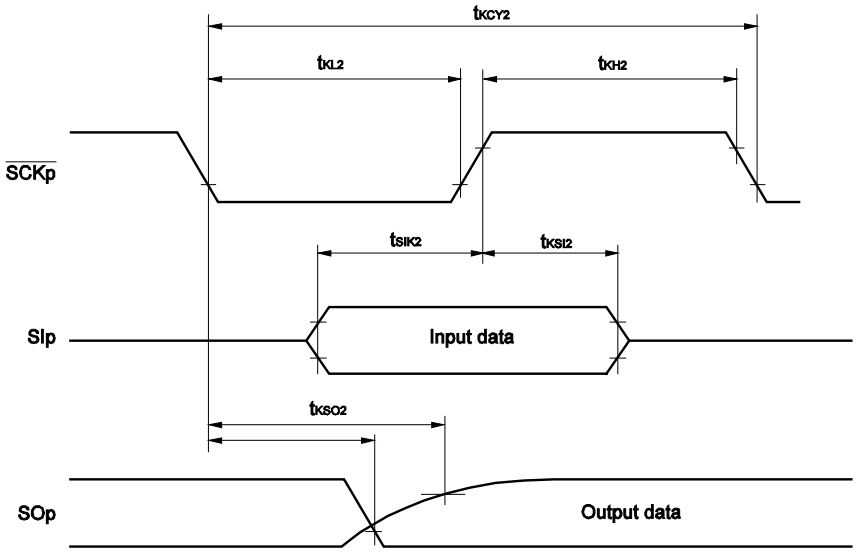


Remarks 1. R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

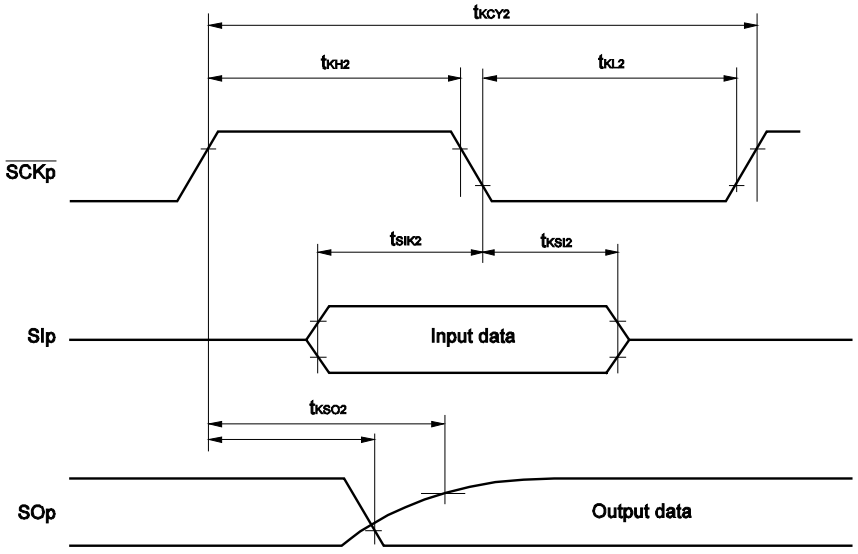
2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

31.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	100	kHz
			2.4 V ≤ EV_{DD} ≤ 5.5 V	0	100	
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.7		
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.0		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.7		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.0		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		250		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		250		
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.0		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		4.7		

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode (T_A = −40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	400	kHz
			2.4 V ≤ EV_{DD} ≤ 5.5 V	0	400	
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0.6		
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0.6		
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		1.3		
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0.6		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		100		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		100		
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		0.6		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V		1.3		

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

31.6 Analog Characteristics

31.6.1 A/D converter characteristics

A/D converter characteristics column

Input channel/Reference voltage	Reference voltage (+) = AV_{REFP} Reference voltage (−) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (−) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (−) = AV_{REFM}
ANI0 to ANI1	–	Refer to 31.6.1 (3)	Refer to 31.6.1 (4)
ANI16 to ANI23	Refer to 31.6.1 (2)		
Internal reference voltage Temperature sensor output voltage	Refer to 31.6.1 (1)		–

(1) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target: internal reference voltage, temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution target: internal reference voltage output, temperature sensor output voltage, HS (high-speed main) mode	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±1.5	LSB
Analog input voltage	V_{AIN}	Internal reference voltage output 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		V_{BGR} [Note 4]			V
		Temperature sensor output voltage 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		V_{TMPS25} [Note 4]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} is smaller than V_{DD} (AV_{REFP} < V_{DD}), the MAX. values are as follows;
Overall error: Add or subtract 1.0 LSB to or from the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error or full-scale error: Add or subtract 0.05%FSR to or from the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error or differential linearity error: Add or subtract 0.5 LSB to or from the MAX. value when AV_{REFP} = V_{DD}.

4. Refer to 31.6.2 Temperature sensor/internal reference voltage characteristics.

(2) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target: ANI16 to ANI23

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = E_{VDD} =V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI23		0		AV_{REFP} and EV_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} is smaller than V_{DD} (AV_{REFP} < V_{DD}), the MAX. values are as follows;
Overall error: Add or subtract 4.0 LSB to or from the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error or full-scale error: Add or subtract 0.20%FSR to or from the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error or differential linearity error: Add or subtract 2.0 LSB to or from the MAX. value when AV_{REFP} = V_{DD}.

(3) When $AV_{REF(+)} = V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF(-)} = V_{SS}$ (ADREFM = 0), target: ANI0, ANI1, ANI16 to ANI23, internal reference voltage, temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V ≤ $EV_{DD} = V_{DD} \leq$ 5.5 V, $V_{SS} = EV_{SS}$ = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution target: internal reference voltage, temperature sensor output voltage HS (high-speed main) mode	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	VAIN	ANI0, ANI1		0		V_{DD}	V
		ANI16 to ANI23		0		EV_{DD}	V
		Internal reference voltage output, 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		V_{BGR} Note 3			V
		Temperature sensor output voltage, 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		V_{TMPS25} Note 3			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 31.6.2 Temperature sensor/internal reference voltage characteristics.

(4) When $AV_{REF(+)}$ = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target : ANI0, ANI16 to ANI23

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V) (HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 31.6.2 Temperature sensor/internal reference voltage characteristics.

4. When the reference voltage (–) = VSS, the MAX. values are as follows;

Zero-scale error: Add or subtract 0.35%FSR to or from the MAX. value when the reference voltage (–) = AV_{REFM}.

Integral linearity error: Add or subtract 0.5 LSB to or from the MAX. value when the reference voltage (–) = AV_{REFM}.

Integral linearity error or differential linearity error: Add or subtract 0.2 LSB to or from the MAX. value when the reference voltage (–) = AV_{REFM}.

31.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +105°C, 2.4 V ≤ = EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (HS (high-speed main) mode)

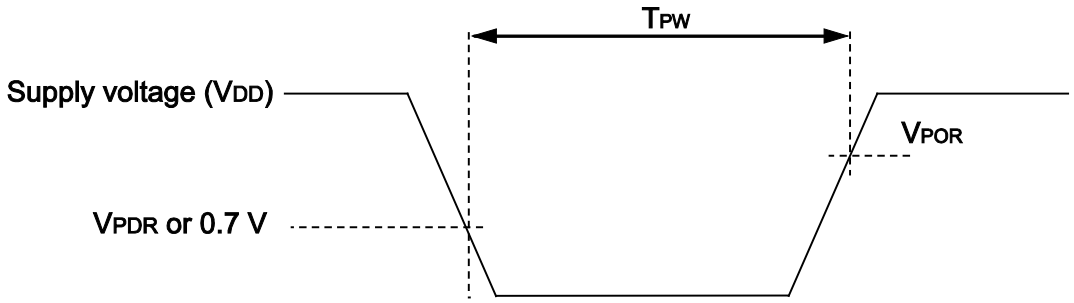
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

31.6.3 POR circuit characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width Note	T_{PW}		300			μs

Note: Minimum pulse width is required to power-on reset when V_{DD} is smaller than V_{PDR}. When RL78 microcontroller is in STOP mode, or the main system clock (f_{MAIN}) is stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC), the minimum pulse width is required to power-on reset from when V_{DD} falls below 0.7 V and until V_{DD} exceeds V_{POR}.



31.6.4 LVD circuit characteristics

(T_A = –40 to +105°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +105°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage			2.64	2.75	2.86	V
	V_{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
				Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
				Falling interrupt voltage	2.85	2.96	3.07	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
				Falling interrupt voltage	3.83	3.98	4.13	V

31.6.5 Supply voltage rise time

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}				54	V/ms

Caution Make sure to retain an internal reset status by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range described in 31.4 AC Characteristics.

31.7 LCD Characteristics

31.7.1 Resistance division method

(1) Static display mode

(T_A = –40 to +105°C, V_{L4} (MIN.) ≤ V_{DD} [Note] ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

Note Must be 2.4 V or higher.

(2) 1/2 bias method, 1/4 bias method

(T_A = –40 to +105°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

(T_A = –40 to +105°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}[Note]	V

Note 5.5 V (MAX.) when driving a memory-type liquid crystal (the MLCDEN bit of the MLCD register = 1).

31.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4[Note 1] = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4[Note 1] = 0.47 μF		2 V_{L1} −0.1	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4[Note 1] = 0.47 μF		3 V_{L1} −0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time[Note 2]	t_{VWAIT1}			5			ms
Voltage boost wait time[Note 3]	t_{VWAIT2}	C1 to C4[Note 1] = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 μF±30 %

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1} Note 4	C1 to C5 Note 1 = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 μF		2 V_{L1}–0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 μF		3 V_{L1}–0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4} Note 4	C1 to C5 Note 1 = 0.47 μF		4 V_{L1}–0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 μF±30 %

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

4. Make sure to set V_{L4} to 5.5 V or less.

31.7.3 Capacitor split method

1/3 bias method

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 μF[Note 2]		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 μF[Note 2]	2/3 V_{L4} −0.1	2/3 V_{L4}	2/3 V_{L4} +0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 μF[Note 2]	1/3 V_{L4} −0.1	1/3 V_{L4}	1/3 V_{L4} +0.1	V
Capacitor split wait time[Note 1]	t_{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L4} and GND

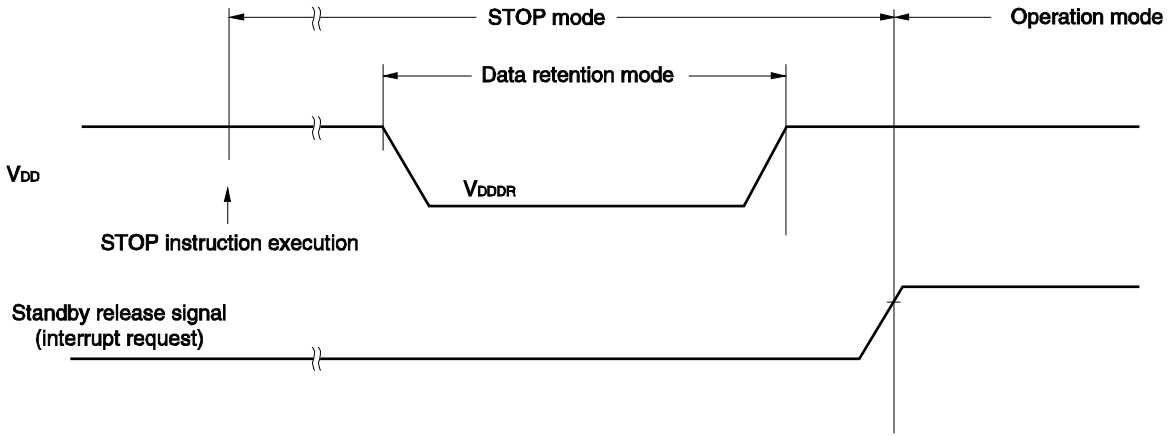
C1 = C2 = C3 = C4 = 0.47 μF ± 30 %

31.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



31.9 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years	T_A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year	T_A = 25°C		1,000,000		
		Retained for 5 years	T_A = 85°C	100,000			
		Retained for 20 years	T_A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.
2. When using flash memory programmer and Renesas Electronics self programming library
3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

31.10 Dedicated Flash Memory Programmer Communication (UART)

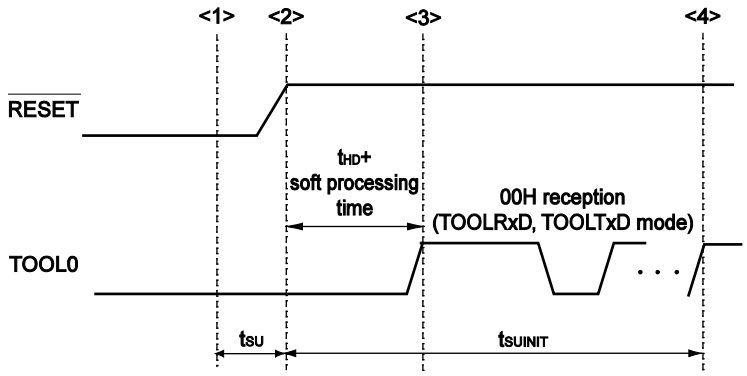
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		When flash memory is programming	115,200		1,000,000	bps

31.11 Timing for Switching Flash Memory Programming Modes

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a pin reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the pin reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a pin reset ends	t_{SU}	POR and LVD reset must end before the pin reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (except flash memory firmware processing time)	t_{HD}	POR and LVD reset must end before the pin reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The pins reset ends. (POR and LVD reset must end before the pin reset ends.)

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and completion of the baud rate setting

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the reset ends.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends (MIN. 10 μs)

t_{HD}: How long the TOOL0 pin is kept at the low level from after an external reset ends (except flash memory firmware processing time)