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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0140A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G24 Descriptions in the User's Manual: Hardware Rev. 1.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G24 Group	Lot No. All lots	Reference Document	RL78/G24 User's Manual: Hardware Rev. 1.10 R01UH0961EJ0110 (Nov. 2023)		

This document describes misstatements found in the RL78/G24 User's Manual: Hardware Rev. 1.10 (R01UH0961EJ0110).

Corrections

Applicable Item	Applicable Page	Contents
2.4 Block Diagrams of Pins	Page 89, Page 96, Page 102, Page 103, Page 104	Incorrect descriptions revised
20.3.9 Analog input channel specification register (ADS)	Page 1106	Incorrect descriptions revised
20.3.10 Analog input channel specification registers n for advanced mode (ADSn)	Page 1107	Incorrect descriptions revised
20.6.2 Software trigger no-wait mode (select mode, one-shot conversion mode)	Page 1120	Incorrect descriptions revised
24.3.8 Serial status registers mn (SSRmn) (mn = 00 to 03, 10, 11)	Page 1244	Incorrect descriptions revised
27.4.3 Repeat mode	Page 1594	Incorrect descriptions revised
29.4 Interrupt Servicing Operations	Page 1634, Page 1636	Incorrect descriptions revised
42.2 Operation List	Page 1840	Incorrect descriptions revised
43.2 Characteristics of the Oscillators	Page 1845	Incorrect descriptions revised
43.3.2 Supply current characteristics	Page 1856, Page 1859	Incorrect descriptions revised
44.2 Characteristics of the Oscillators	Page 1925	Incorrect descriptions revised
44.3.2 Supply current characteristics	Page 1934, Page 1937	Incorrect descriptions revised
44.4 AC Characteristics	Page 1942	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0961EJ0110	
1	3.1 Memory Space		Page 106, Page 107, Page 112	Page 3 to Page 5
2	20.3.3 A/D converter mode register 0 (ADM0)		Page 1071, Page 1075 to Page 1077, Page 1079, Page 1081, Page 1083, Page 1084, Page 1086, Page 1088, Page 1090, Page 1091, Page 1093	Page 6 to Page 18
3	20.3.4 A/D converter mode register 1 (ADM1)		Page 1096	Page 19
4	20.3.5 A/D converter mode register 2 (ADM2)		Page 1098, Page1099	Page 20, Page21
5	39.6.1 Self-programming procedure		Page 1760	Page 22
6	39.10.1 Overview of the data flash memory		Page 1811	Page 23
7	40.3 Security Settings for On-chip Debugging		Page 1814	Page 24
8	2.4 Block Diagrams of Pins		Page 89, Page 96, Page 102, Page 103, Page 104	Page 25 to Page 30
9	20.3.9 Analog input channel specification register (ADS)		Page 1106	Page 31
10	20.3.10 Analog input channel specification registers n for advanced mode (ADSn)		Page 1107	Page 32
11	20.6.2 Software trigger no-wait mode (select mode, one-shot conversion mode)		Page 1120	Page 33
12	24.3.8 Serial status registers mn (SSRmn) (mn = 00 to 03, 10, 11)		Page 1244	Page 34
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14	29.4 Interrupt Servicing Operations		Page 1634, Page 1636	Page 36, Page 37
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16	43.2 Characteristics of the Oscillators		Page 1845	Page 39
17	43.3.2 Supply current characteristics		Page 1856, Page 1859	Page 40, Page 41
18	44.2 Characteristics of the Oscillators		Page 1925	Page 42
19	44.3.2 Supply current characteristics		Page 1934, Page 1937	Page 43, Page 44
20	44.4 AC Characteristics		Page 1942	Page 45

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G24 Correction for incorrect description notice

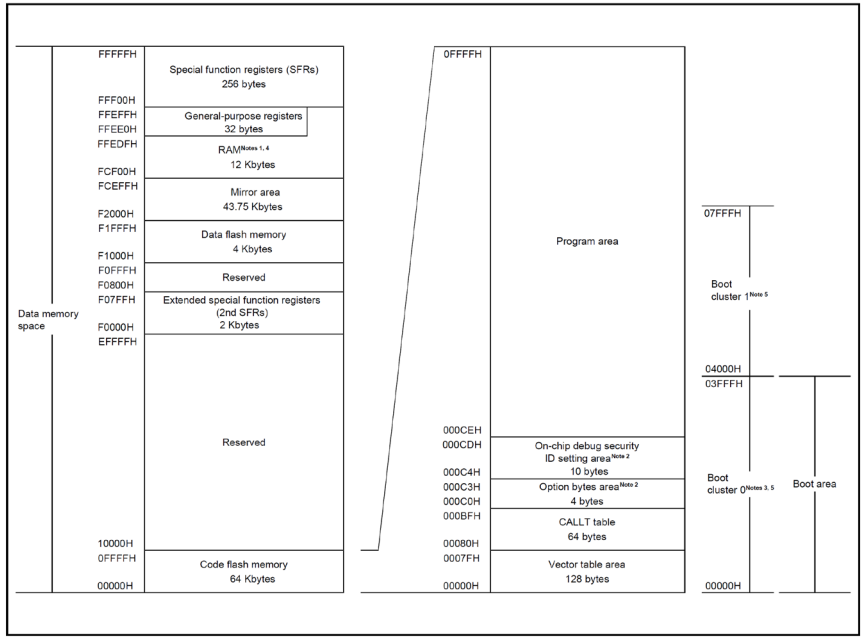
Document Number	Issue Date	Description
TN-RL*-A0135A/E	Apr. 26, 2024	First edition issued Corrections No.1 to No.7 revised
TN-RL*-A0140A/E	Jan. 8, 2025	Corrections No.8 to No.XX revised (this document)

1. Memory Space (Page 106, Page107, Page 112)

Incorrect:
(Page 106)

Products in the RL78/G24 can access a 1 MB address space. For details, see Figures 3 - 1 and 3 - 2.

Figure 3 - 1 Memory Map (R7F101GxE (x = 6, 7, 8, A, B, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

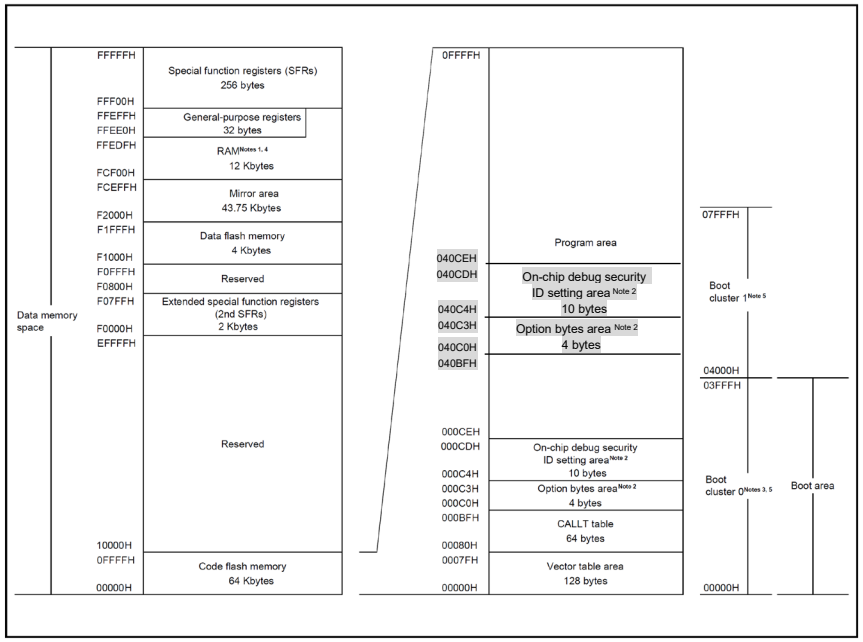
Note 2. **When boot swap is not used**: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Correct:

Products in the RL78/G24 can access a 1 MB address space. For details, see Figures 3 - 1 and 3 - 2.

Figure 3 - 1 Memory Map (R7F101GxE (x = 6, 7, 8, A, B, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

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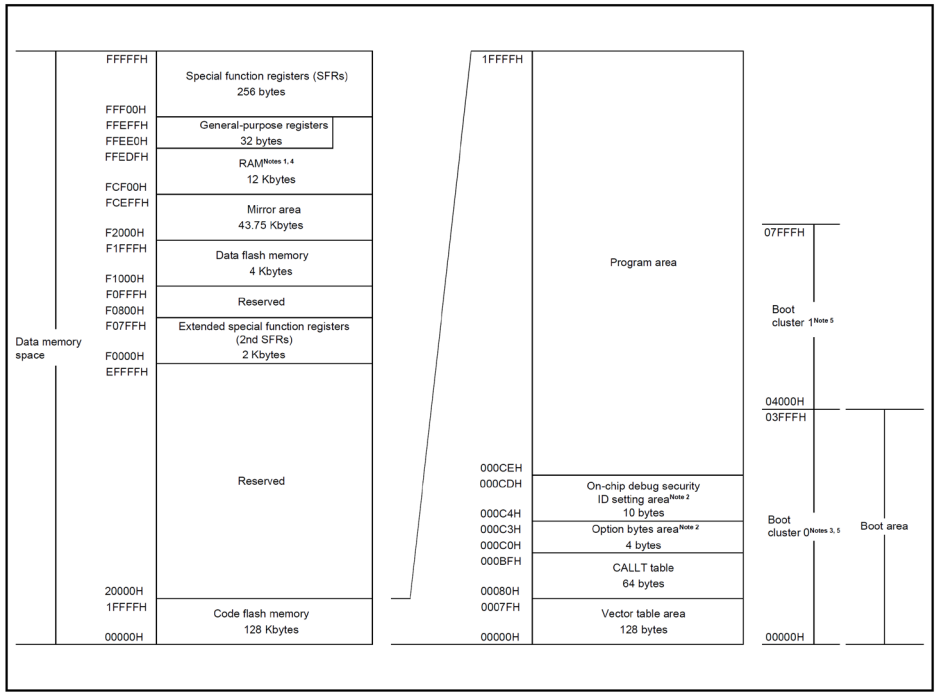
Figure 3 - 2 Memory Map (R7F101GxG (x = 6, 7, 8, A, B, E, F, G, J, L))

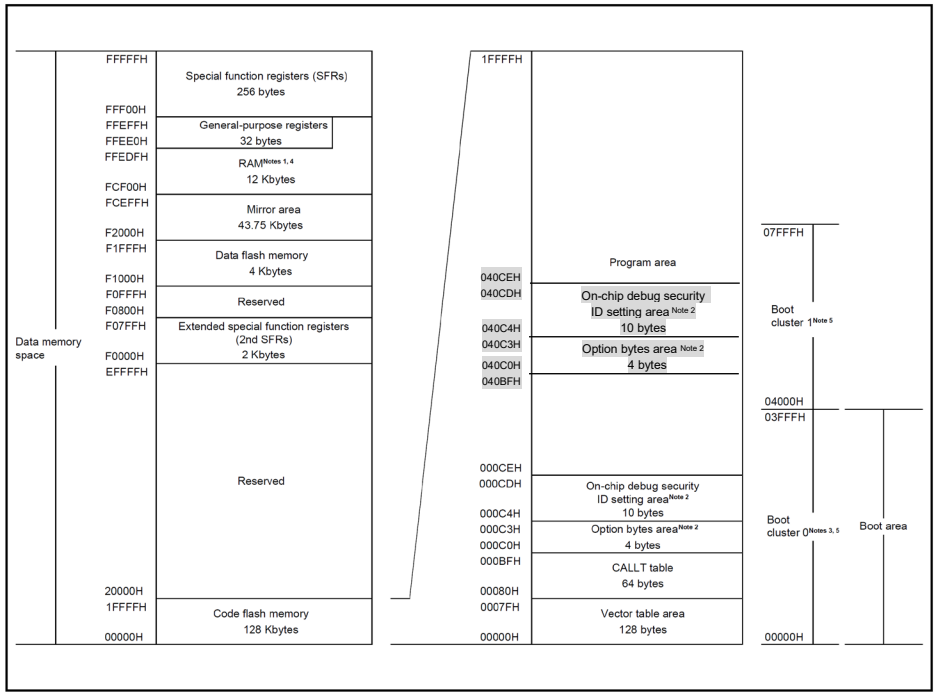


Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used**: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 2 Memory Map (R7F101GxG (x = 6, 7, 8, A, B, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 112)

(omitted)

3. Option bytes area
   A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when **the boot swap is used**. For details, see Section 38 Option Bytes.
4. On-chip debug security ID setting area
   A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when **the boot swap is not used** and at 000C4H to 000CDH and at 040C4H to 040CDH when **the boot swap is used**. For details, see Section 40 On-chip Debugging.

(omitted)

3. Option bytes area
   A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0. For details, see Section 38 Option Bytes.
4. On-chip debug security ID setting area
   A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. Set the 10-byte security ID for on-chip debugging at 000C4H to 000CDH when boot swapping is not to be used, that is, the value of the BTFLG bit in the FLSEC register is 1, and at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0. For details, see Section 40 On-chip Debugging.

2. 20.3.3 A/D converter mode register 0 (ADM0) (Page 1071, Page 1075 to Page1077, Page1079, Page 1081, Page 1083, Page 1084, Page 1086, Page 1088, Page 1090, Page 1091, Page 1093)

Incorrect:
(Page 1071)

Figure 20 - 4 Format of A/D Converter Mode Register 0 (ADM0)

(omitted)

ADCE	A/D voltage comparator operation control[Note 2]
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Note 1. For details of the FR[2:0] and LV[1:0] bits and A/D conversion, see Table 20 - 6 Selection of A/D Conversion Time.

Note 2. While in the software trigger no-wait mode or hardware trigger no-wait mode, the operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and it takes 1 μs + 2 cycles of the conversion clock (fAD) from the start of operation for the operation to stabilize. Therefore, immediately after the ADCS bit is set to 1 after at least 1 μs + 2 cycles of the conversion clock (fAD) have elapsed from the time ADCE bit is set to 1, the conversion result becomes valid. When ADCS is set to 1 while ADCE = 0, A/D conversion starts after the stabilization wait time has passed. If ADCS is set to 1 before at least 1 μs + 2 cycles of the conversion clock (fAD) have elapsed, ignore data of the first conversion.

Caution 1. Change the ADMD, FR[2:0], and LV[1:0] bits while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 2. Setting change from ADCS = 1 and ADCE = 1 to ADCS = 1 and ADCE = 0 is prohibited.

Caution 3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to follow the procedure described in 20.7 A/D Converter Setup Flowchart.

Caution 4. Do not set ADMS to 1 when the advanced mode is enabled.

Caution 5. Do not overwrite ADCS with 1 when the setting of ADCS is 1 in the advanced mode.

Caution 6. Do not overwrite ADCE with 1 when the setting of ADCE is 1 in the advanced mode.

Correct:

Figure 20 - 4 Format of A/D Converter Mode Register 0 (ADM0)

(omitted)

ADCE	A/D voltage comparator operation control[Note 2]
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Note 1. For details of the FR[2:0] and LV[1:0] bits and A/D conversion, see Table 20 - 6 Selection of A/D Conversion Time.

Note 2. While in the software trigger no-wait mode or hardware trigger no-wait mode, the operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and it takes 1 μs + 2 cycles of the conversion clock (fAD) from the start of operation for the operation to stabilize. Therefore, immediately after the ADCS bit is set to 1 after at least 1 μs + 2 cycles of the conversion clock (fAD) have elapsed from the time ADCE bit is set to 1, the conversion result becomes valid. When ADCS is set to 1 while ADCE = 0, A/D conversion starts after the stabilization wait time has passed. If ADCS is set to 1 before at least 1 μs + 2 cycles of the conversion clock (fAD) have elapsed, ignore data of the first conversion.

Caution 1. Change the ADMD, FR[2:0], and LV[1:0] bits while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 2. Setting change from ADCS = 1 and ADCE = 1 to ADCS = 1 and ADCE = 0 is prohibited.

Caution 3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to follow the procedure described in 20.7 A/D Converter Setup Flowchart.

Caution 4. Do not set ADMS to 1 when the advanced mode is enabled.

Caution 5. Do not overwrite ADCS with 1 when the setting of ADCS is 1 in the advanced mode.

Caution 6. Do not overwrite ADCE with 1 when the setting of ADCE is 1 in the advanced mode.

Caution 7. Following stoppage of conversion by setting the ADCS and ADCE bits to 0 from the conversion standby or conversion state, wait for at least 5 μs before restoring the values of the bits to 1. Note that, when changing the settings of bits ADMD, FR2 to FR0, LV1, and LV0, start by setting the ADCS and ADCE bits to 0, then wait for at least 0.2 μs before changing the rest of the bits.

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Caution 1. If using the hardware trigger wait mode, setting the ADCS bit to 1 is prohibited (but the bit is automatically switched to 1 when the hardware trigger signal is detected). However, it is possible to clear the ADCS bit to 0 to specify the A/D conversion standby state.

Caution 2. While in the one-shot conversion mode of the hardware trigger no-wait mode or advanced mode, the ADCS bit is not automatically cleared to 0 when A/D conversion ends. Instead, 1 is retained.

Caution 3. Only rewrite the value of the ADCE bit when ADCS = 0 (while in the conversion stopped/conversion standby state).

Caution 4. In advanced mode, three cycles of the fCLK clock are required from the occurrence of a trigger source until detection of the trigger. Table 20 - 5 lists the required numbers of clock cycles from the occurrence of a trigger or completion of the most recently executed conversion until A/D conversion starts in advanced mode.

Caution 5. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no-wait mode: 2 cycles of the fCLK clock + conversion start time + A/D conversion time

Hardware trigger wait mode: **2 cycles of the fCLK clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time**

Advanced mode: 3 cycles of the fCLK clock + conversion start time + A/D conversion time

(omitted)

Caution 1. If using the hardware trigger wait mode, setting the ADCS bit to 1 is prohibited (but the bit is automatically switched to 1 when the hardware trigger signal is detected). However, it is possible to clear the ADCS bit to 0 to specify the A/D conversion standby state.

Caution 2. While in the one-shot conversion mode of the hardware trigger no-wait mode or advanced mode, the ADCS bit is not automatically cleared to 0 when A/D conversion ends. Instead, 1 is retained.

Caution 3. Only rewrite the value of the ADCE bit when ADCS = 0 (while in the conversion stopped/conversion standby state).

Caution 4. In advanced mode, three cycles of the fCLK clock are required from the occurrence of a trigger source until detection of the trigger. Table 20 - 5 lists the required numbers of clock cycles from the occurrence of a trigger or completion of the most recently executed conversion until A/D conversion starts in advanced mode.

Caution 5. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no-wait mode: 2 cycles of the fCLK clock + conversion start time + A/D conversion time

Hardware trigger wait mode: 2 fCLK clock cycles + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 5µs

Advanced mode: 3 cycles of the fCLK clock + conversion start time + A/D conversion time

(omitted)

(Page 1076)

Table 20 - 6 Selection of A/D Conversion Time (1/11)

1. Normal modes 1 and 2 with no A/D power supply stabilization wait time
(software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	64 f_{AD}	1 f_{AD}	2112/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	66 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	64 f_{AD}	1 f_{AD}	1056/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	66 µs	33 µs
1	1	0	0				f_{CLK}/2	1 f_{AD}	181 f_{AD}	1 f_{AD}	366/f_{CLK}	Setting prohibited	91.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	1 f_{AD}	181 f_{AD}	1 f_{AD}	183/f_{CLK}	183 µs	45.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Caution 5. When the internal reference voltage is selected for the + side reference voltage, normal modes 1 and 2 cannot be used. In such cases, use low voltage mode 1 or 2.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

Table 20 - 6 Selection of A/D Conversion Time (1/11)

1. Normal modes 1 and 2 with no A/D power supply stabilization wait time
(software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	64 f_{AD}	1 f_{AD}	2112/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	66 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	64 f_{AD}	1 f_{AD}	1056/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	66 µs	33 µs
1	1	0	0				f_{CLK}/2	1 f_{AD}	181 f_{AD}	1 f_{AD}	366/f_{CLK}	Setting prohibited	91.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	1 f_{AD}	181 f_{AD}	1 f_{AD}	183/f_{CLK}	183 µs	45.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Caution 5. When the internal reference voltage is selected for the + side reference voltage, normal modes 1 and 2 cannot be used. In such cases, use low voltage mode 1 or 2.

Remark f_{CLK}: CPU/peripheral hardware clock frequency

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Table 20 - 6 Selection of A/D Conversion Time (2/11)

2. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	2624/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	1312/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	218/fCLK	Setting prohibited	54.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	109/fCLK	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

Table 20 - 6 Selection of A/D Conversion Time (2/11)

2. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	2624/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	1312/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	218/fCLK	Setting prohibited	54.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	109/fCLK	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

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Table 20 - 6 Selection of A/D Conversion Time (3/11)

3. Normal modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	2304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	72 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	1152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	72 µs	36 µs
1	1	0	0				f_{CLK}/2	4 f_{AD}	181 f_{AD}	4 f_{AD}	378/f_{CLK}	Setting prohibited	94.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	191/f_{CLK}	191 µs	47.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (1/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Table 20 - 6 Selection of A/D Conversion Time (3/11)

3. Normal modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	2304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	72 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	1152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	72 µs	36 µs
1	1	0	0				f_{CLK}/2	4 f_{AD}	181 f_{AD}	4 f_{AD}	378/f_{CLK}	Setting prohibited	94.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	191/f_{CLK}	191 µs	47.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (1/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

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Table 20 - 6 Selection of A/D Conversion Time (4/11)

4. Low voltage modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	4 f_{AD}	80 f_{AD}	4 f_{AD}	2816/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	88 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	80 f_{AD}	4 f_{AD}	1408/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	88 µs	44 µs
1	1	0	0				f_{CLK}/2	4 f_{AD}	107 f_{AD}	4 f_{AD}	230/f_{CLK}	Setting prohibited	57.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	107 f_{AD}	4 f_{AD}	117/f_{CLK}	117 µs	29.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (2/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Table 20 - 6 Selection of A/D Conversion Time (4/11)

4. Low voltage modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	4 f_{AD}	80 f_{AD}	4 f_{AD}	2816/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	88 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	80 f_{AD}	4 f_{AD}	1408/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	88 µs	44 µs
1	1	0	0				f_{CLK}/2	4 f_{AD}	107 f_{AD}	4 f_{AD}	230/f_{CLK}	Setting prohibited	57.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	107 f_{AD}	4 f_{AD}	117/f_{CLK}	117 µs	29.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (2/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Table 20 - 6 Selection of A/D Conversion Time (5/11)

5. Normal modes 1 and 2 with no A/D power supply stabilization wait time
(software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)										2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	0	0	Normal 1	fCLK/32	1 fAD	64 fAD	1 fAD	8256/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	258 µs
0	0	0	1				fCLK/16	1 fAD	64 fAD	1 fAD	4128/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	258 µs	129 µs
1	1	0	0				fCLK/2	1 fAD	181 fAD	1 fAD	1452/fCLK	Setting prohibited	363 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	181 fAD	1 fAD	726/fCLK	726 µs	181.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Caution 5. When the internal reference voltage is selected for the + side reference voltage, normal modes 1 and 2 cannot be used. In such cases, use low voltage mode 1 or 2.

Remark fCLK: CPU/peripheral hardware clock frequency

Table 20 - 6 Selection of A/D Conversion Time (5/11)

5. Normal modes 1 and 2 with no A/D power supply stabilization wait time
(software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)										2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	0	0	Normal 1	fCLK/32	1 fAD	64 fAD	1 fAD	8256/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	258 µs
0	0	0	1				fCLK/16	1 fAD	64 fAD	1 fAD	4128/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	258 µs	129 µs
1	1	0	0				fCLK/2	1 fAD	181 fAD	1 fAD	1452/fCLK	Setting prohibited	363 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	181 fAD	1 fAD	726/fCLK	726 µs	181.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Caution 5. When the internal reference voltage is selected for the + side reference voltage, normal modes 1 and 2 cannot be used. In such cases, use low voltage mode 1 or 2.

Remark fCLK: CPU/peripheral hardware clock frequency

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Table 20 - 6 Selection of A/D Conversion Time (6/11)

6. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	10304/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	322 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	5152/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	322 µs	161 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	860/fCLK	Setting prohibited	215 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	430/fCLK	430 µs	107.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

Table 20 - 6 Selection of A/D Conversion Time (6/11)

6. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	10304/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	322 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	5152/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	322 µs	161 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	860/fCLK	Setting prohibited	215 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	430/fCLK	430 µs	107.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

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Table 20 - 6 Selection of A/D Conversion Time (7/11)

7. Normal modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)										2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	$f_{CLK}/32$	4 f_{AD}	64 f_{AD}	4 f_{AD}	8448/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	264 µs
0	0	0	1				$f_{CLK}/16$	4 f_{AD}	64 f_{AD}	4 f_{AD}	4224/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	264 µs	132 µs
1	1	0	0				$f_{CLK}/2$	4 f_{AD}	181 f_{AD}	4 f_{AD}	1464/f_{CLK}	Setting prohibited	366 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	734/f_{CLK}	734 µs	183.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (1/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Table 20 - 6 Selection of A/D Conversion Time (7/11)

7. Normal modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)										2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0						f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	$f_{CLK}/32$	4 f_{AD}	64 f_{AD}	4 f_{AD}	8448/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	264 µs
0	0	0	1				$f_{CLK}/16$	4 f_{AD}	64 f_{AD}	4 f_{AD}	4224/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	264 µs	132 µs
1	1	0	0				$f_{CLK}/2$	4 f_{AD}	181 f_{AD}	4 f_{AD}	1464/f_{CLK}	Setting prohibited	366 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	734/f_{CLK}	734 µs	183.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (1/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (f_{AD}) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (t_{CONV}) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

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Table 20 - 6 Selection of A/D Conversion Time (8/11)

8. Low voltage modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	4 fAD	80 fAD	4 fAD	10496/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	328 µs
0	0	0	1				fCLK/16	4 fAD	80 fAD	4 fAD	5248/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	328 µs	164 µs
1	1	0	0				fCLK/2	4 fAD	107 fAD	4 fAD	872/fCLK	Setting prohibited	218 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	6 fAD	107 fAD	4 fAD	438/fCLK	438 µs	109.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (2/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (fAD) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (tCONV) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Table 20 - 6 Selection of A/D Conversion Time (8/11)

8. Low voltage modes 1 and 2 with A/D power supply stabilization wait time
(software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay[Note 2]	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	4 fAD	80 fAD	4 fAD	10496/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	328 µs
0	0	0	1				fCLK/16	4 fAD	80 fAD	4 fAD	5248/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	328 µs	164 µs
1	1	0	0				fCLK/2	4 fAD	107 fAD	4 fAD	872/fCLK	Setting prohibited	218 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	6 fAD	107 fAD	4 fAD	438/fCLK	438 µs	109.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected. For details, see Table 20 - 6 Selection of A/D Conversion Time (2/11).

Note 2. This number denotes the number of clock cycles for interrupt output delay in the one-shot conversion mode. When the sequential conversion mode is selected, the number of conversion clock (fAD) cycles becomes shorter by three cycles.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics. Note that the conversion time (tCONV) does not include A/D power supply stabilization wait time.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

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Table 20 - 6 Selection of A/D Conversion Time (9/11)

9. Normal mode 1 with no A/D power supply stabilization wait time (in advanced mode) when ANI0 to ANI7 are to be A/D converted

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion Note	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)						
(ADM1)	(ADM0)											2.4 V ≤ VDD ≤ 5.5 V					2.7 V ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz	fCLK = 48 MHz
0	0	0	0	0	0	Normal 1	fCLK/32	1 fAD	41 fAD	1 fAD	1376/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	43 μs	28.667 μs
0	0	0	1				fCLK/16	1 fAD	41 fAD	1 fAD	688/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	43 μs	21.5 μs	14.333 μs
1	1	0	0				fCLK/2	1 fAD	41 fAD	1 fAD	86/fCLK	Setting prohibited	21.5 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	41 fAD	1 fAD	43/fCLK	43 μs	10.75 μs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Note The listed value denotes the number of clock cycles for conversion when the setting of ADSPMOD[1:0] in the ADSPMODregister is 01B.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the simultaneous sampling is to proceed, the following conditions must be met.
ADLSP = 0, FR[2:0] = 100, LV[1:0] = 00, fCLK ≥ 32 MHz, VDD ≥ 2.7 V
ADLSP = 0, FR[2:0] = 101, LV[1:0] = 00, fCLK ≥ 16 MHz, VDD ≥ 2.7 V

Remark fCLK: CPU/peripheral hardware clock frequency

Table 20 - 6 Selection of A/D Conversion Time (9/11)

9. Normal mode 1 with no A/D power supply stabilization wait time (in advanced mode) when ANI0 to ANI7 are to be A/D converted

Note The listed value denotes the number of clock cycles for conversion when the setting of ADSPMOD[1:0] in the ADSPMODregister is 01B.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 μs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the simultaneous sampling is to proceed, the following conditions must be met.
ADLSP = 0, FR[2:0] = 100, LV[1:0] = 00, fCLK ≥ 32 MHz, VDD ≥ 2.7 V
ADLSP = 0, FR[2:0] = 101, LV[1:0] = 00, fCLK ≥ 16 MHz, VDD ≥ 2.7 V

Remark fCLK: CPU/peripheral hardware clock frequency

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Table 20 - 6 Selection of A/D Conversion Time (10/11)

10. Normal modes 1 and 2 with no A/D power supply stabilization wait time (in advanced mode) when ANI0 to ANI7, and ANI16 to ANI30 are to be A/D converted

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion Note	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)										2.4 V ≤ V_{DD} ≤ 5.5 V					2.7 V ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz	f_{CLK} = 48 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	48 f_{AD}	1 f_{AD}	1600/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	33.333 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	48 f_{AD}	1 f_{AD}	800/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	25 µs	16.667 µs
1	1	0	0				f_{CLK}/2	1 f_{AD}	261 f_{AD}	1 f_{AD}	526/f_{CLK}	Setting prohibited	131.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	1 f_{AD}	261 f_{AD}	1 f_{AD}	263/f_{CLK}	263 µs	65.75 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Note The listed value denotes the number of clock cycles for conversion when the setting of ADSPMOD[1:0] in the ADSPMOD register is 00B.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Table 20 - 6 Selection of A/D Conversion Time (10/11)

10. Normal modes 1 and 2 with no A/D power supply stabilization wait time (in advanced mode) when ANI0 to ANI7, and ANI16 to ANI30 are to be A/D converted

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion Note	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)										2.4 V ≤ V_{DD} ≤ 5.5 V					2.7 V ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz	f_{CLK} = 48 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	48 f_{AD}	1 f_{AD}	1600/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	33.333 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	48 f_{AD}	1 f_{AD}	800/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	50 µs	25 µs	16.667 µs
1	1	0	0				f_{CLK}/2	1 f_{AD}	261 f_{AD}	1 f_{AD}	526/f_{CLK}	Setting prohibited	131.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	1 f_{AD}	261 f_{AD}	1 f_{AD}	263/f_{CLK}	263 µs	65.75 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Note The listed value denotes the number of clock cycles for conversion when the setting of ADSPMOD[1:0] in the ADSPMOD register is 00B.

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use normal mode 2.

Table 20 - 6 Selection of A/D Conversion Time (11/11)

11. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (advanced mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz	fCLK = 48 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	2624/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	54.667 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	1312/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs	27.333 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	218/fCLK	Setting prohibited	54.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	109/fCLK	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

Table 20 - 6 Selection of A/D Conversion Time (11/11)

11. Low voltage modes 1 and 2 with no A/D power supply stabilization wait time (advanced mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (fAD)	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V	1.8 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V	2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							fCLK = 1 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz	fCLK = 32 MHz	fCLK = 48 MHz
0	0	0	0	1	0	Low voltage 1	fCLK/32	1 fAD	80 fAD	1 fAD	2624/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	54.667 µs
0	0	0	1				fCLK/16	1 fAD	80 fAD	1 fAD	1312/fCLK	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs	27.333 µs
1	1	0	0				fCLK/2	1 fAD	107 fAD	1 fAD	218/fCLK	Setting prohibited	54.5 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				fCLK	1 fAD	107 fAD	1 fAD	109/fCLK	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited										

Caution 1. The A/D conversion time must be within the relevant range of conversion clock (fAD) and conversion times (tCONV) described in 43.6.1 A/D converter characteristics or 44.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR[2:0] and LV[1:0] bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting the FR[2:0] and LV[1:0] bits.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. The conversion start time applies when no contention is present. For details on the conversion start time when contention is present, see Note 2 for Figure 20 - 5. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, use low voltage mode 2 with the conversion clock (fAD) with a frequency of no more than 16 MHz.

3. 20.3.4 A/D converter mode register 1 (ADM1) (p. 1096)

Incorrect:

(omitted)

Caution 1. Only rewrite the value of the ADM1 register while conversion operation is stopped (ADCS = 0, ADCE = 0).

Caution 2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no-wait mode: 2 cycles of the fCLK clock + conversion start time + A/D conversion time

Hardware trigger wait mode: **2 cycles of the fCLK clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time**

(omitted)

Correct:

(omitted)

Caution 1. Only rewrite the value of the ADM1 register while conversion operation is stopped (ADCS = 0, ADCE = 0).

Caution 2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no-wait mode: 2 cycles of the fCLK clock + conversion start time + A/D conversion time

Hardware trigger wait mode: 2 cycles of the fCLK clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 5μs

(omitted)

4. 20.3.5 A/D converter mode register 2 (ADM2) (Page 1098, Page 1099)

Incorrect:

(Page 1098)

(omitted)

Figure 20 - 8 Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	ADTYP1	ADTYP0

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AVREFP/ANI0
1	0	Supplied from the internal reference voltage Note 1
1	1	Discharged

• Use the following procedure to rewrite the ADREFP[1:0] bits.
<1> Set ADCE = 0.
<2> Set ADREFP[1:0] to 11B. This step is only necessary when the value of the ADREFP[1:0] bits is changed to 10B.
<3> Reference voltage discharge time: 1 µs
This step is only necessary when the value of the ADREFP[1:0] bits is changed to 10B.
<4> Change the value of the ADREFP[1:0] bit.
<5> Reference voltage stabilization wait time A
<6> Set ADCE = 1.
<7> Reference voltage stabilization wait time B
When the ADREFP[1:0] bits are set to 10B, A = 5 µs and B = 1 µs + 2 cycles of the conversion clock (fAD).
When the ADREFP[1:0] bits are set to 00B or 01B, **a wait A is not required** and B = 1 µs + 2 cycles of the conversion clock (fAD).
After <7> stabilization time, start the A/D conversion.
• When the ADREFP[1:0] bits are set to 10B, A/D conversion of the temperature sensor output voltage and internal reference voltage Note 1 cannot proceed.
Be sure to perform A/D conversion while ADISS = 0.

(omitted)

Correct:

(omitted)

Figure 20 - 8 Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	ADTYP1	ADTYP0

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from P20/AVREFP/ANI0
1	0	Supplied from the internal reference voltage Note 1
1	1	Discharged

• Use the following procedure to rewrite the ADREFP[1:0] bits.
<1> Set ADCE = 0.
<2> Wait for at least 0.2 us.
<3> Set ADREFP[1:0] to 11B. This step is only necessary when the value of the ADREFP[1:0] bits is changed to 10B.
<4> Reference voltage discharge time: 1 µs
This step is only necessary when the value of the ADREFP[1:0] bits is changed to 10B.
<5> Change the value of the ADREFP[1:0] bit.
<6> Reference voltage stabilization wait time A
<7> Set ADCE = 1.
<8> Reference voltage stabilization wait time B
When the ADREFP[1:0] bits are set to 10B, A = 5 µs and B = 1 µs + 2 cycles of the conversion clock (fAD).
When the ADREFP[1:0] bits are set to 00B or 01B, A = 4.8 µs and B = 1 µs + 2 cycles of the conversion clock (fAD).
After <8> stabilization time, start the A/D conversion.
• When the ADREFP[1:0] bits are set to 10B, A/D conversion of the temperature sensor output voltage and internal reference voltage Note 1 cannot proceed.
Be sure to perform A/D conversion while ADISS = 0.

(omitted)

(Page 1099)

(omitted)

AWC	Specification of the SNOOZE mode
0	Does not use the SNOOZE mode function
1	Uses the SNOOZE mode function.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

- The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (fCLK). If any other clock is selected, specifying this mode is prohibited.
- When using the SNOOZE mode function, set AWC to 0 in software trigger wait mode, and set AWC to 1 in hardware trigger wait mode.
- Using the SNOOZE mode function in the software trigger no-wait mode, hardware trigger no-wait mode, or advanced mode is prohibited.
- Using the SNOOZE mode function in hardware trigger wait mode in sequential conversion mode is prohibited.
- When using the SNOOZE mode function, specify a hardware trigger interval of at least **"transition time to SNOOZE mode[Note 2] + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 2 cycles of the fCLK clock".**
- Even when using the SNOOZE mode, be sure to set the AWC bit to 0 in normal operation and change it to 1 just before shifting to STOP mode. Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation. If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE mode or normal operation.

(omitted)

(omitted)

AWC	Specification of the SNOOZE mode
0	Does not use the SNOOZE mode function
1	Uses the SNOOZE mode function.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

- The SNOOZE mode function can only be specified when the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (fCLK). If any other clock is selected, specifying this mode is prohibited.
- When using the SNOOZE mode function, set AWC to 0 in software trigger wait mode, and set AWC to 1 in hardware trigger wait mode.
- Using the SNOOZE mode function in the software trigger no-wait mode, hardware trigger no-wait mode, or advanced mode is prohibited.
- Using the SNOOZE mode function in hardware trigger wait mode in sequential conversion mode is prohibited.
- When using the SNOOZE mode function, specify a hardware trigger interval of at least "transition time to SNOOZE mode[Note 2] + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 2 cycles of the fCLK clock + 5us".
- Even when using the SNOOZE mode, be sure to set the AWC bit to 0 in normal operation and change it to 1 just before shifting to STOP mode. Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation. If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE mode or normal operation.

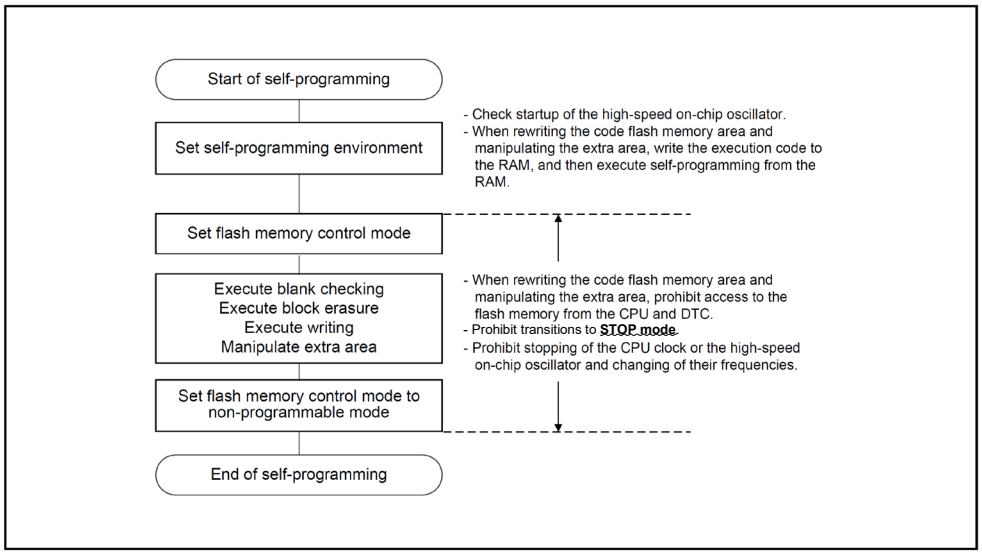
(omitted)

5. 39.6.1 Self-programming procedure (Page 1760)

Incorrect:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 39.6.2 Registers to control the flash memory.

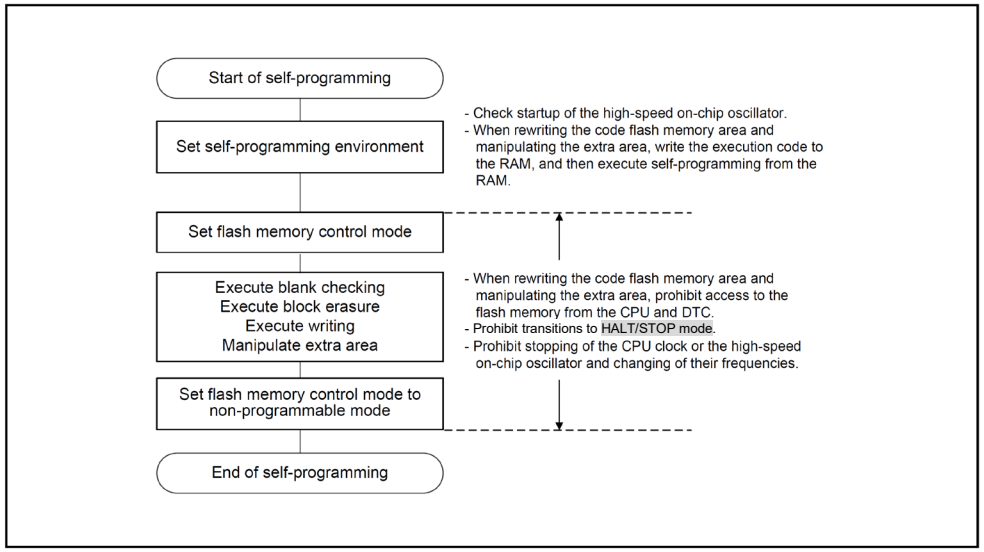
Figure 39 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



Correct:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 39.6.2 Registers to control the flash memory.

Figure 39 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



6. 39.10.1 Overview of the data flash memory (Page 1811)

Incorrect:

An overview of the data flash memory is provided below.

(omitted)

• Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.

• Transition to the **STOP mode** is prohibited while rewriting the data flash memory.

Correct:

An overview of the data flash memory is provided below.

(omitted)

• Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.

• Transition to the HALT/STOP mode is prohibited while rewriting the data flash memory.

7. 40.3 Security Settings for On-chip Debugging (Page 1814)

Incorrect:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 39.9 Security Settings).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 38 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.Note

Note The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.

Table 40 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID codeNote
040C4H to 040CDH	

Note. The setting FFFFFFFFFFFFFFFFFFFFH is not allowed.

Correct:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 39.9 Security Settings).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 38 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.Note

Note The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.

Table 40 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID codeNote 1, 2
040C4H to 040CDH	

Note 1. The setting FFFFFFFFFFFFFFFFFFFFH is not allowed.

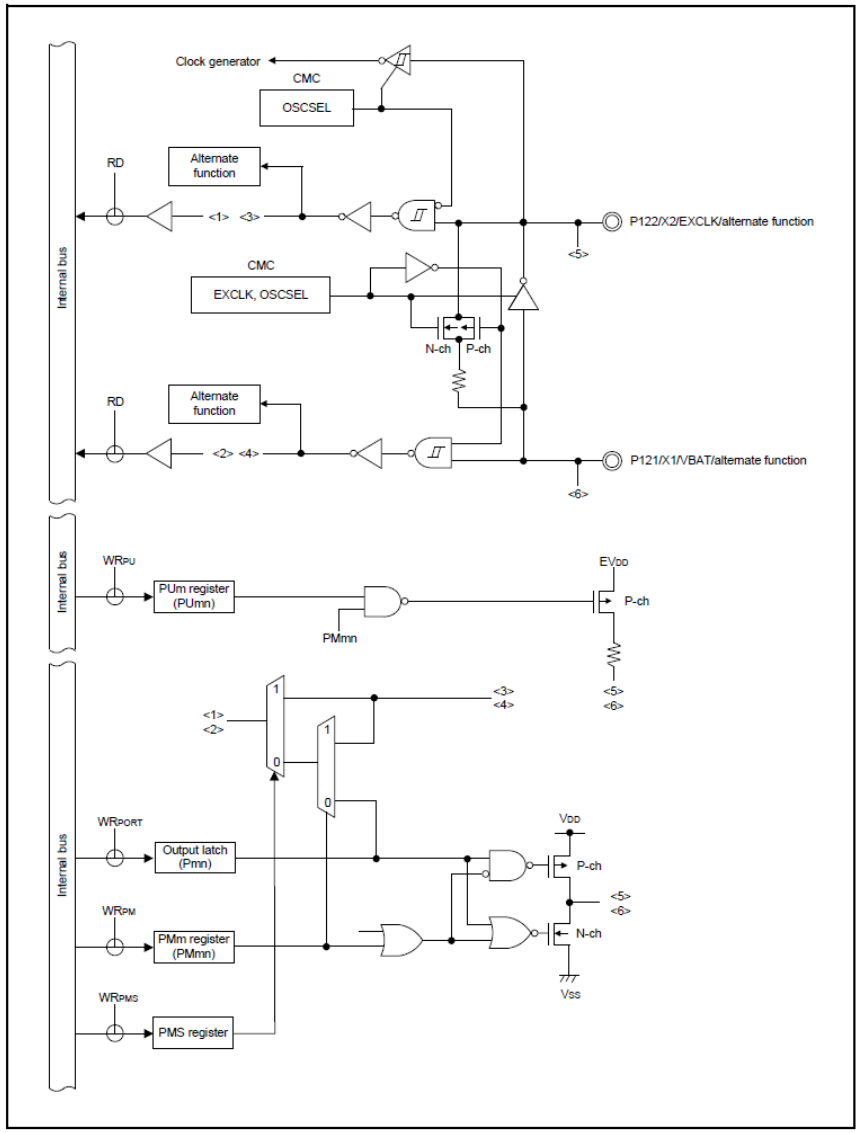
Note 2. Set the 10-byte security ID for on-chip debugging at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0.

8. **2.4 Block Diagrams of Pins (Page 89, Page 96, Page 102, Page 103, Page 104)**

Incorrect:

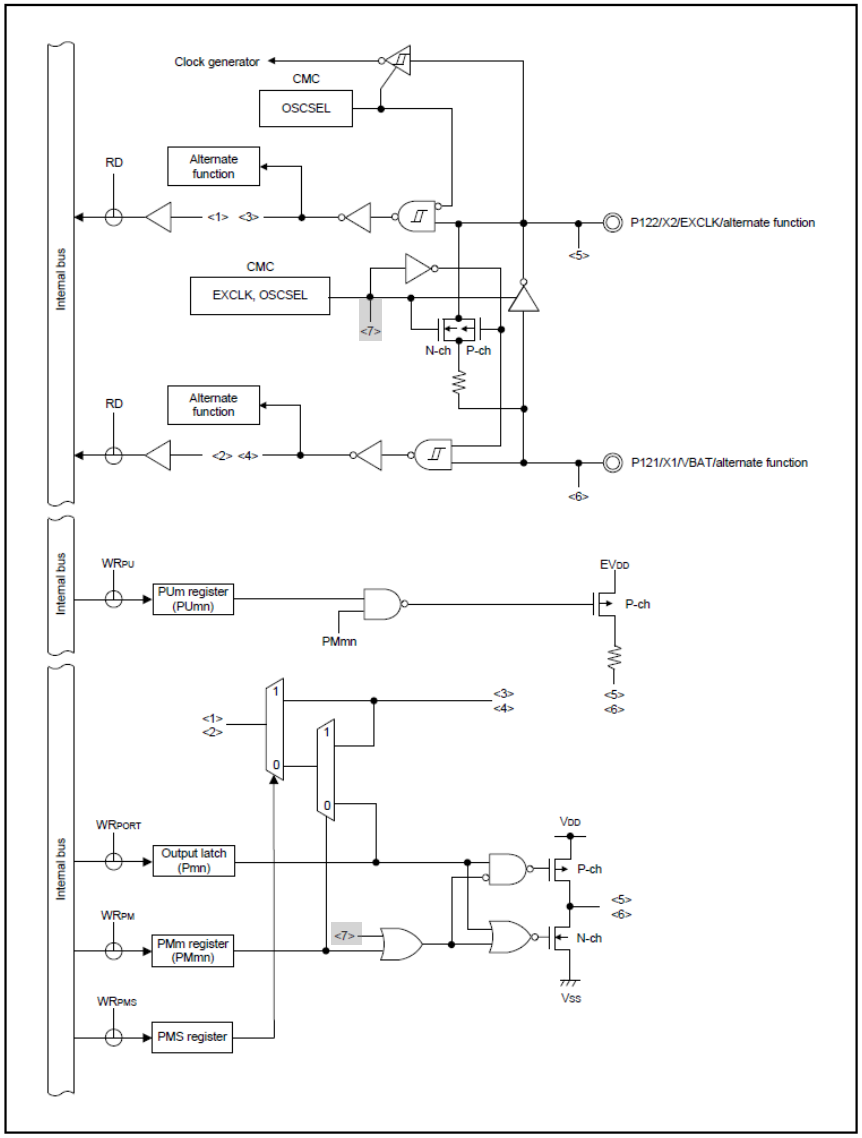
(Page 89)

Figure 2 - 13 Pin Block Diagram for Pin Type 7-2-1



Correct:

Figure 2 - 13 Pin Block Diagram for Pin Type 7-2-1



(Page 96)

Figure 2 - 20 Pin Block Diagram for Pin Type 7-38-3

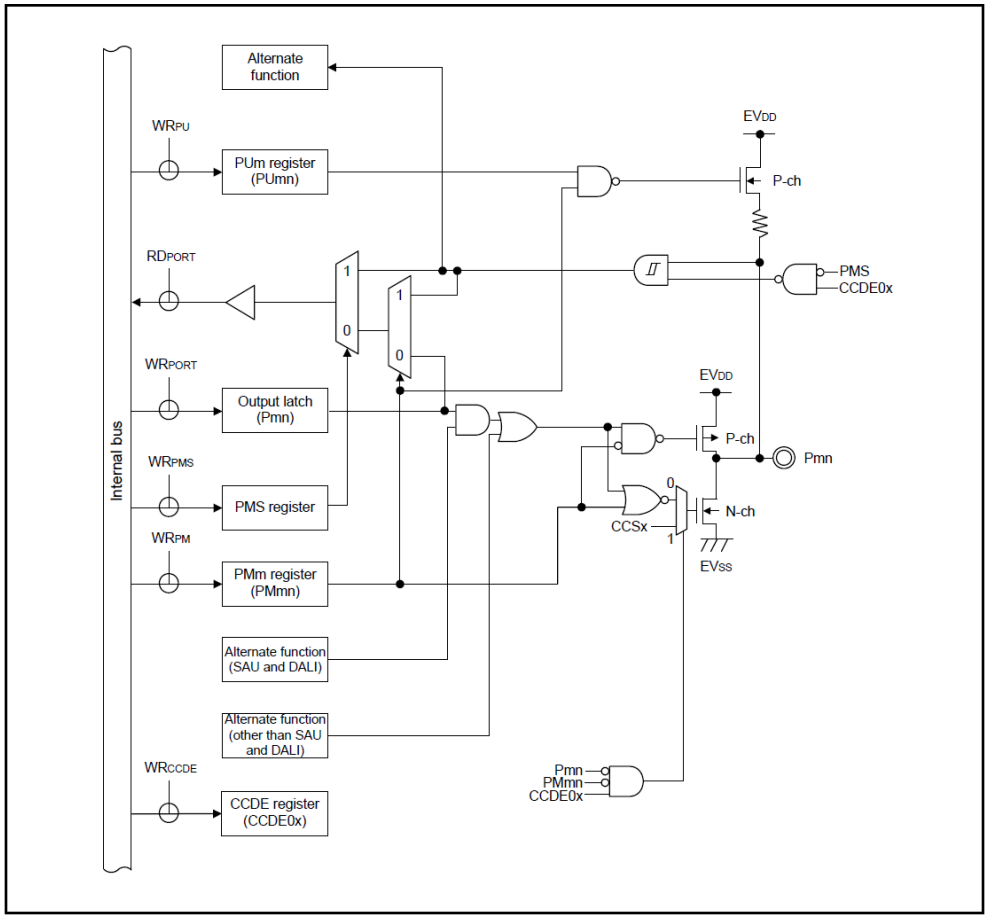
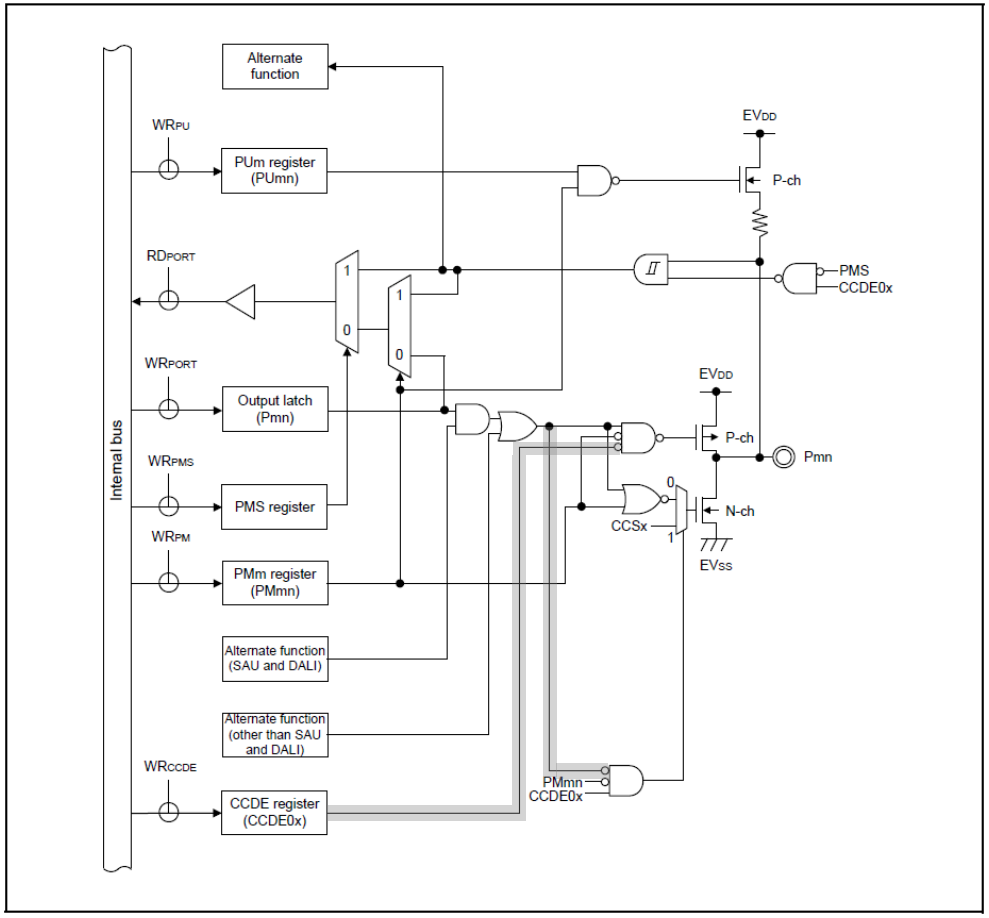


Figure 2 - 20 Pin Block Diagram for Pin Type 7-38-3



(Page 102)

Figure 2 - 26 Pin Block Diagram for Pin Type 8-41-1

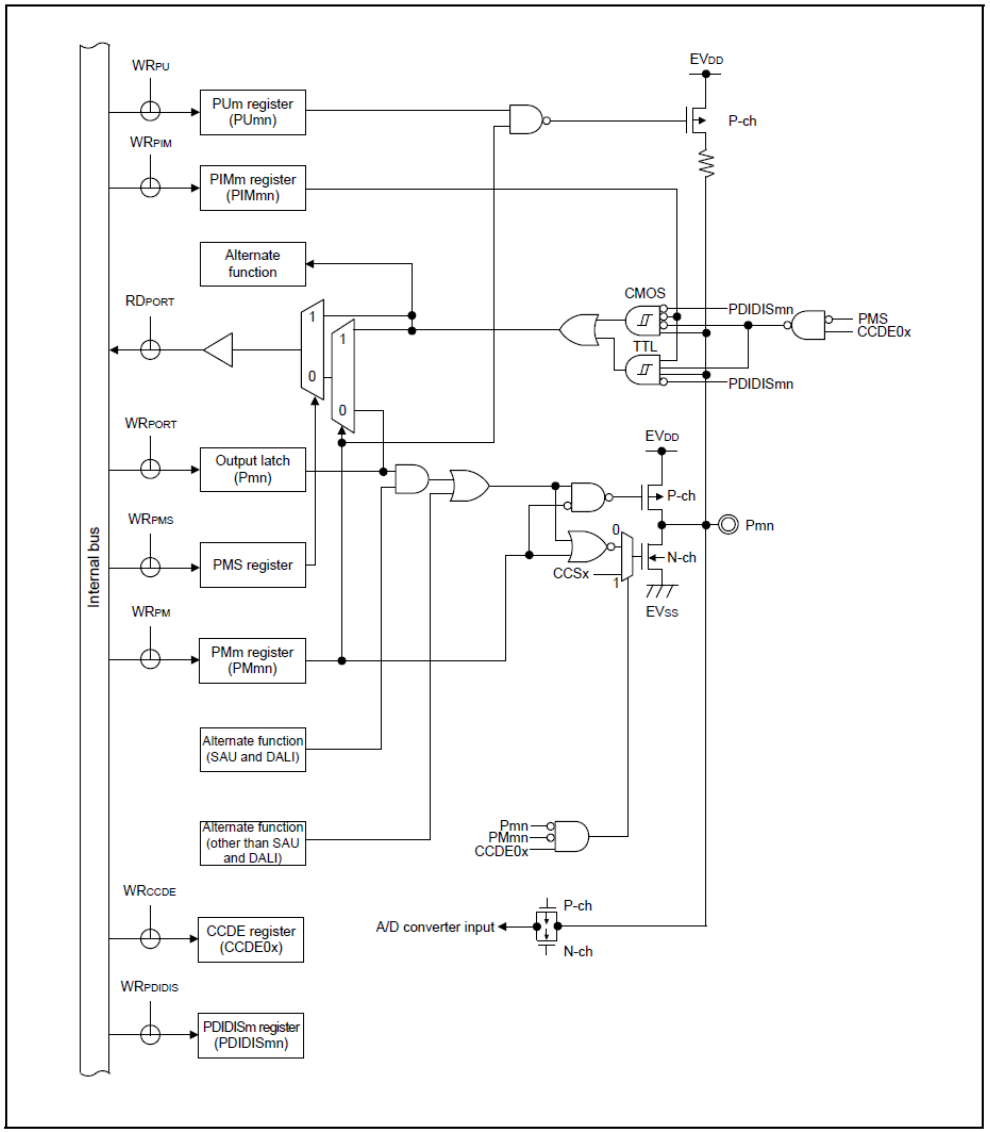
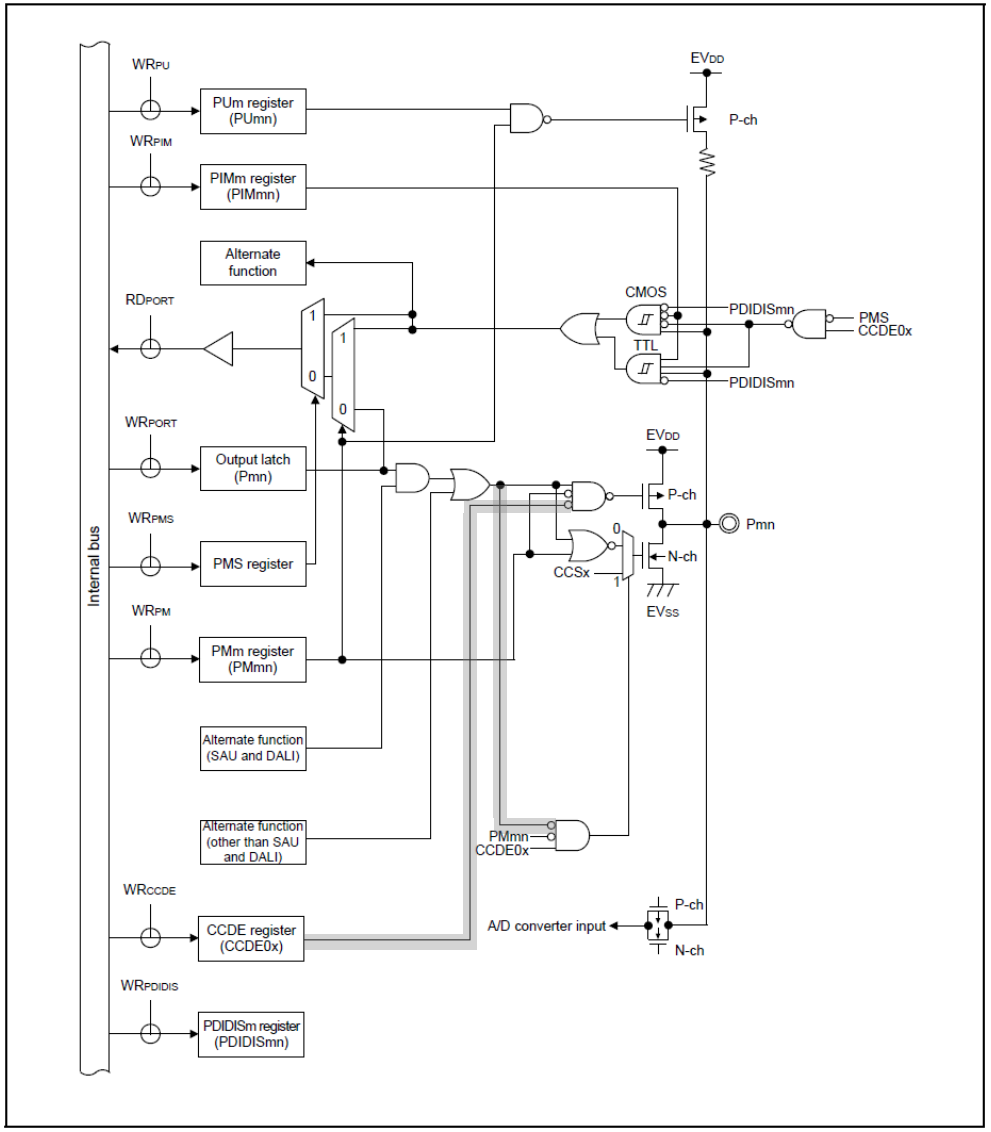


Figure 2 - 26 Pin Block Diagram for Pin Type 8-41-1



(Page 103)

Figure 2 - 27 Pin Block Diagram for Pin Type 8-41-2

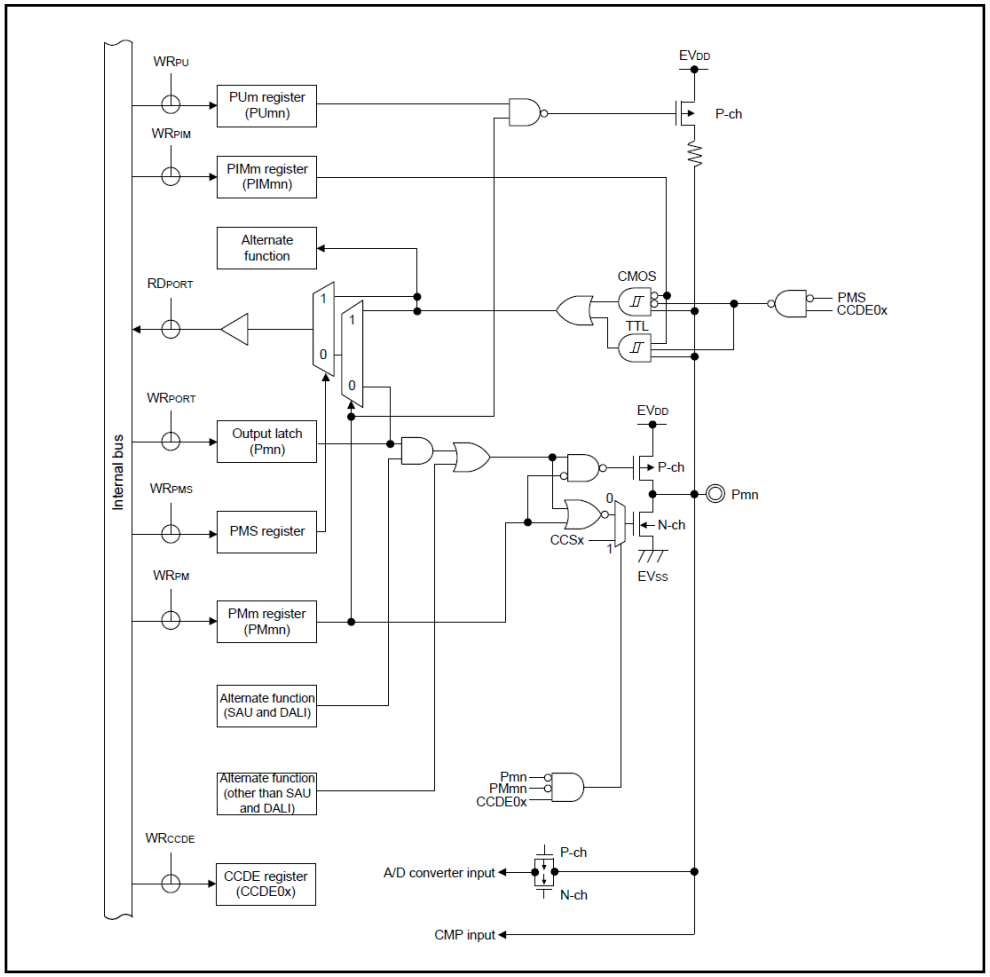
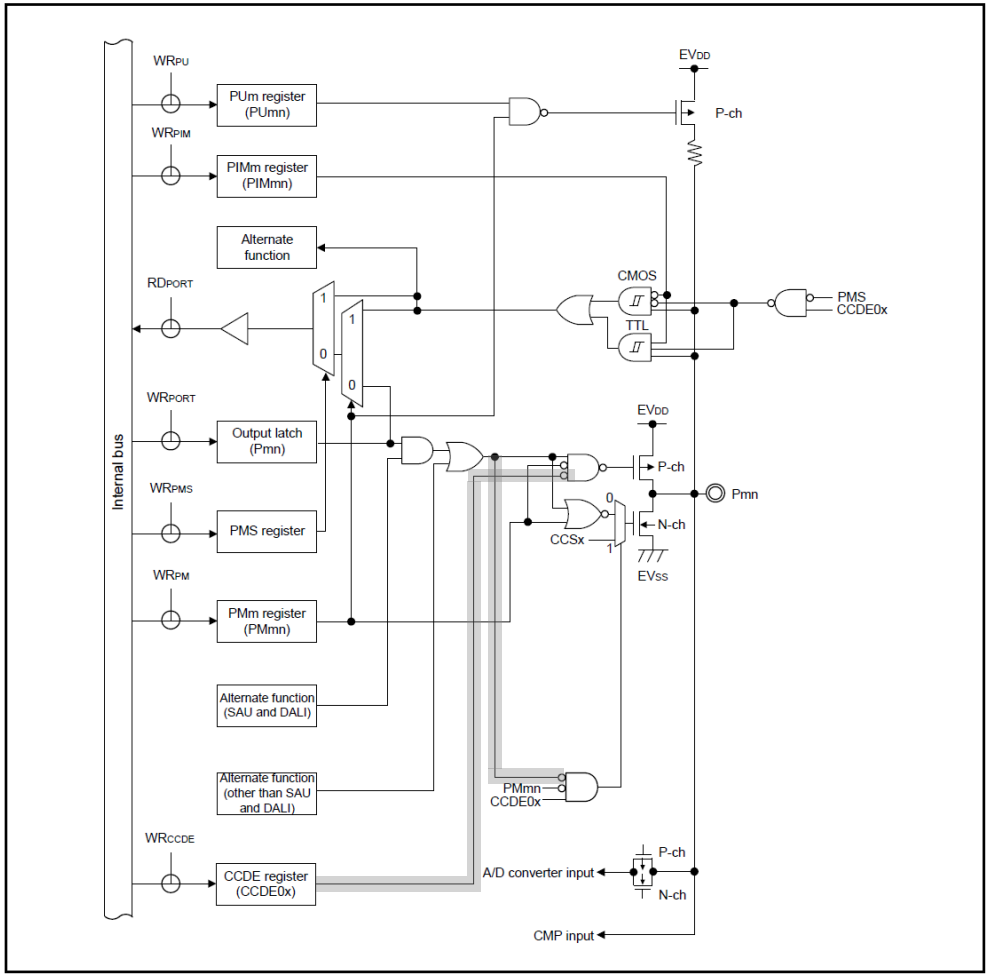


Figure 2 - 27 Pin Block Diagram for Pin Type 8-41-2



(Page 104)

Figure 2 - 28 Pin Block Diagram for Pin Type 8-42-1

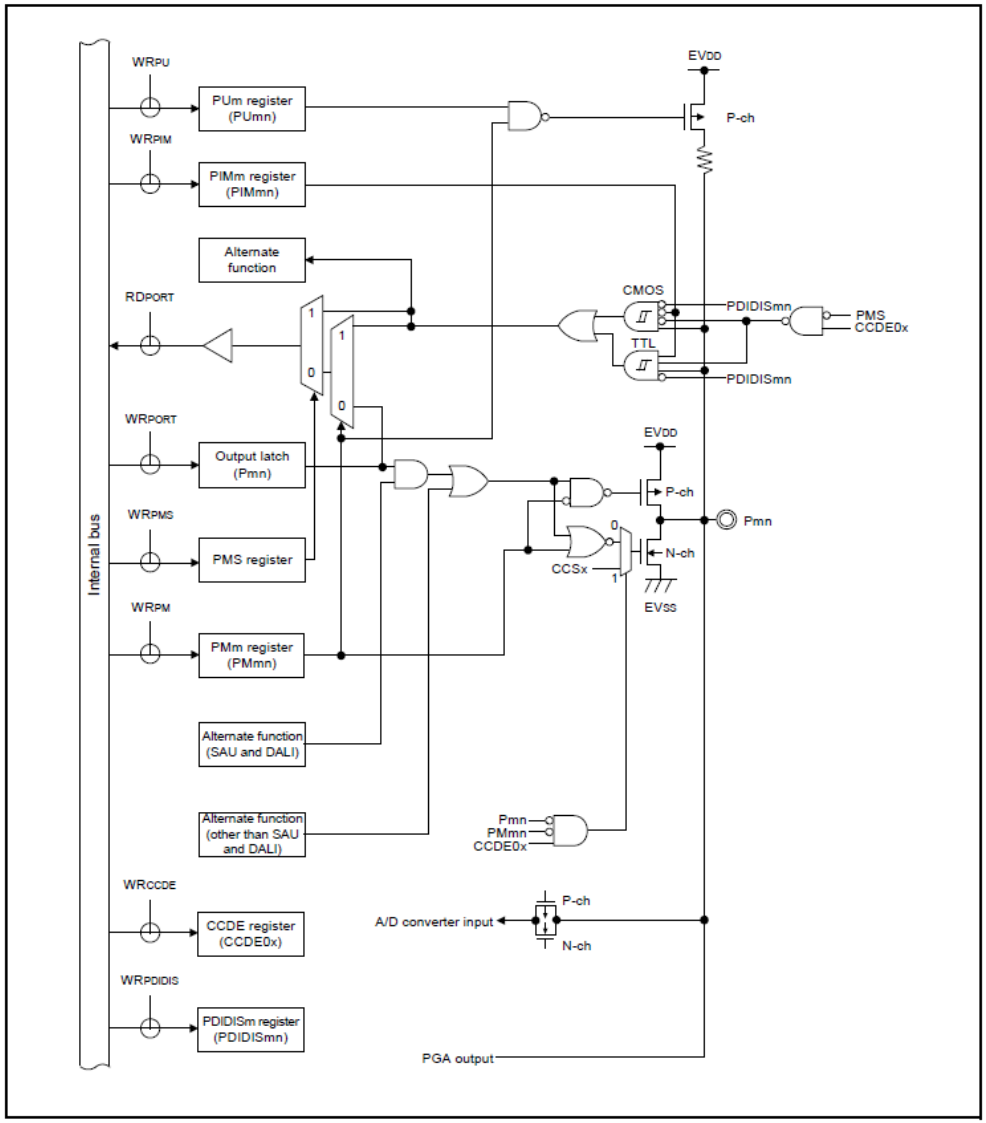
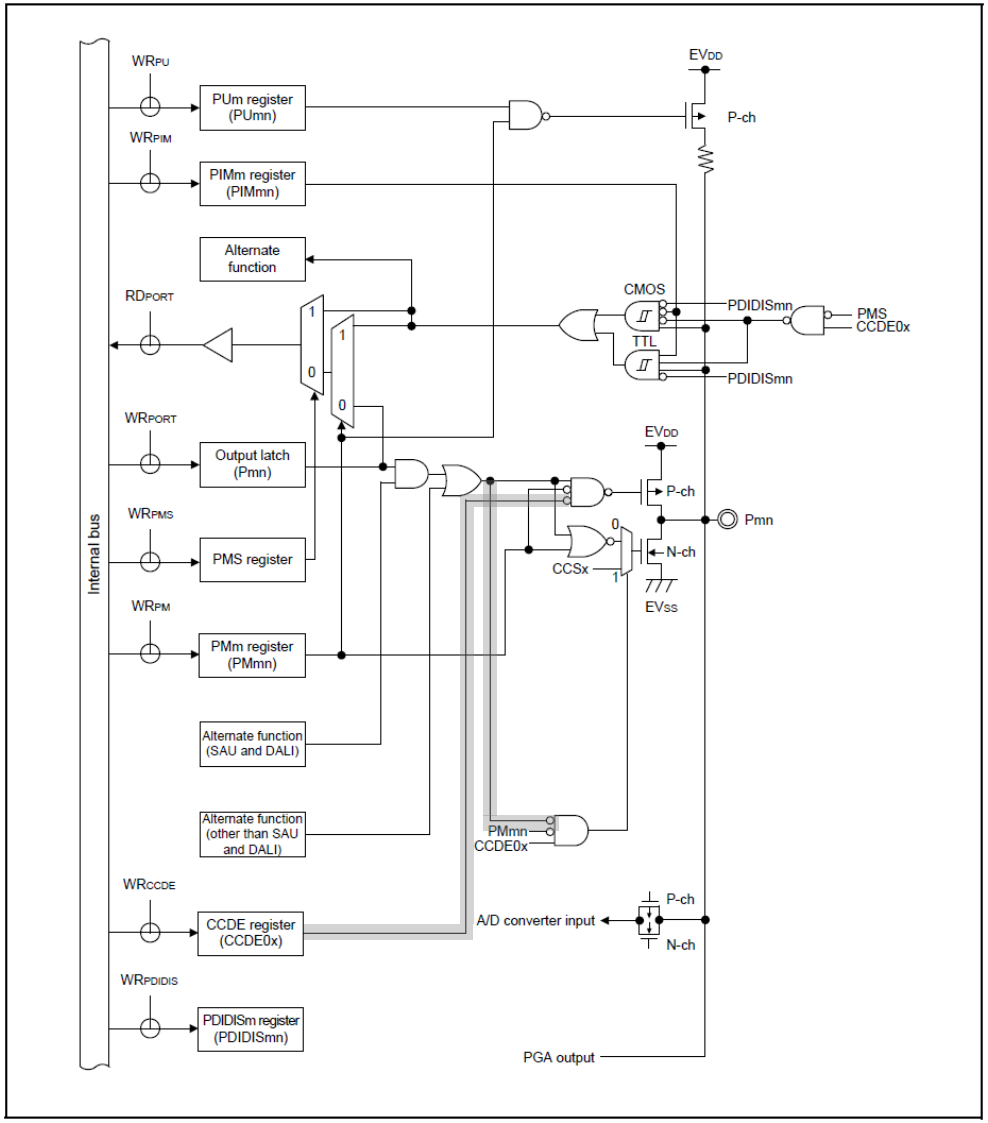
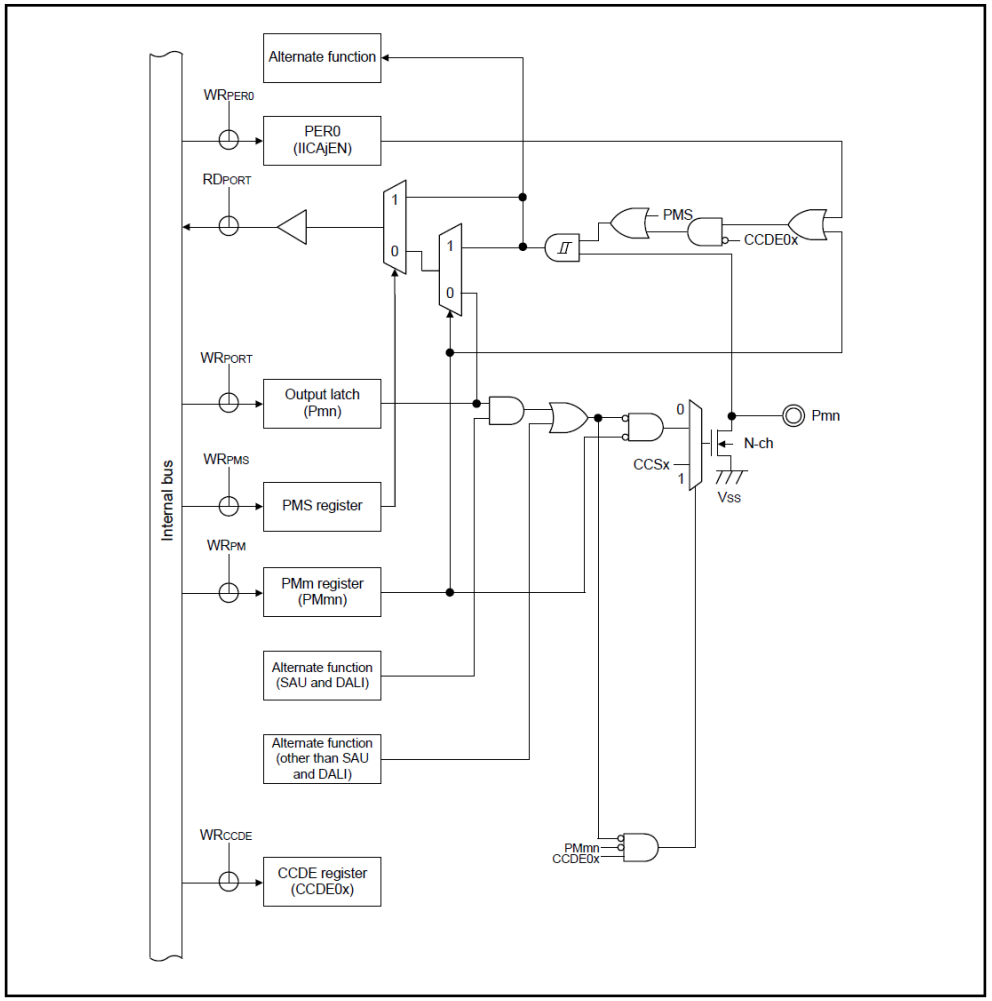


Figure 2 - 28 Pin Block Diagram for Pin Type 8-42-1



Add the figure below

Figure 2 - 29 Pin Block Diagram for Pin Type 12-38-2



9. 20.3.9 Analog input channel specification register (ADS) (Page 1106)

Incorrect:

Caution 8. Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating with the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in 43.3.2 Supply current characteristics or 44.3.2 Supply current characteristics will be added.

Caution 9. When the ADISS bit is set to 1, the hardware trigger wait mode and one-shot conversion mode are not available.

Caution 10. Set the ADS register to 00H when the advanced mode is enabled (ADM3.ADVMOD = 1).

Correct:

Caution 8. Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating with the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in 43.3.2 Supply current characteristics or 44.3.2 Supply current characteristics will be added.

Caution 9. When the ADISS bit is set to 1, the hardware trigger wait mode and one-shot conversion mode are not available.

Caution 10. When the setting of the ADISS bit is 1, the software trigger wait mode and one-shot conversion mode cannot be used at the same time.

Caution 11. Set the ADS register to 00H when the advanced mode is enabled (ADM3.ADVMOD = 1).

10. 20.3.10 Analog input channel specification registers n for advanced mode (ADSn) (Page 1107)

Incorrect:

Caution 10. Selecting PGA input as the target for conversion in normal 2 mode and low voltage 2 mode is prohibited.

Caution 11. Setting an ANI signal that is used by the PGA, DAC, CMP or other on-chip peripheral modules as the target for A/D conversion is prohibited.

Caution 12. When the ADSPSCn[1:0] bits are to be set to 10B or 11B, set the ADSn[4:0] bits to 00000B.

Correct:

Remove Caution 11.

Caution 10. Selecting PGA input as the target for conversion in normal 2 mode and low voltage 2 mode is prohibited.

Caution 11. When the ADSPSCn[1:0] bits are to be set to 10B or 11B, set the ADSn[4:0] bits to 00000B.

11. **20.6.2 Software trigger no-wait mode (select mode, one-shot conversion mode) (Page 1120)**

Incorrect:

(omitted)

Caution When <4>, <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 20 - 6 Selection of A/D Conversion Time (3/11) and Table 20 - 6 Selection of A/D Conversion Time (4/11).)

Correct:

(omitted)

Caution 1. When <4>, <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 20 - 6 Selection of A/D Conversion Time (3/11) and Table 20 - 6 Selection of A/D Conversion Time (4/11).)

Caution 2. The setting of ADISS being 1 (the input source is temperature sensor output voltage or internal reference voltage) cannot be used in the software trigger wait mode (one-shot conversion mode).

12. 24.3.8 Serial status registers mn (SSRmn) (mn = 00 to 03, 10, 11) (Page 1244)

Incorrect:

(omitted)

Caution 1. If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVFmn = 1) is detected.

Caution 2. When the simplified SPI (CSI) is performing reception operations in the SNOOZE mode (SWCm = 1), the OVFmn flag will not change.

(omitted)

Correct:

(omitted)

Caution 1. If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVFmn = 1) is detected.

Caution 2. When the simplified SPI (CSI) is performing reception operations in the SNOOZE mode (SWCm = 1), the OVFmn and BFFmn flag will not change.

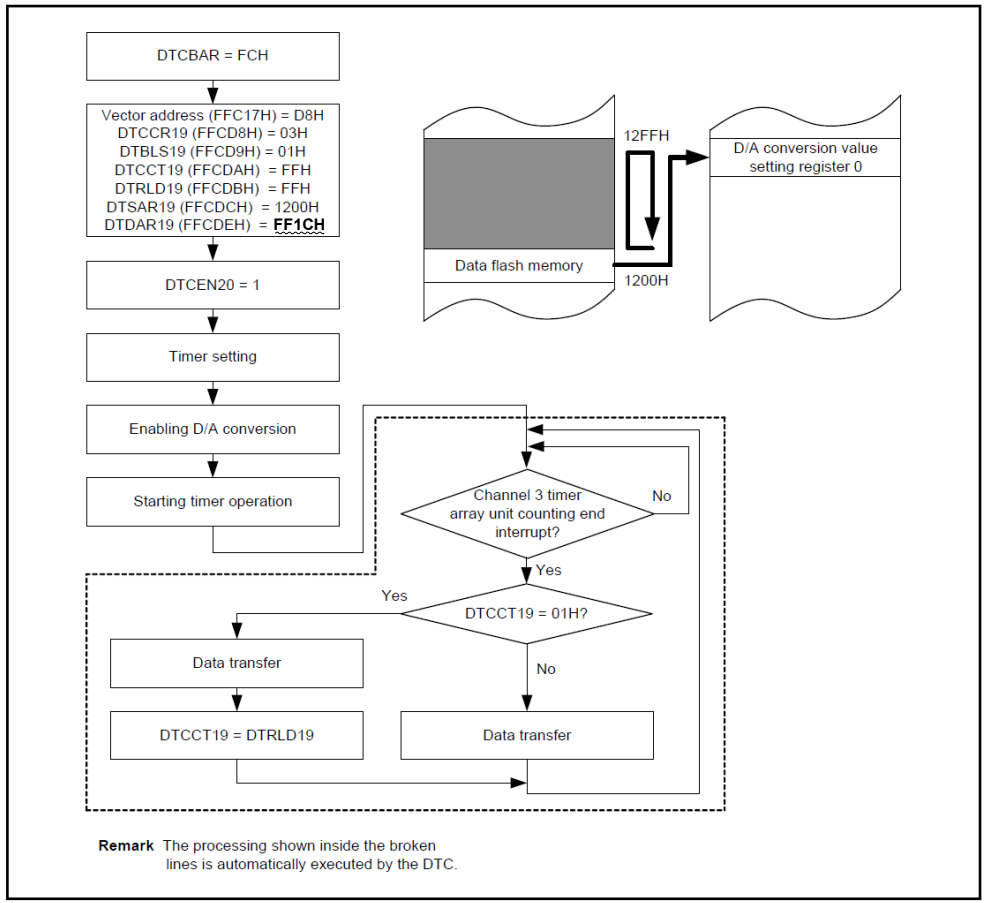
(omitted)

13. 27.4.3 Repeat mode (Page 1594)

Incorrect:

(omitted)

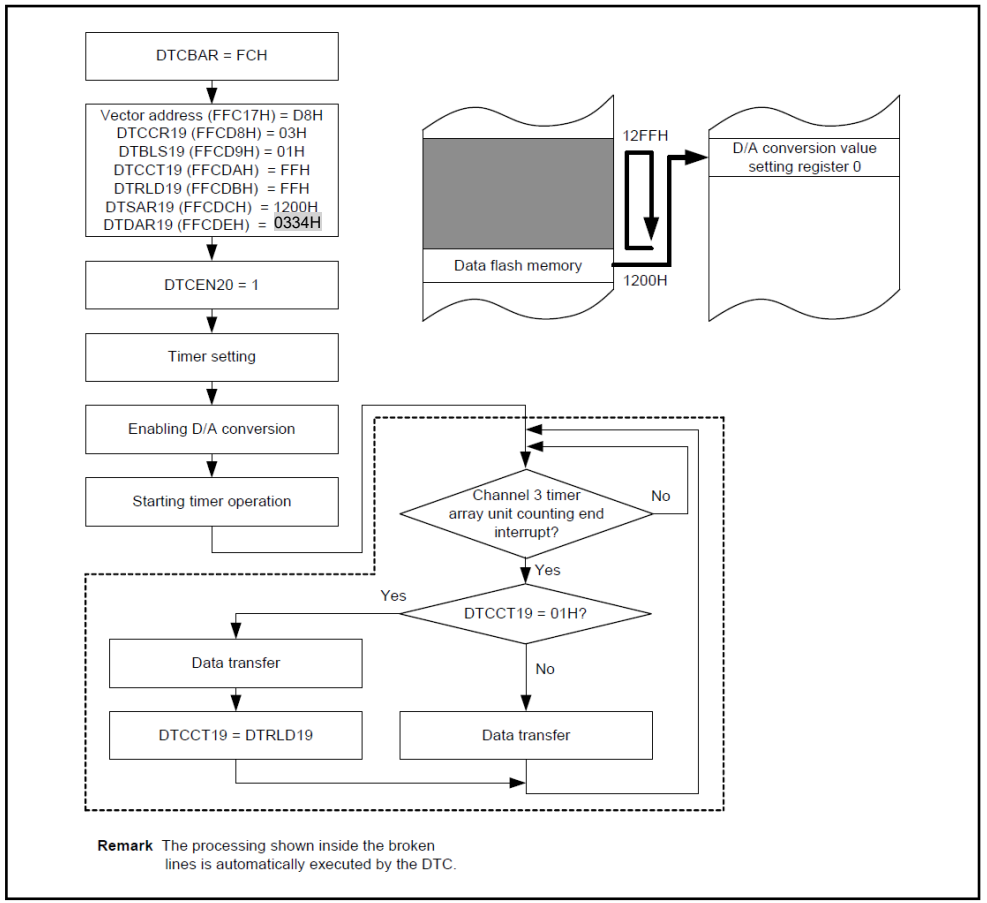
Figure 27 - 20 Example 2 of Using Repeat Mode: Outputting a Sine Wave Using the D/A Converter



Correct:

(omitted)

Figure 27 - 20 Example 2 of Using Repeat Mode: Outputting a Sine Wave Using the D/A Converter



14. 29.4 Interrupt Servicing Operations (Page 1634, Page 1636)

Incorrect:

(Page 1634)

(omitted)

Table 29 - 4 Times until Vectored Interrupt Servicing

	Minimum Time	Maximum Time[Note]
Servicing time (when PFBE = 0)	9 clock cycles	16 clock cycles
Servicing time (when PFBE = 1)	11 clock cycles	20 clock cycles

(omitted)

Correct:

(omitted)

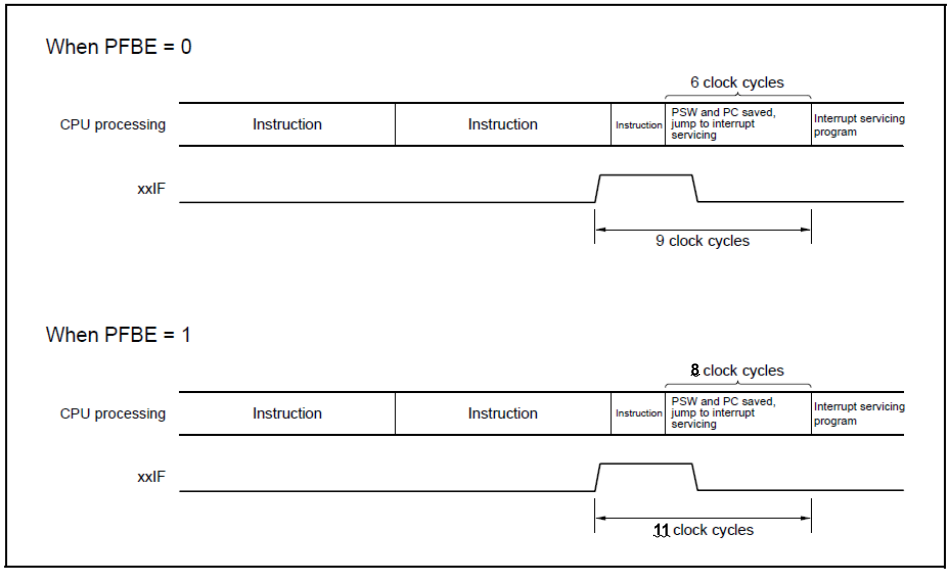
Table 29 - 4 Times until Vectored Interrupt Servicing

	Minimum Time	Maximum Time[Note]
Servicing time (when PFBE = 0)	9 clock cycles	16 clock cycles
Servicing time (when PFBE = 1)	13 clock cycles	24 clock cycles

(omitted)

(Page 1636)

Figure 29 - 8 Interrupt Request Acknowledgment Timing (Minimum Time)



Remark 1 clock cycle: 1/fCLK (fCLK: CPU clock)

Figure 29 - 9 Interrupt Request Acknowledgment Timing (Maximum Time)

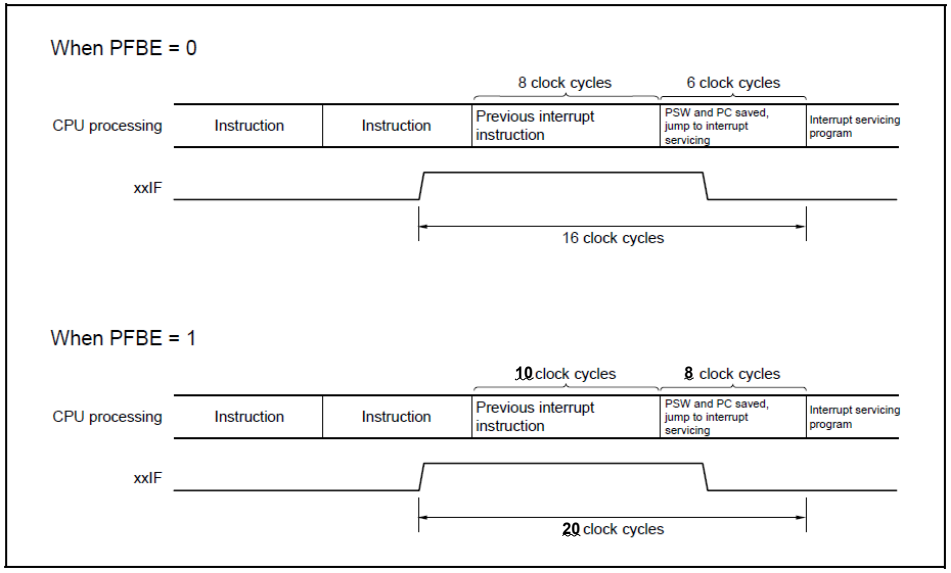
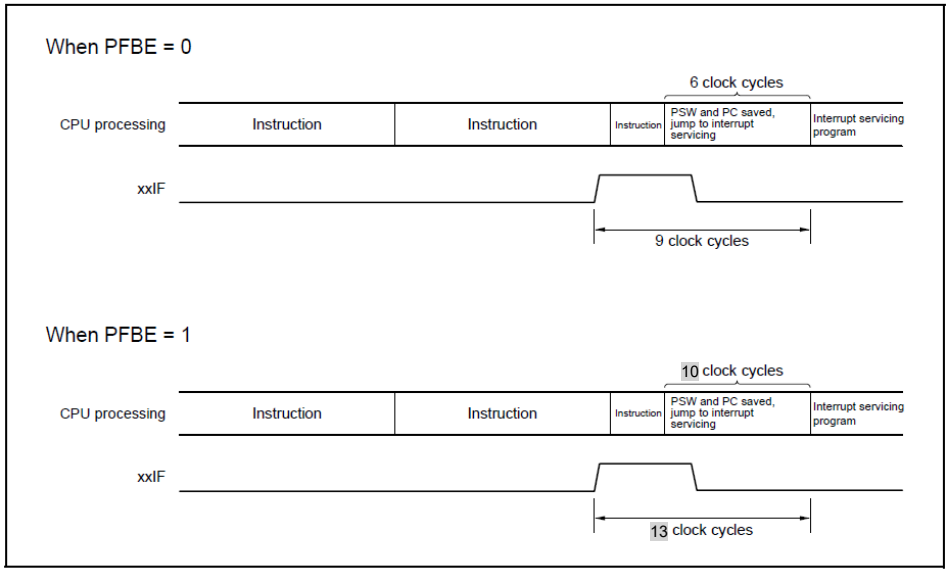
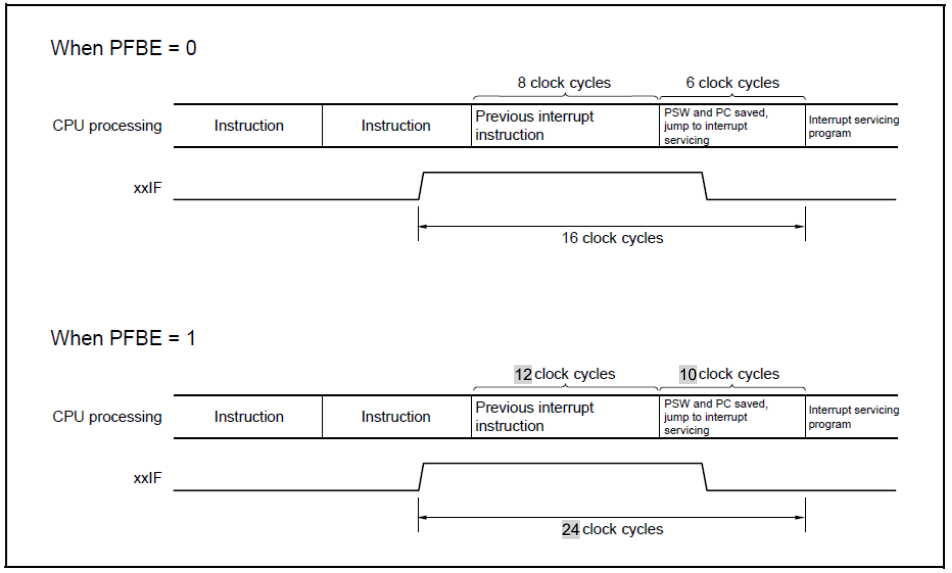


Figure 29 - 8 Interrupt Request Acknowledgment Timing (Minimum Time)



Remark 1 clock cycle: 1/fCLK (fCLK: CPU clock)

Figure 29 - 9 Interrupt Request Acknowledgment Timing (Maximum Time)



15. 42.2 Operation List (Page 1840) Incorrect:

Table 42 - 5 Operation List (17/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Stack manipulate	PUSH	PSW	2	1	—	(SP - 1) ← PSW, (SP - 2) ← 00H, SP ← SP - 2			
		rp	1	1	—	(SP - 1) ← rpH, (SP - 2) ← rpL, SP ← SP - 2			
	POP	PSW	2	3	—	PSW ← (SP + 1), SP ← SP + 2	R	R	R
		rp	1	1	—	rpL ← (SP), rpH ← (SP + 1), SP ← SP + 2			
	MOVW	SP, #word	4	1	—	SP ← word			
		SP, AX	2	1	—	SP ← AX			
		AX, SP	2	1	—	AX ← SP			
		HL, SP	3	1	—	HL ← SP			
		BC, SP	3	1	—	BC ← SP			
		DE, SP	3	1	—	DE ← SP			
	ADDW	SP, #byte	2	1	—	SP ← SP + byte			
	SUBW	SP, #byte	2	1	—	SP ← SP - byte			
Unconditional branch	BR	AX	2	3	—	PC ← CS, AX			
		$addr20	2	3	—	PC ← PC + 2 + jdisp8			
		$!addr20	3	3	—	PC ← PC + 3 + jdisp16			
		!addr16	3	3	—	PC ← 0000, addr16			
		!!addr20	4	3	—	PC ← addr20			
Conditional branch	BC	$addr20	2	2/4/6Note 3	—	PC ← PC + 2 + jdisp8 if CY = 1			
	BNC	$addr20	2	2/4/6Note 3	—	PC ← PC + 2 + jdisp8 if CY = 0			
	BZ	$addr20	2	2/4/6Note 3	—	PC ← PC + 2 + jdisp8 if Z = 1			
	BNZ	$addr20	2	2/4/6Note 3	—	PC ← PC + 2 + jdisp8 if Z = 0			
	BH	$addr20	3	2/4/6Note 3	—	PC ← PC + 3 + jdisp8 if (Z ∨ CY) = 0			
	BNH	$addr20	3	2/4/6Note 3	—	PC ← PC + 3 + jdisp8 if (Z ∨ CY) = 1			
	BT	saddr.bit, $addr20	4	3/5/7Note 3	—	PC ← PC + 4 + jdisp8 if (saddr).bit = 1			
		sfr.bit, $addr20	4	3/5/7Note 3	—	PC ← PC + 4 + jdisp8 if sfr.bit = 1			
		A.bit, $addr20	3	3/5/7Note 3	—	PC ← PC + 3 + jdisp8 if A.bit = 1			
		PSW.bit, $addr20	4	3/5/7Note 3	—	PC ← PC + 4 + jdisp8 if PSW.bit = 1			
		[HL].bit, $addr20	3	3/5/7Note 3	6/7/9Note 3	PC ← PC + 3 + jdisp8 if (HL).bit = 1			
		ES:[HL].bit, $addr20	4	4/6/8Note 3	7/8/10Note 3	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 1			

Note 1. Number of CPU clocks (fCLK) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (fCLK) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. The three numbers indicate the numbers of clock cycles when the condition is not met, when the condition is met and PFBE = 0, and when the condition is met and PFBE = 1.

Correct:

Table 42 - 5 Operation List (17/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Stack manipulate	PUSH	PSW	2	1	—	(SP - 1) ← PSW, (SP - 2) ← 00H, SP ← SP - 2			
		rp	1	1	—	(SP - 1) ← rpH, (SP - 2) ← rpL, SP ← SP - 2			
	POP	PSW	2	3	—	PSW ← (SP + 1), SP ← SP + 2	R	R	R
		rp	1	1	—	rpL ← (SP), rpH ← (SP + 1), SP ← SP + 2			
	MOVW	SP, #word	4	1	—	SP ← word			
		SP, AX	2	1	—	SP ← AX			
		AX, SP	2	1	—	AX ← SP			
		HL, SP	3	1	—	HL ← SP			
		BC, SP	3	1	—	BC ← SP			
		DE, SP	3	1	—	DE ← SP			
	ADDW	SP, #byte	2	1	—	SP ← SP + byte			
	SUBW	SP, #byte	2	1	—	SP ← SP - byte			
Unconditional branch	BR	AX	2	3/5Note 3	—	PC ← CS, AX			
		$addr20	2	3/5Note 3	—	PC ← PC + 2 + jdisp8			
		$!addr20	3	3/5Note 3	—	PC ← PC + 3 + jdisp16			
		!addr16	3	3/5Note 3	—	PC ← 0000, addr16			
		!!addr20	4	3/5Note 3	—	PC ← addr20			
Conditional branch	BC	$addr20	2	2/4/6Note 4	—	PC ← PC + 2 + jdisp8 if CY = 1			
	BNC	$addr20	2	2/4/6Note 4	—	PC ← PC + 2 + jdisp8 if CY = 0			
	BZ	$addr20	2	2/4/6Note 4	—	PC ← PC + 2 + jdisp8 if Z = 1			
	BNZ	$addr20	2	2/4/6Note 4	—	PC ← PC + 2 + jdisp8 if Z = 0			
	BH	$addr20	3	2/4/6Note 4	—	PC ← PC + 3 + jdisp8 if (Z ∨ CY) = 0			
	BNH	$addr20	3	2/4/6Note 4	—	PC ← PC + 3 + jdisp8 if (Z ∨ CY) = 1			
	BT	saddr.bit, $addr20	4	3/5/7Note 4	—	PC ← PC + 4 + jdisp8 if (saddr).bit = 1			
		sfr.bit, $addr20	4	3/5/7Note 4	—	PC ← PC + 4 + jdisp8 if sfr.bit = 1			
		A.bit, $addr20	3	3/5/7Note 4	—	PC ← PC + 3 + jdisp8 if A.bit = 1			
		PSW.bit, $addr20	4	3/5/7Note 4	—	PC ← PC + 4 + jdisp8 if PSW.bit = 1			
		[HL].bit, $addr20	3	3/5/7Note 4	6/7/9Note 4	PC ← PC + 3 + jdisp8 if (HL).bit = 1			
		ES:[HL].bit, $addr20	4	4/6/8Note 4	7/8/10Note 4	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 1			

Note 1. Number of CPU clocks (fCLK) when the internal RAM area, SFR area, or second SFR area is accessed, or when no data is accessed.

Note 2. Number of CPU clocks (fCLK) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Note 3. The two numbers indicate the numbers of clock cycles when PFBE = 0 and PFBE = 1.

Note 4. The three numbers indicate the numbers of clock cycles when the condition is not met, when the condition is met and PFBE = 0, and when the condition is met and PFBE = 1.

16. 43.2 Characteristics of the Oscillators (Page 1845)

Incorrect:

43.2.1 Characteristics of the X1 and XT1 oscillators

(TA = –40 to +105°C, **2.4 V ≤ VDD ≤ 5.5 V (20- to 32-pin products), 1.6 V ≤ VDD ≤ 5.5 V (40- to 64-pin products)** VSS = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time Note	Ceramic resonator/ crystal resonator		0.05		1	μs
XT1 clock oscillation frequency (fXT) Note	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillators. For actual applications, request the resonator manufacturer for evaluation of the resonators on the oscillator circuit mounted on a board so you can use appropriate values. Refer to **43.4 AC Characteristics** for instruction execution time.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Sufficiently evaluate the oscillation stabilization time with the resonator to be used, and then specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS).**

Correct:

43.2.1 Characteristics of the X1 oscillator

(TA = –40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V , VSS = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time Note	Ceramic resonator/ crystal resonator		0.05		1	μs

Note The listed time and frequency indicate permissible ranges of the oscillators. For actual applications, request the resonator manufacturer for evaluation of the resonators on the oscillator circuit mounted on a board so you can use appropriate values. Refer to **43.4 AC Characteristics** for instruction execution time.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Sufficiently evaluate the oscillation stabilization time with the resonator to be used, and then specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS).**

43.2.2 Characteristics of the XT1 oscillator

(TA = –40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V (20- to 32-pin products), 2.7 V ≤ VDD ≤ 5.5 V (40- to 64-pin products) , VSS = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
XT1 clock oscillation frequency (fXT) Note	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillators. For actual applications, request the resonator manufacturer for evaluation of the resonators on the oscillator circuit mounted on a board so you can use appropriate values. Refer to **43.4 AC Characteristics** for instruction execution time.

17. 43.3.2 Supply current characteristics (Page 1856, Page 1859)

Incorrect:

(Page 1856)

(T_A = –40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/5)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	LS (low-speed main) mode	f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	2.4	mA
						V_{DD} = 1.8 V		0.9	2.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Typ. column do not include the peripheral operating current in the HS (high-speed main), LS (low-speed main), or **LV (low-voltage main)** mode. **The currents in the Max. column include the peripheral operating current, but do not include those of the FAA, A/D converter, sample & hold circuit, D/A converter, PGA, comparator, TRNG, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing when the data flash memory is being rewritten.**

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

Correct:

(T_A = –40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/5)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	LS (low-speed main) mode	f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	2.4	mA
						V_{DD} = 1.8 V		0.9	2.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Typ. column do not include the peripheral operating current in the HS (high-speed main), LS (low-speed main), or LP (low-power main) mode. The currents in the Max. column include the operating currents of the PCLBUZ, TAU, SAU, IICA, timer RD2, timer RX, and 16-bit timers KB30, KB31, and KB32.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1859)

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Typ. column do not include the peripheral operating current when the CPU is placed in the HS (high-speed main), LS (low-speed main), or **LV (low-voltage main)** mode. **The currents in the Max. column include the peripheral operating current, but do not include those of the FAA, A/D converter, sample & hold circuit, D/A converter, PGA, comparator, TRNG, LVD circuit, I/O port, and on-chip pull-up-/pulldown resistors, and those flowing when the data flash memory is being rewritten. The currents in the Max. column include that of the RTC when the CPU is placed in the HALT mode.**

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Typ. column do not include the peripheral operating current when the CPU is placed in the HS (high-speed main), LS (low-speed main), or LP (low-power main) mode. The currents in the Max. column include the operating currents of the PCLBUZ, TAU, SAU, IICA, timer RD2, timer RX, and 16-bit timers KB30, KB31, and KB32.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

18. 44.2 Characteristics of the Oscillators (Page 1925)

Incorrect:

44.2.1 Characteristics of the X1 and XT1 oscillators

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time Note	Ceramic resonator/ crystal resonator		0.05		1	μs
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillators. For actual applications, request the resonator manufacturer for evaluation of the resonators on the oscillator circuit mounted on a board so you can use appropriate values. Refer to **44.4 AC Characteristics** for instruction execution time.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Sufficiently evaluate the oscillation stabilization time with the resonator to be used, and then specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS).**

Correct:

44.2.1 Characteristics of the X1 oscillator

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time Note	Ceramic resonator/ crystal resonator		0.05		1	μs

Note The listed time and frequency indicate permissible ranges of the oscillators. For actual applications, request the resonator manufacturer for evaluation of the resonators on the oscillator circuit mounted on a board so you can use appropriate values. Refer to **44.4 AC Characteristics** for instruction execution time.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Sufficiently evaluate the oscillation stabilization time with the resonator to be used, and then specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS).**

44.2.2 Characteristics of the XT1 oscillator

(T_A = –40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V (40- to 64-pin, V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillators. For actual applications, request the resonator manufacturer for evaluation of the resonators on the oscillator circuit mounted on a board so you can use appropriate values. Refer to **44.4 AC Characteristics** for instruction execution time.

19. 44.3.2 Supply current characteristics (Page 1934, Page 1937)

Incorrect:

(Page 1934)

(T_A = –40 to +125°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/5)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	LS (low-speed main) mode	f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	2.8	mA
						V_{DD} = 2.7 V		0.9	2.8	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Typ. column do not include the peripheral operating current when the CPU is placed in the HS (high-speed main), LS (low-speed main), or **LV (low-voltage main)** mode. **The currents in the Max. column include the peripheral operating current, but do not include those of the FAA, A/D converter, sample & hold circuit, D/A converter, PGA, comparator, TRNG, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing when the data flash memory is being rewritten.**

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

Correct:

(T_A = –40 to +125°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/5)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	LS (low-speed main) mode	f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	2.8	mA
						V_{DD} = 2.7 V		0.9	2.8	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Typ. column do not include the peripheral operating current when the CPU is placed in the HS (high-speed main), LS (low-speed main), or LP (low-power main) mode. The currents in the Max. column include the operating currents of the PCLBUZ, TAU, SAU, IICA, timer RD2, timer RX, and 16-bit timers KB30, KB31, and KB32.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1937)

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Typ. column do not include the peripheral operating current when the CPU is placed in the HS (high-speed main), LS (low-speed main), or **LV (low-voltage main)** mode. **The currents in the Max. column include the peripheral operating current, but do not include those flowing into the FAA, A/D converter, sample & hold circuit, D/A converter, PGA, comparator, TRNG, LVD circuit, I/O port, and on-chip pull-up-/pull-down resistors, and those flowing when the data flash memory is being rewritten. The currents in the Max. column include that of the RTC when the CPU is placed in the HALT mode.**

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Typ. column do not include the peripheral operating current when the CPU is placed in the HS (high-speed main), LS (low-speed main), or LP (low-power main) mode. The currents in the Max. column include the operating currents of the PCLBUZ, TAU, SAU, IICA, timer RD2, timer RX, and 16-bit timers KB30, KB31, and KB32.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

20. 44.4 AC Characteristics (Page 1942)

Incorrect:

(T_A = –40 to +125°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Instruction cycle	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode (Prefetch ON)	0.02083		1	μs
			HS (high-speed main) mode (Prefetch OFF)	0.03125		1	μs
			LS (low-speed main) mode	0.04167		1	μs
			LP (low-power main) mode	0.5		1	μs
		Subsystem clock (f_{SUB}) operation		26.041	30.5	31.3	μs
		Self-programming mode	HS (high-speed main) mode	0.03125		1	μs
			LS (low-speed main) mode	0.04167		1	μs
External system clock frequency	f_{EX}			1.0		20.0	MHz
	f_{EXS}			32		38.4	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}			24			ns
	t_{EXHS}, t_{EXLS}			13.7			μs
TI00 to TI03 input high-level width, low-level width	t_{TIH}, t_{TIL}			1/f_{MCK} + 10			ns
Timer RJ input cycle	t_C	TRJIO		100			ns
Timer RJ input high-level width, low-level width	t_{TJIH}, t_{TJIL}	TRJIO		40			ns
Timer RD2 input high-level width, low-level width	t_{TDIH}, t_{TDIL}	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/f_{CLK}			ns
Timer RD2 forcible shut-off signal input low-level width	t_{TDSIL}	P137/INTP0	2 MHz ≤ f_{CLK} ≤ 48 MHz	1			μs
			f_{CLK} ≤ 2 MHz	1/f_{CLK} + 1			μs
Timer RG2 input high-level width, low-level width	t_{TGIH}, t_{TGIL}	TRGIOA, TRGIOB, TRGIDZ, TRGTRG		2.5/f_{CLK}			ns
TO00 to TO03 TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TRJIO0, TRJO0, TRGIOA, TRGIOB, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 output frequency	f_{TO}	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
		LP (low-power main) mode				2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
		LP (low-power main) mode				2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP20, INTP21	2.7 V ≤ V_{DD} ≤ 5.5 V	1			μs
		INTP1 to INTP11	2.7 V ≤ EV_{DD0} ≤ 5.5 V	1			μs
Key interrupt input high-level width, low-level width	t_{KRH}, t_{KRL}	KR0 to KR7	2.7 V ≤ EV_{DD0} ≤ 5.5 V	250			ns

Correct:

(T_A = –40 to +125°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Instruction cycle	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode (Prefetch ON)	0.02083		1	μs
			HS (high-speed main) mode (Prefetch OFF)	0.03125		1	μs
			LS (low-speed main) mode	0.04167		1	μs
			LP (low-power main) mode	0.5		1	μs
		Subsystem clock (f_{SUB}) operation		26.041	30.5	31.3	μs
		Self-programming mode	HS (high-speed main) mode	0.03125		1	μs
			LS (low-speed main) mode	0.04167		1	μs
External system clock frequency	f_{EX}			1.0		20.0	MHz
	f_{EXS}			32		38.4	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}			24			ns
	t_{EXHS}, t_{EXLS}			13.7			μs
TI00 to TI03 input high-level width, low-level width	t_{TIH}, t_{TIL}			1/f_{MCK} + 10			ns
Timer RJ input cycle	t_C	TRJIO		100			ns
Timer RJ input high-level width, low-level width	t_{TJIH}, t_{TJIL}	TRJIO		40			ns
Timer RD2 input high-level width, low-level width	t_{TDIH}, t_{TDIL}	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/f_{CLK}			ns
Timer RD2 forcible shut-off signal input low-level width	t_{TDSIL}	P137/INTP0	2 MHz ≤ f_{CLK} ≤ 48 MHz	1			μs
			f_{CLK} ≤ 2 MHz	1/f_{CLK} + 1			μs
Timer RG2 input high-level width, low-level width	t_{TGIH}, t_{TGIL}	TRGIOA, TRGIOB, TRGIDZ, TRGTRG		2.5/f_{CLK}			ns
TO00 to TO03 TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TRJIO0, TRJO0, TRGIOA, TRGIOB, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 output frequency	f_{TO}	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V			12	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
		LP (low-power main) mode				2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V			12	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
		LP (low-power main) mode				2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP20, INTP21	2.7 V ≤ V_{DD} ≤ 5.5 V	1			μs
		INTP1 to INTP11	2.7 V ≤ EV_{DD0} ≤ 5.5 V	1			μs
Key interrupt input high-level width, low-level width	t_{KRH}, t_{KRL}	KR0 to KR7	2.7 V ≤ EV_{DD0} ≤ 5.5 V	250			ns