Date: Oct. 30, 2025

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0151A/E	Rev.	3.00
Title	Correction for Incorrect Description Notice RL78/G23 Descriptions in the User's Manual: Hardware Rev. 1.30 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G23 Group	Lot No. All lots	Reference Document	RL78/G23 User's Manual: Hardware Rev. 1.30 R01UH0896EJ0130 (Jan. 2024)		

This document describes misstatements found in the RL78/G23 User's Manual: Hardware Rev. 1.30 (R01UH0896EJ0130).

Corrections

Applicable Item	Applicable Page	Contents
23.3 Standby Function Operation	Page 1128, Page 1130, Page 1140, Page 1141	Incorrect descriptions revised Caution added
Table 30-1 CTSU Functions	Page 1254	Incorrect descriptions revised
Figure 30-4 Sensor Drive Pulse Output Clock Configuration	Page 1255	Incorrect descriptions revised Description added
30.1.2 Measurement Status	-	Description added
30.2.3 CTSU control registers AL and AH (CTSUCRAL, CTSUCRAH)	Page 1262 to Page 1265	Caution added Incorrect descriptions revised Description added Improvement descriptions
30.2.4 CTSU control registers BL and BH (CTSUCRBL, CTSUCRBH)	Page 1266 to Page 1268	Caution added Incorrect descriptions revised Description added
30.2.5 CTSU measurement channel registers L and H (CTSUMCHL, CTSUMCHH)	Page 1270	Caution added Incorrect descriptions revised
30.2.6 CTSU channel enable control registers AL, AH, BL, and BH (CTSUCHACAL, CTSUCHACAH, CTSUCHACBL, CTSUCHACBH)	Page 1272	Incorrect descriptions revised Description added
30.2.7 CTSU channel transmit/receive control registers AL, AH, BL, and BH (CTSUCHTRCAL, CTSUCHTRCAH, CTSUCHTRCBL, CTSUCHTRCBH)	Page 1274	Incorrect descriptions revised
30.2.8 CTSU status register L (CTSUSRL)	Page 1276	Caution added Incorrect descriptions revised Description added
30.2.9 CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)	Page 1277, Page 1278	Caution added Incorrect descriptions revised Description added
30.2.10 CTSU sensor counter registers L and H (CTSUSC, CTSUUC)	Page 1279	Description added
30.2.13 CTSU trimming registers AL and AH (CTSUTRIM0, CTSUTRIM1)	Page 1285, Page 1286	Caution added Description added
30.2.14 CTSU trimming registers BL and BH (CTSUTRIM2, CTSUTRIM3)	Page 1287	Caution added Description added
Added Description of TSCAP pin	-	Caution added Description added

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

No.	Corrections and Applicable Items		Pages in this document for corrections
	Document No. English	R01UH0896EJ0130	
1	3.1 Memory Space	Page 147 to Page 153, Page 160	Page 4 to Page 11
2	33.6.1 Self-programming procedure	Page 1315	Page 12
3	33.10.1 Overview of the data flash memory	Page 1366	Page 13
4	34.3 Security Settings for On-chip Debugging	Page 1369	Page 14
5	2.2.3.2 Connecting the VBAT pin to the battery for use in backing up	Page 106	Page 15
6	2.2.3.3 Using the VBAT pin	Page 107	Page 16
7	2.4 Block Diagrams of Pins	Page 125, Page 126, Page 132, Page 135, Page 138 to Page 141, Page 143 to Page 145	Page 17 to Page 26
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10	12.6.6 Software trigger wait mode (select mode, one-shot conversion mode)	Page 586	Page 30
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13	17.3.4 Baud Rate Generator	Page 943	Page 33
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16	37.3.1 Pin characteristics	Page 1406	Page 38
17	37.3.2 Supply current characteristics	Page 1411, Page 1414, Page 1418, Page 1421, Page 1425, Page 1428	Page 39 to Page 44
18	37.6.1 A/D converter characteristics	Page 1475, Page 1476	Page 45, Page 46
19	23.3 Standby Function Operation	Page 1128, Page 1130, Page 1140, Page 1141	Page 47 to Page 49
20	Table 30-1 CTSU Functions	Page 1254	Page 50
21	Figure 30-4 Sensor Drive Pulse Output Clock Configuration	Page 1255	Page 51
22	30.1.2 Measurement Status	-	Page 52, Page 53
23	30.2.3 CTSU control registers AL and AH (CTSUCRAL, CTSUCRAH)	Page 1262 to Page 1265	Page 54 to Page 58
24	30.2.4 CTSU control registers BL and BH (CTSUCRBL, CTSUCRBH)	Page 1266 to Page 1268	Page 59 to Page 62
25	30.2.5 CTSU measurement channel registers L and H (CTSUMCHL, CTSUMCHH)	Page 1270	Page 63, Page 64
26	30.2.6 CTSU channel enable control registers AL, AH, BL, and BH (CTSUCHACAL, CTSUCHACAH, CTSUCHACBL, CTSUCHACBH)	Page 1272	Page 65
27	30.2.7 CTSU channel transmit/receive control registers AL, AH, BL, and BH (CTSUCHTRCAL, CTSUCHTRCAH, CTSUCHTRCBL, CTSUCHTRCBH)	Page 1274	Page 66
28	30.2.8 CTSU status register L (CTSUSRL)	Page 1276	Page 67
29	30.2.9 CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)	Page 1277, Page 1278	Page 68 to Page 70
30	30.2.10 CTSU sensor counter registers L and H (CTSUSC, CTSUUC)	Page 1279	Page 71
31	30.2.13 CTSU trimming registers AL and AH (CTSUTRIM0, CTSUTRIM1)	Page 1285, Page 1286	Page 72, Page 73
32	30.2.14 CTSU trimming registers BL and BH (CTSUTRIM2, CTSUTRIM3)	Page 1287	Page 74
33	Added Description of TSCAP pin	-	Page 75

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G23 Correction for incorrect description notice

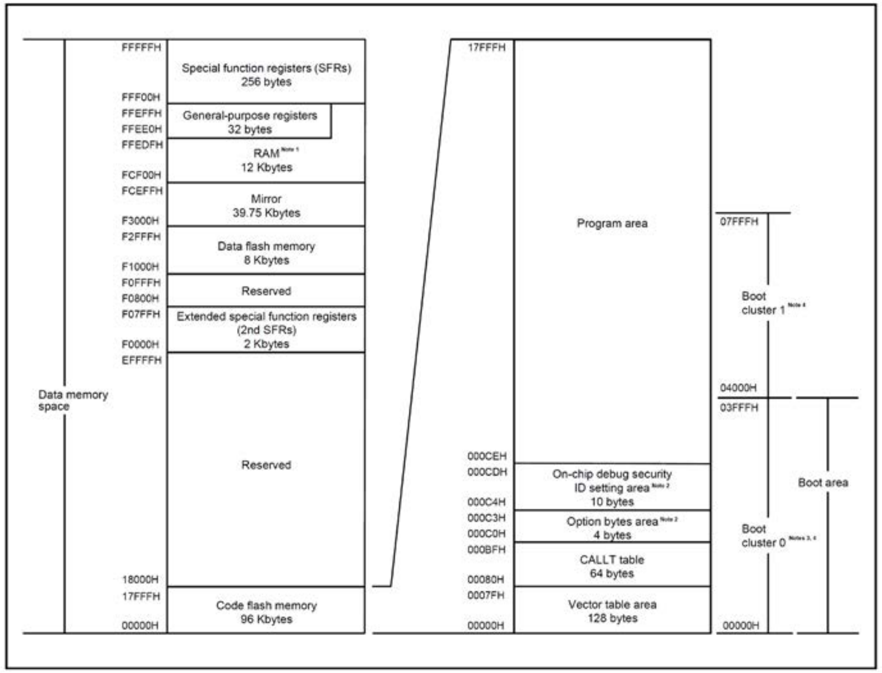
Document Number	Issue Date	Description
TN-RL*-A0133A/E	Apr. 26, 2024	First edition issued Corrections No.1 to No.4 revised
TN-RL*-A0133B/E	May. 22, 2025	Corrections No.5 to No.18 revised
TN-RL*-A0151A/E	Oct. 30, 2025	Corrections No.19 to No.33 revised (this document)

1. 3.1 Memory Space (Page 147 to Page 153, Page 160)

Incorrect:
(Page 147)

Products in the RL78/G23 can access a 1 MB address space. Figure 3 - 1 to Figure 3 - 3 show the memory maps.

Figure 3 - 1 Memory Map (R7F100GxF (x = A, B, C, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

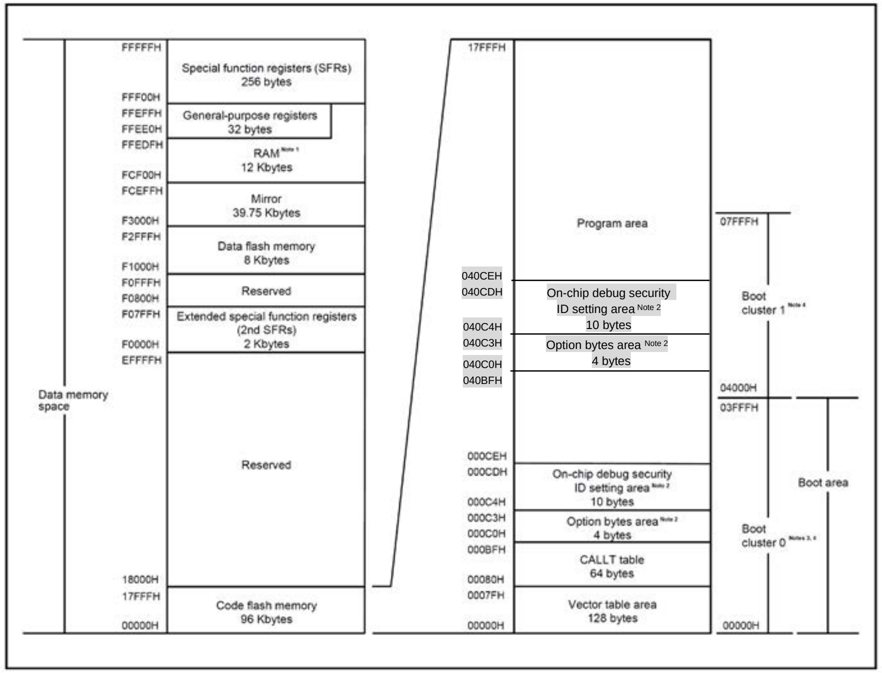
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Correct:

Products in the RL78/G23 can access a 1 MB address space. Figure 3 - 1 to Figure 3 - 3 show the memory maps.

Figure 3 - 1 Memory Map (R7F100GxF (x = A, B, C, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

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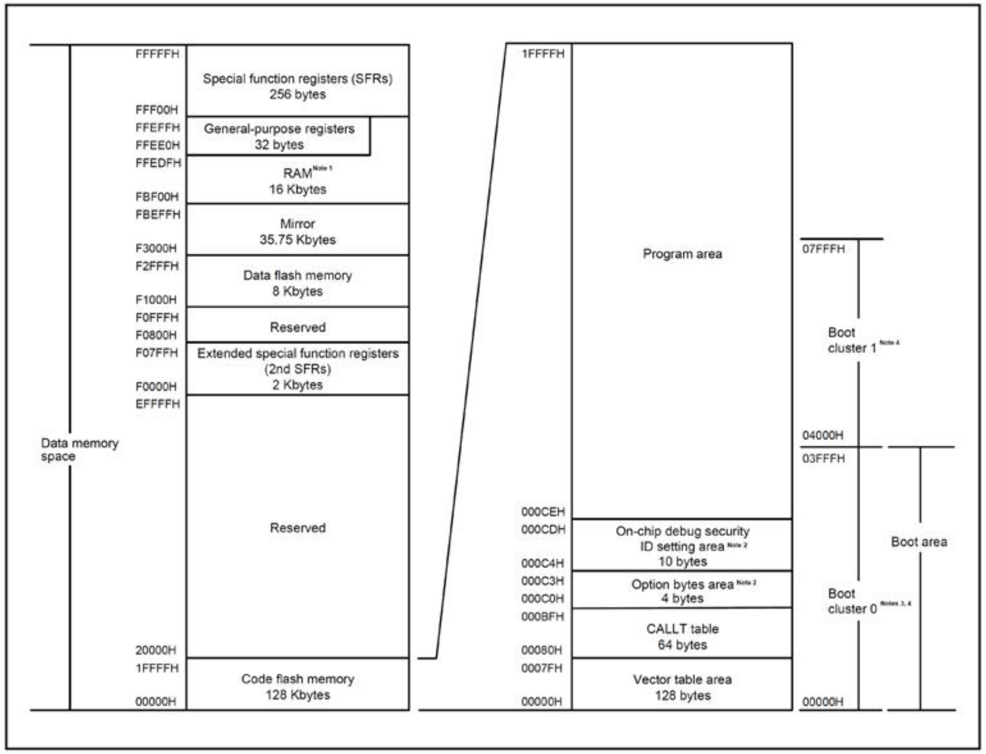
Figure 3 - 2 Memory Map (R7F100GxG (x = A, B, C, E, F, G, J, L, M, P))



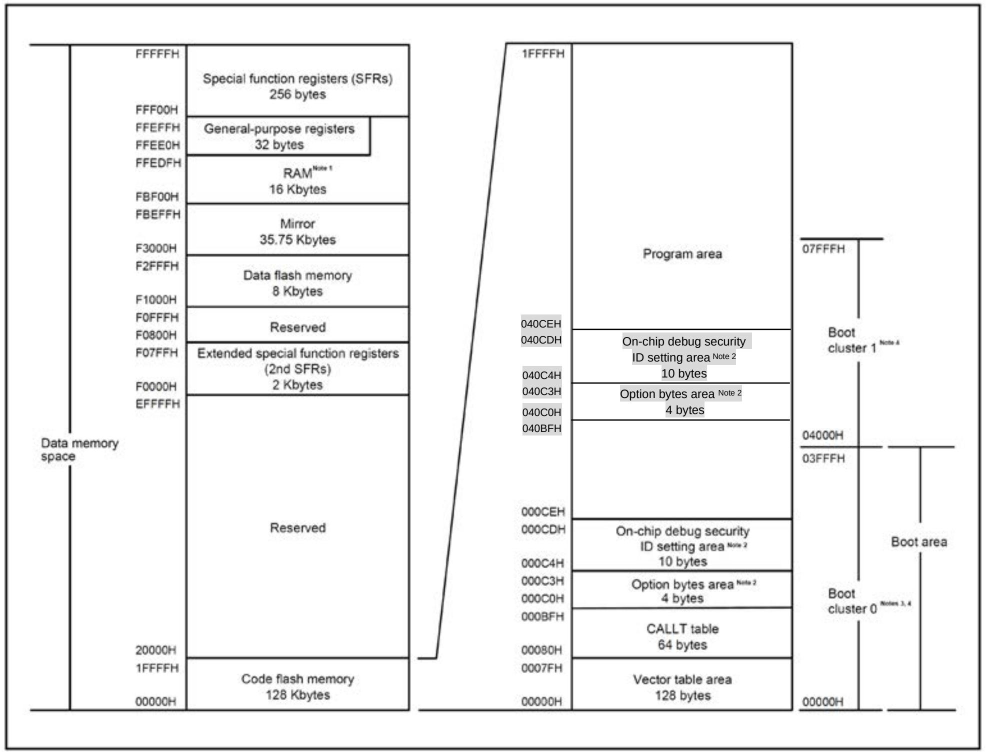
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 2 Memory Map (R7F100GxG (x = A, B, C, E, F, G, J, L, M, P))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

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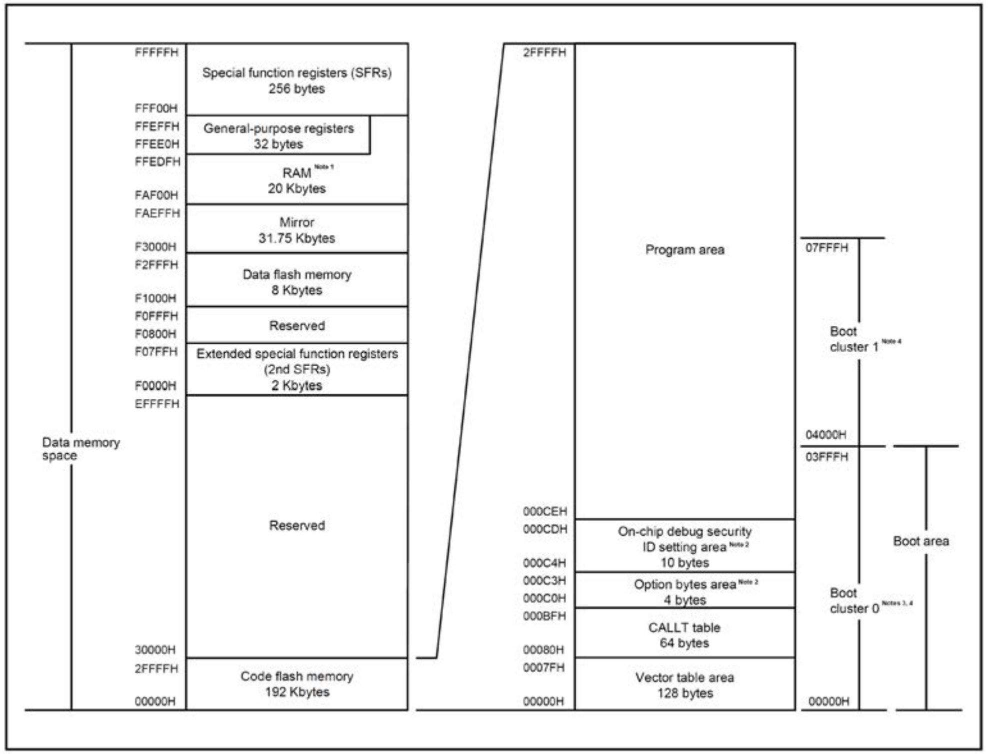
Figure 3 - 3 Memory Map (R7F100GxH (x = A, B, C, E, F, G, J, L, M, P))



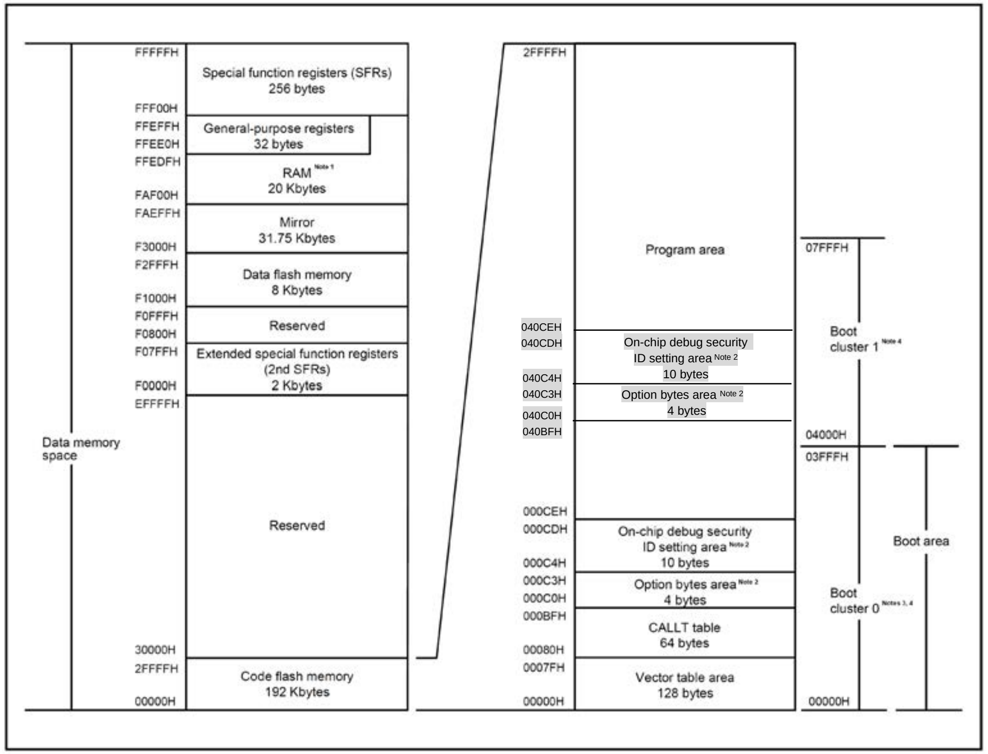
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 3 Memory Map (R7F100GxH (x = A, B, C, E, F, G, J, L, M, P))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

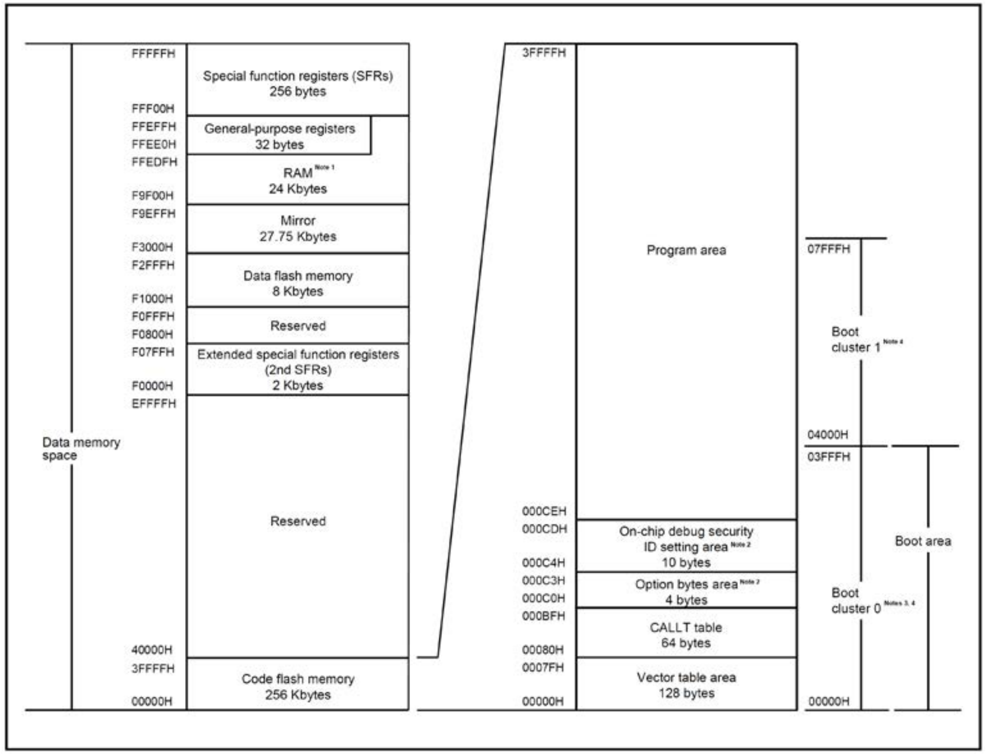
Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 150)

Figure 3 - 4 Memory Map (R7F100GxJ (x = A, B, C, E, F, G, J, L, M, P, S))



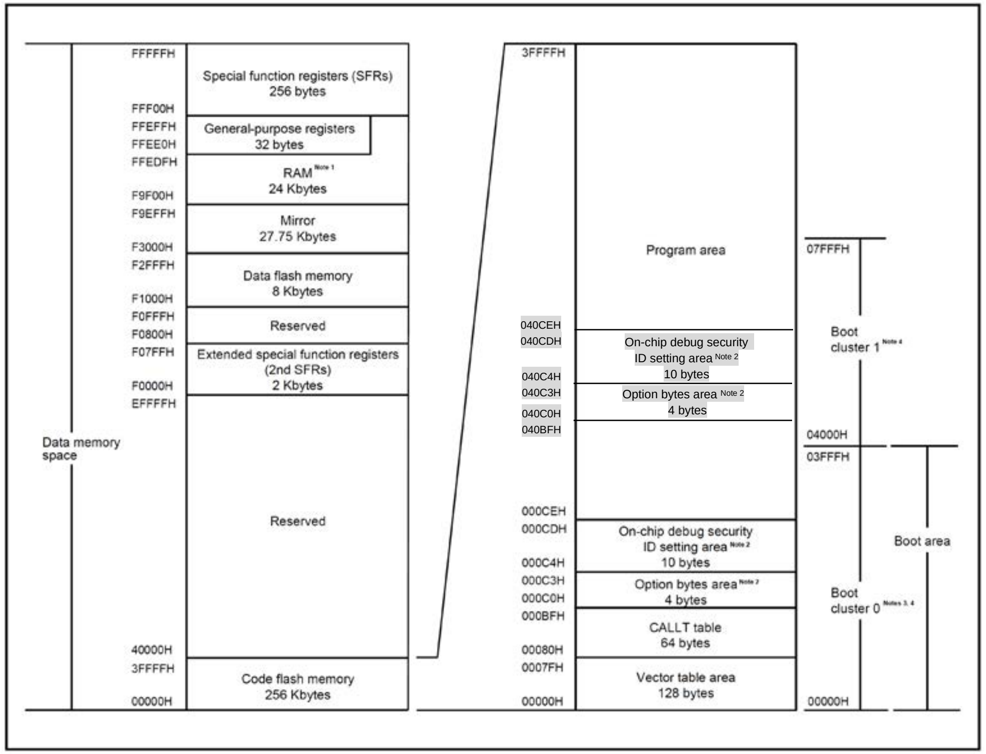
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 4 Memory Map (R7F100GxJ (x = A, B, C, E, F, G, J, L, M, P, S))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

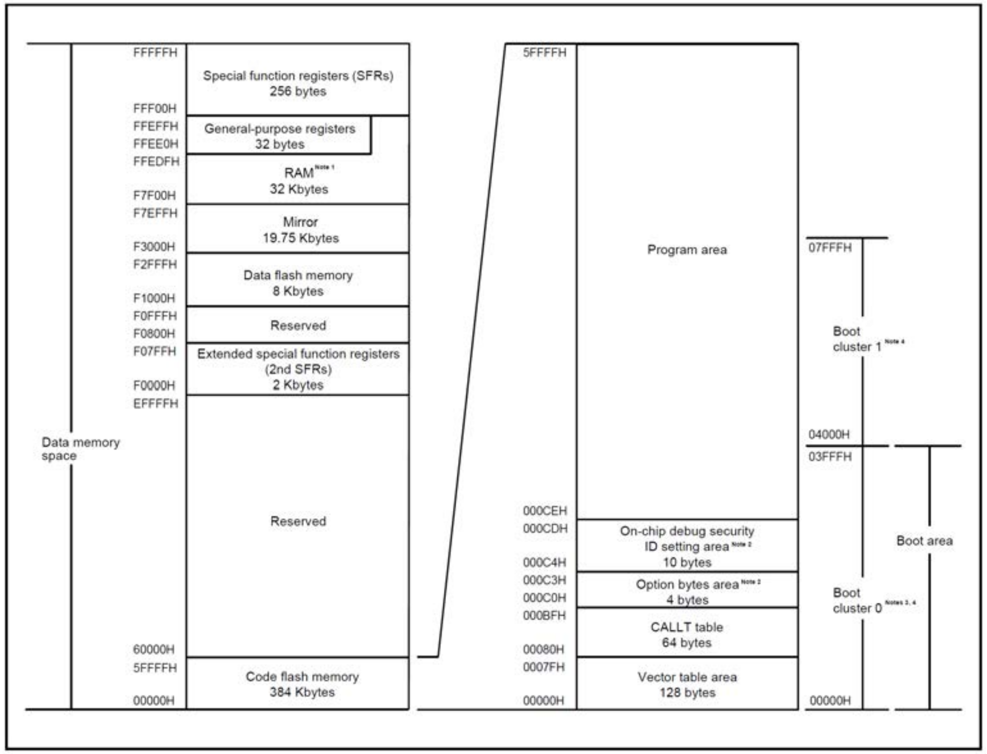
Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 151)

Figure 3 - 5 Memory Map (R7F100GxK (x = F, G, J, L, M, P, S))



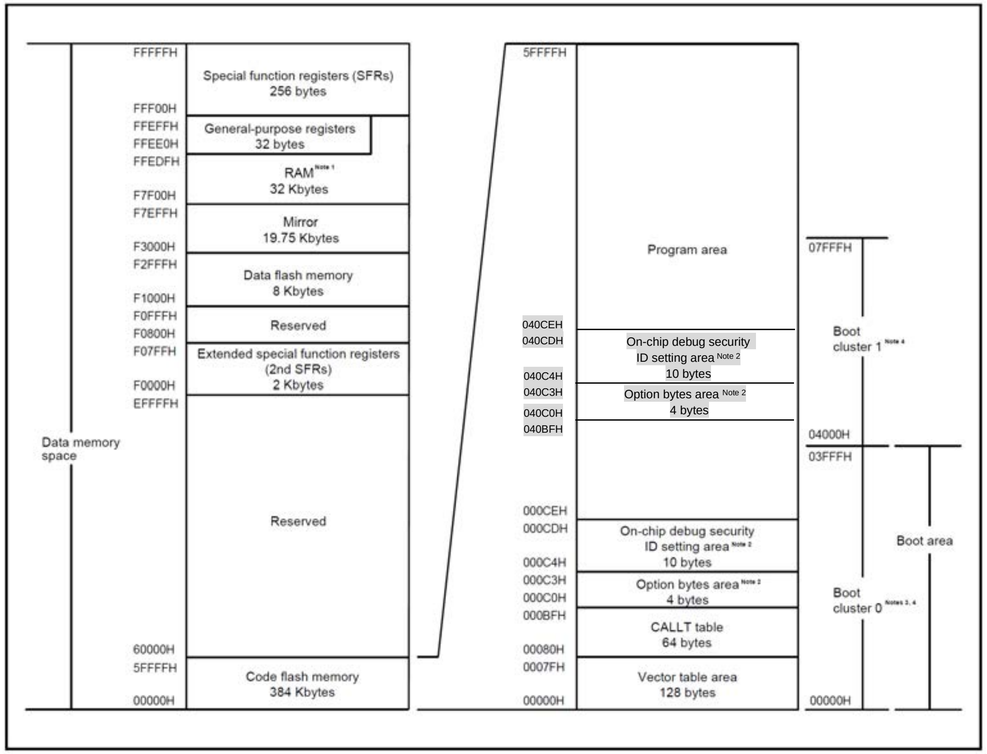
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 5 Memory Map (R7F100GxK (x = F, G, J, L, M, P, S))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

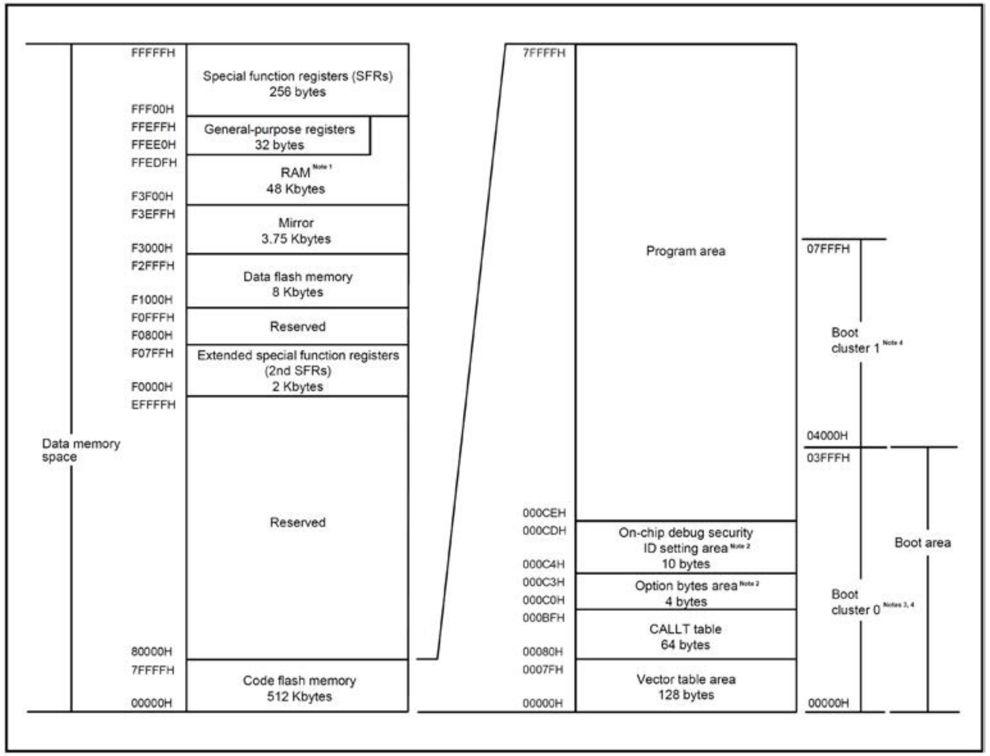
Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 152)

Figure 3 - 6 Memory Map (R7F100GxL (x = F, G, J, L, M, P, S))

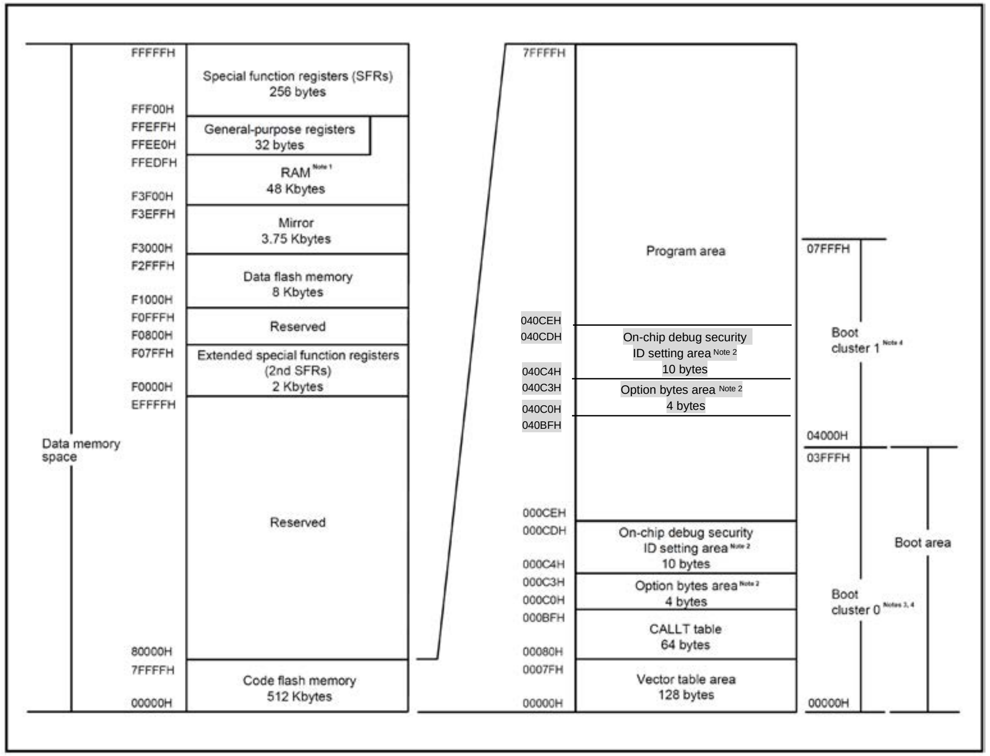


Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 6 Memory Map (R7F100GxL (x = F, G, J, L, M, P, S))



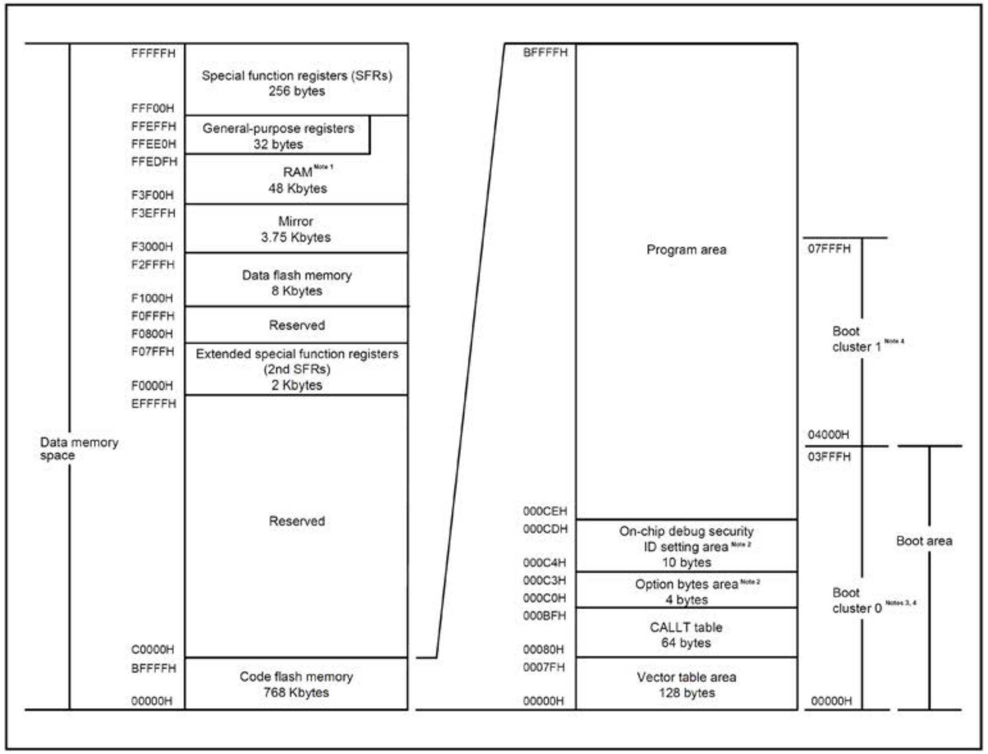
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 153)

Figure 3 - 7 Memory Map (R7F100GxN (x = F, G, J, L, M, P, S))



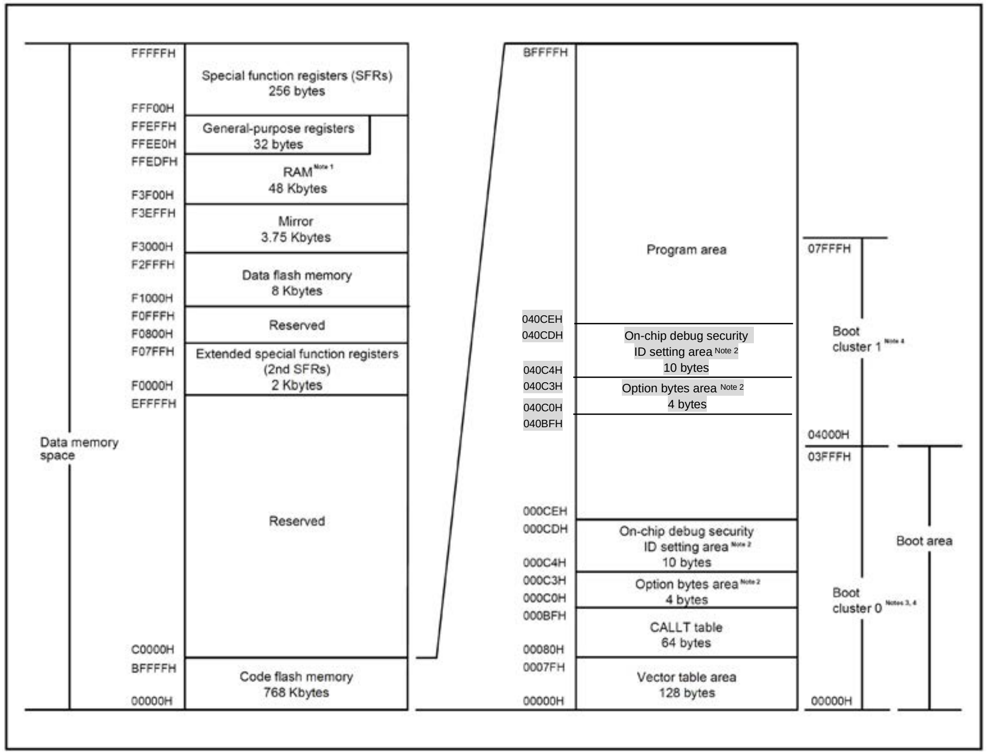
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 7 Memory Map (R7F100GxN (x = F, G, J, L, M, P, S))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 160)

(omitted)

3. Option bytes area

   A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when **the boot swap is used**. For details, see Section 32 Option Bytes.

4. On-chip debug security ID setting area

   A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. **Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when the boot swap is not used and at 000C4H to 000CDH and at 040C4H to 040CDH when the boot swap is used.** For details, see Section 34 On-chip Debugging.

(omitted)

3. Option bytes area

   A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0. For details, see Section 32 Option Bytes.

4. On-chip debug security ID setting area

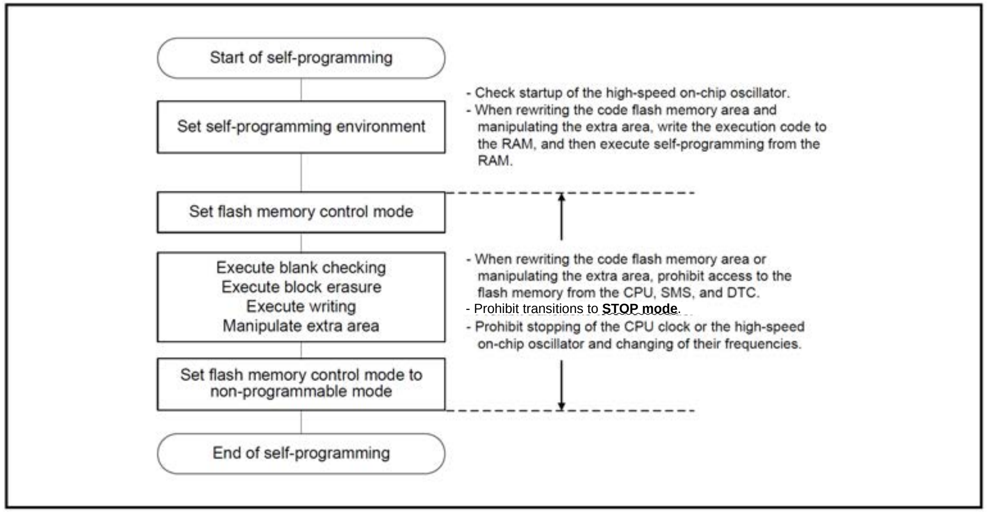
   A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. Set the 10−byte security ID for on-chip debugging at 000C4H to 000CDH when boot swapping is not to be used, that is, the value of the BTFLG bit in the FLSEC register is 1, and at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0. For details, see Section 34 On-chip Debugging.

2. 33.6.1 Self-programming procedure (Page 1315)

Incorrect:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 33.6.2 Registers to control the flash memory.

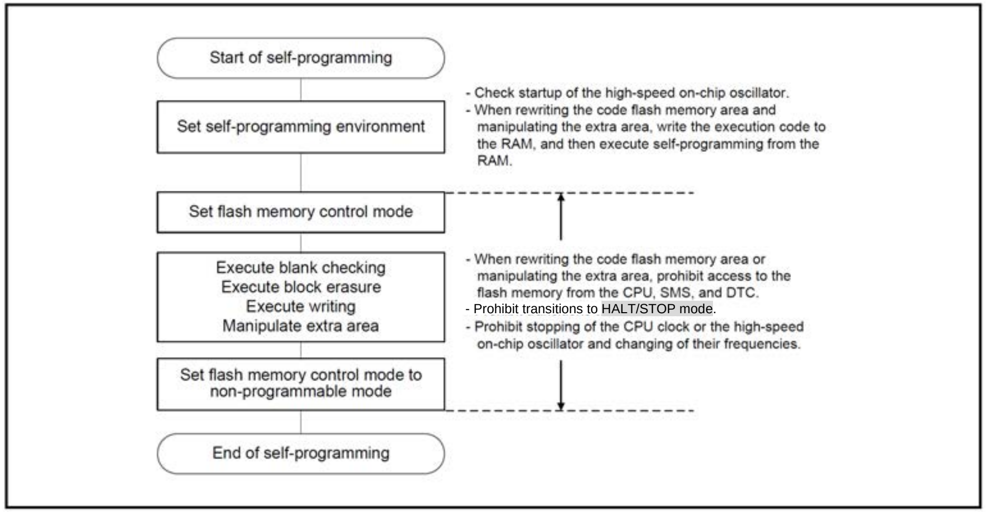
Figure 33 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



Correct:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 33.6.2 Registers to control the flash memory.

Figure 33 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



3. 33.10.1 Overview of the data flash memory (Page 1366)

Incorrect:

An overview of the data flash memory is provided below.

(omitted)

- Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.
- Transition to the **STOP mode** is prohibited while rewriting the data flash memory.

(omitted)

Correct:

An overview of the data flash memory is provided below.

(omitted)

- Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.
- Transition to the HALT/STOP mode is prohibited while rewriting the data flash memory.

(omitted)

4. 34.3 Security Settings for On-chip Debugging (Page 1369)

Incorrect:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 33.9 Security Settings in Section 33 Flash Memory).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 32 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.[Note 1]

Table 34 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID code[Note 2]
040C4H to 040CDH	

Note 1. The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.

Note 2. The setting FFFFFFFFFFFFFFFFFFFFH is not allowed.

Correct:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 33.9 Security Settings in Section 33 Flash Memory).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 32 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.[Note]

Note The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.

Table 34 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID code[Note 2, 3]
040C4H to 040CDH	

Note 1. The setting FFFFFFFFFFFFFFFFFFFFH is not allowed.

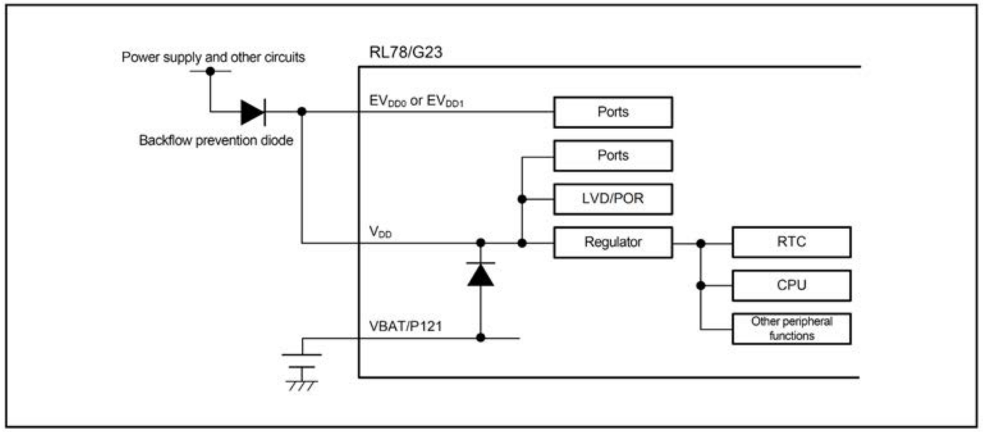
Note 2. Set the 10-byte security ID for on-chip debugging at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0.

5. 2.2.3.2 Connecting the VBAT pin to the battery for use in backing up (Page 106)

Incorrect:

(omitted)

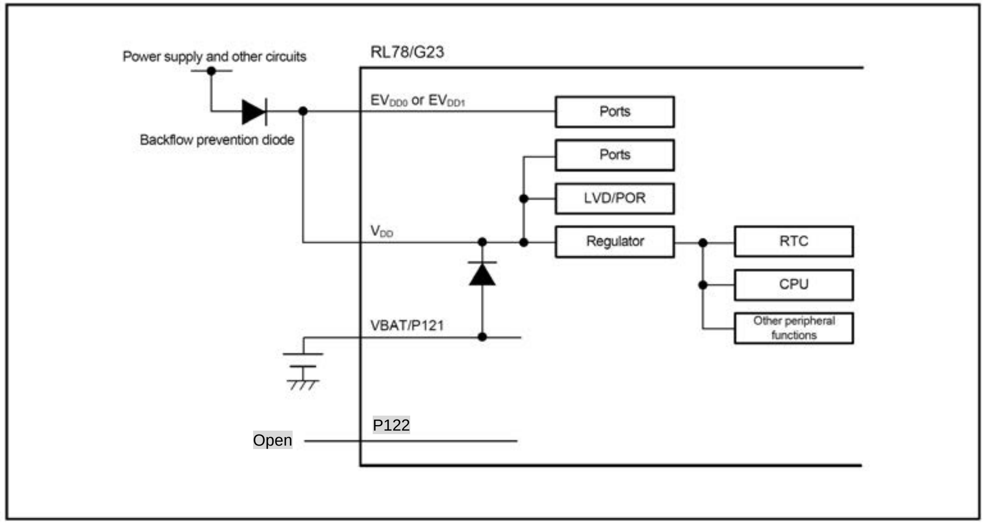
Figure 2 - 1 Example of the Connection of the VBAT Pin



Correct:

(omitted)

Figure 2 - 1 Example of the Connection of the VBAT Pin



6. 2.2.3.3 Using the VBAT pin (Page 107)

Incorrect:

How to make the initial settings for the VBAT pin and an example of the procedure for switching the power supply pin to the VBAT pin are described below. This processing is to be completed before the voltage on the VDD pin falls below that supplied from the VBAT pin. In addition, **Figure 2 - 2** shows the state transitions in switching the power supply pin between the VDD and VBAT pins.

1. Making the initial settings for the VBAT pin
   Set the P121 pin to X1 oscillation mode (by setting the EXCLK and OSCSEL bits of the CMC register to 0 and 1, respectively, and the MSTOP bit of the CSC register to **0**) in the initial settings.

(omitted)

Correct:

How to make the initial settings for the VBAT pin and an example of the procedure for switching the power supply pin to the VBAT pin are described below. This processing is to be completed before the voltage on the VDD pin falls below that supplied from the VBAT pin. In addition, **Figure 2 - 2** shows the state transitions in switching the power supply pin between the VDD and VBAT pins.

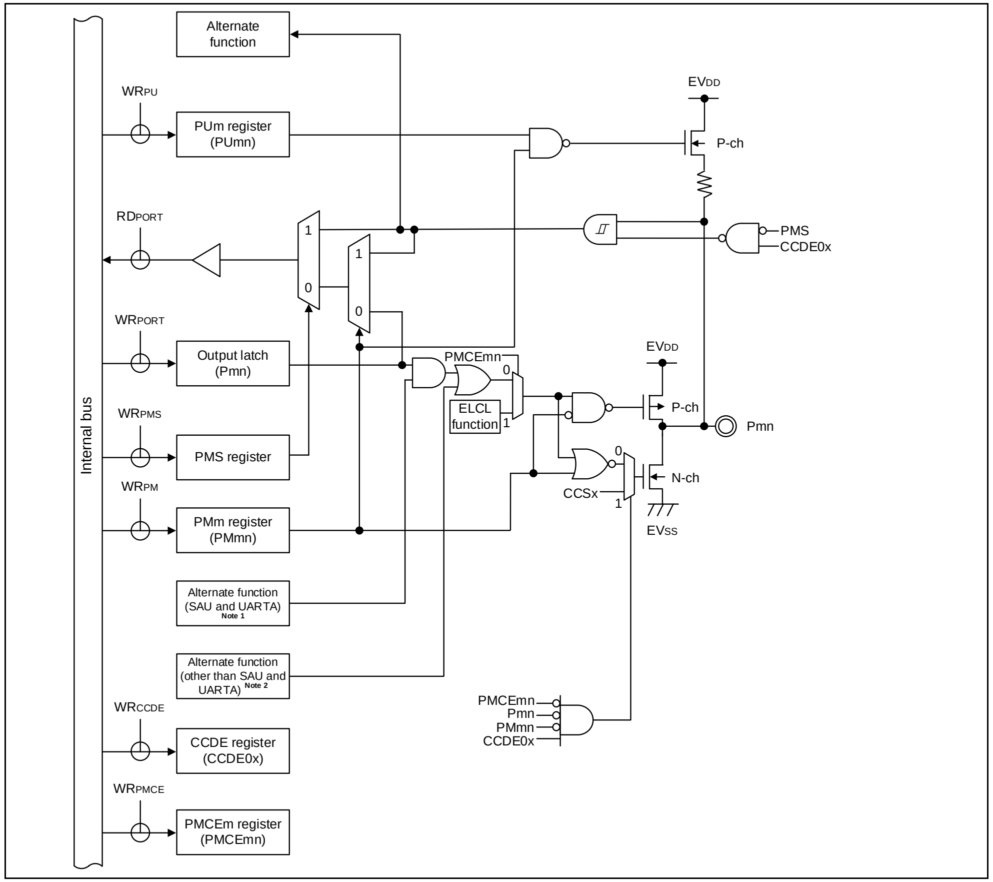
1. Making the initial settings for the VBAT pin
   Set the P121 pin to X1 oscillation mode (by setting the EXCLK and OSCSEL bits of the CMC register to 0 and 1, respectively, and the MSTOP bit of the CSC register to 1) in the initial settings.

(omitted)

7. 2.4 Block Diagrams of Pins (Page 125, Page 126, Page 132, Page 135, Page 138 to Page 141, Page 143 to Page 145)

Incorrect:
(Page 125)

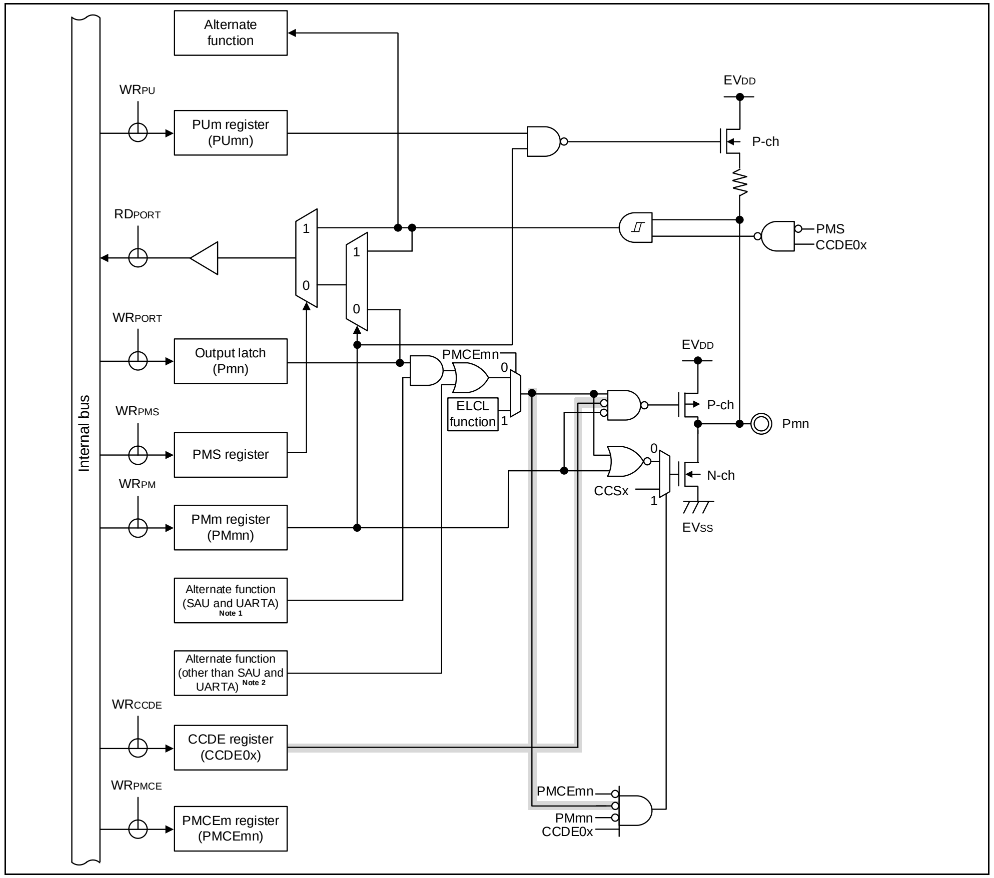
Figure 2 - 21 Pin Block Diagram for Pin Type 7-38-1



(omitted)

Correct:

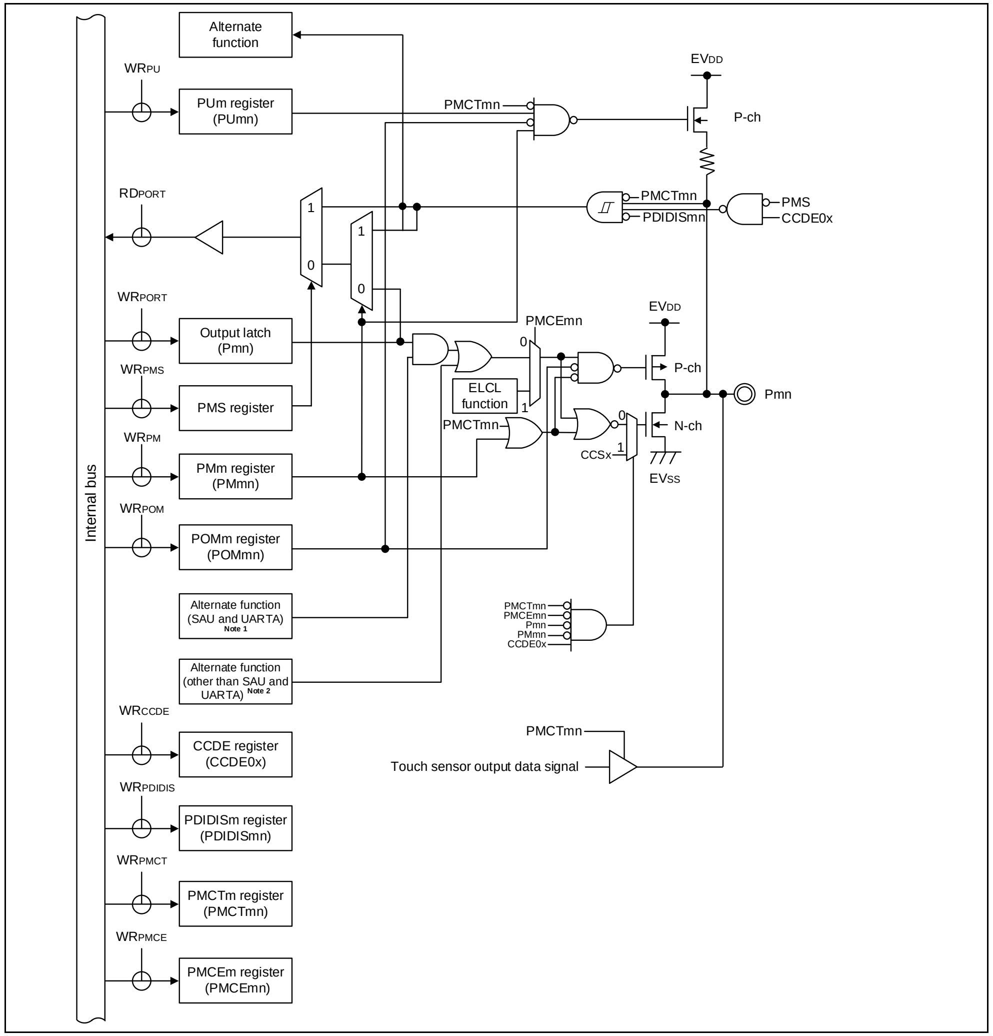
Figure 2 - 21 Pin Block Diagram for Pin Type 7-38-1



(omitted)

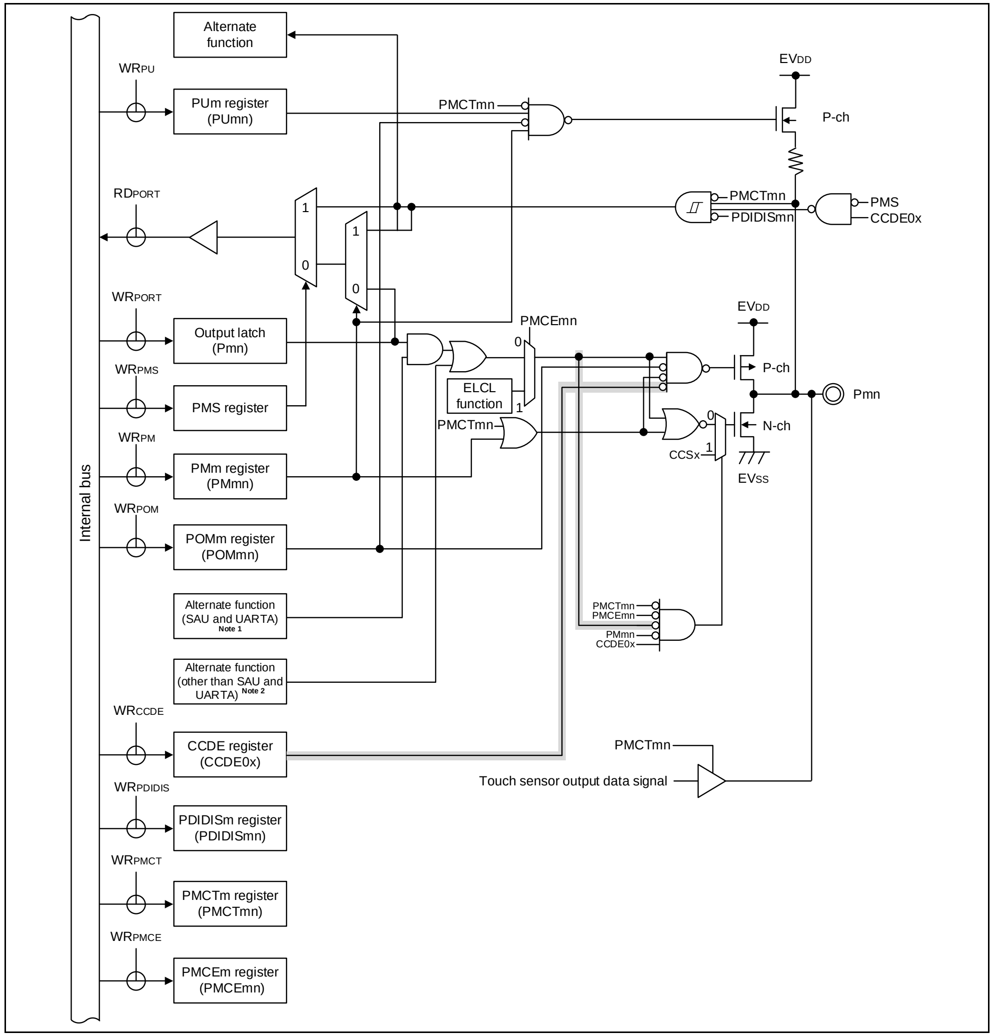
(Page 126)

Figure 2 - 22 Pin Block Diagram for Pin Type 7-39-1



(omitted)

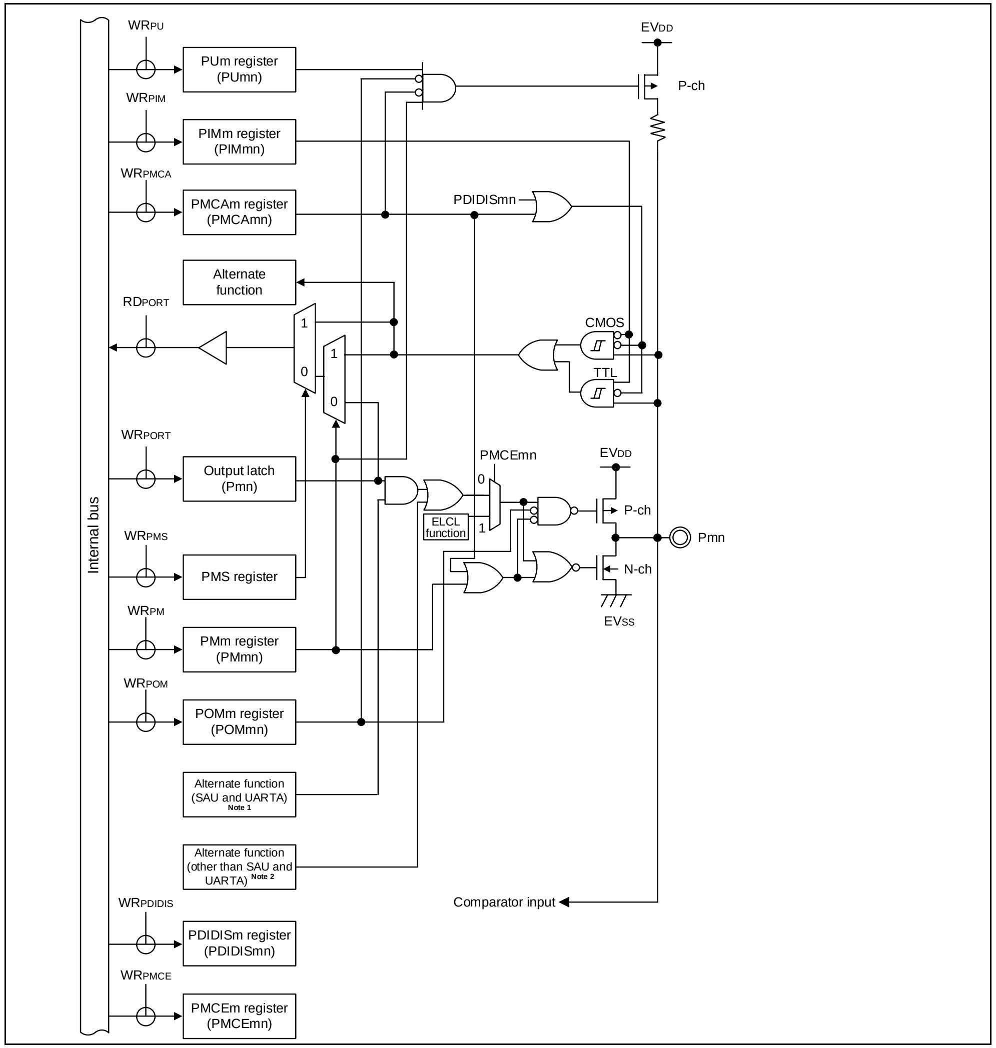
Figure 2 - 22 Pin Block Diagram for Pin Type 7-39-1



(omitted)

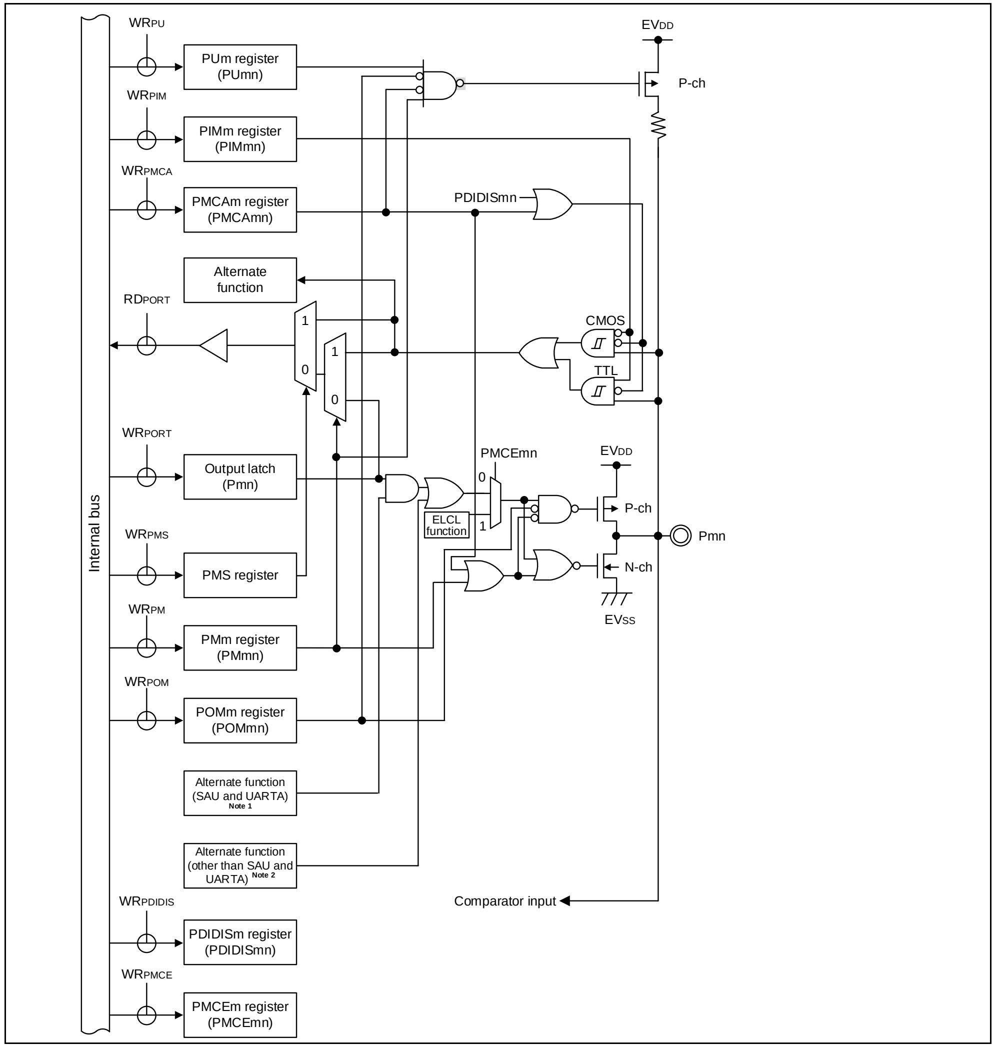
(Page 132)

Figure 2 - 26 Pin Block Diagram for Pin Type 8-6-9



(omitted)

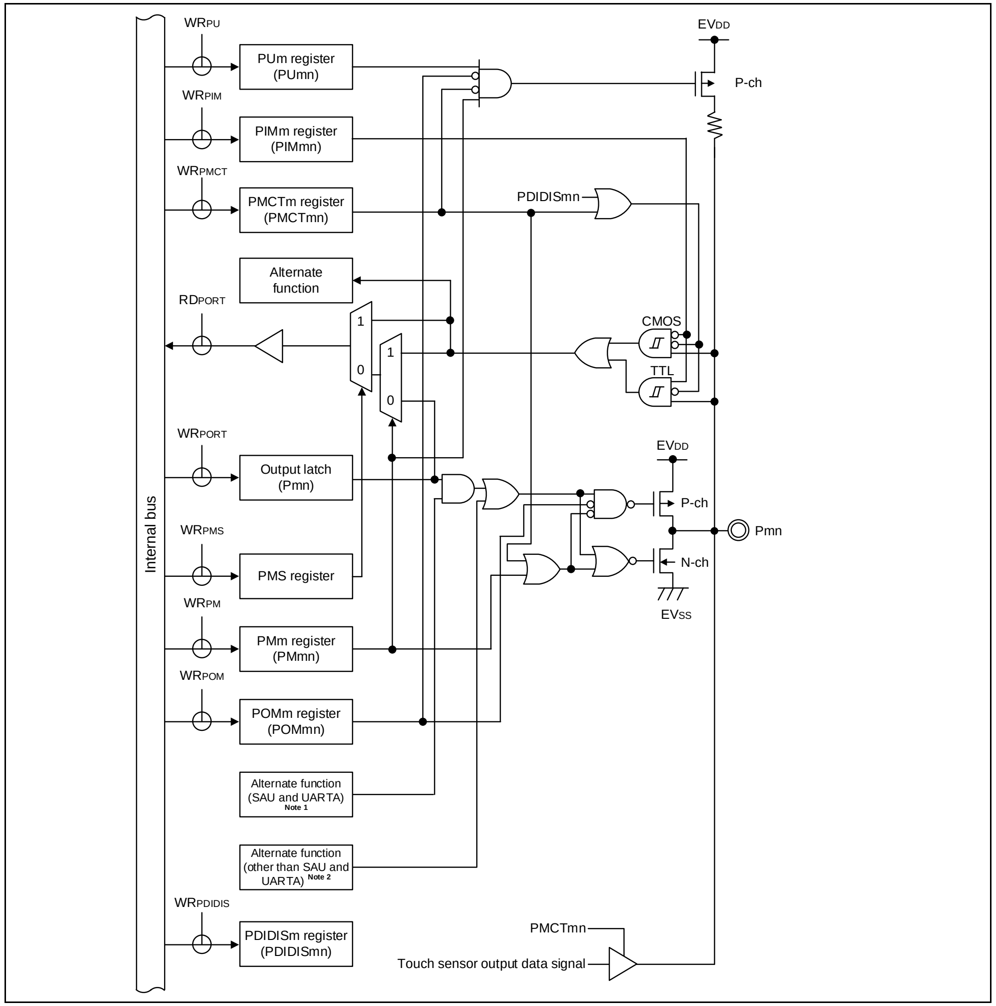
Figure 2 - 26 Pin Block Diagram for Pin Type 8-6-9



(omitted)

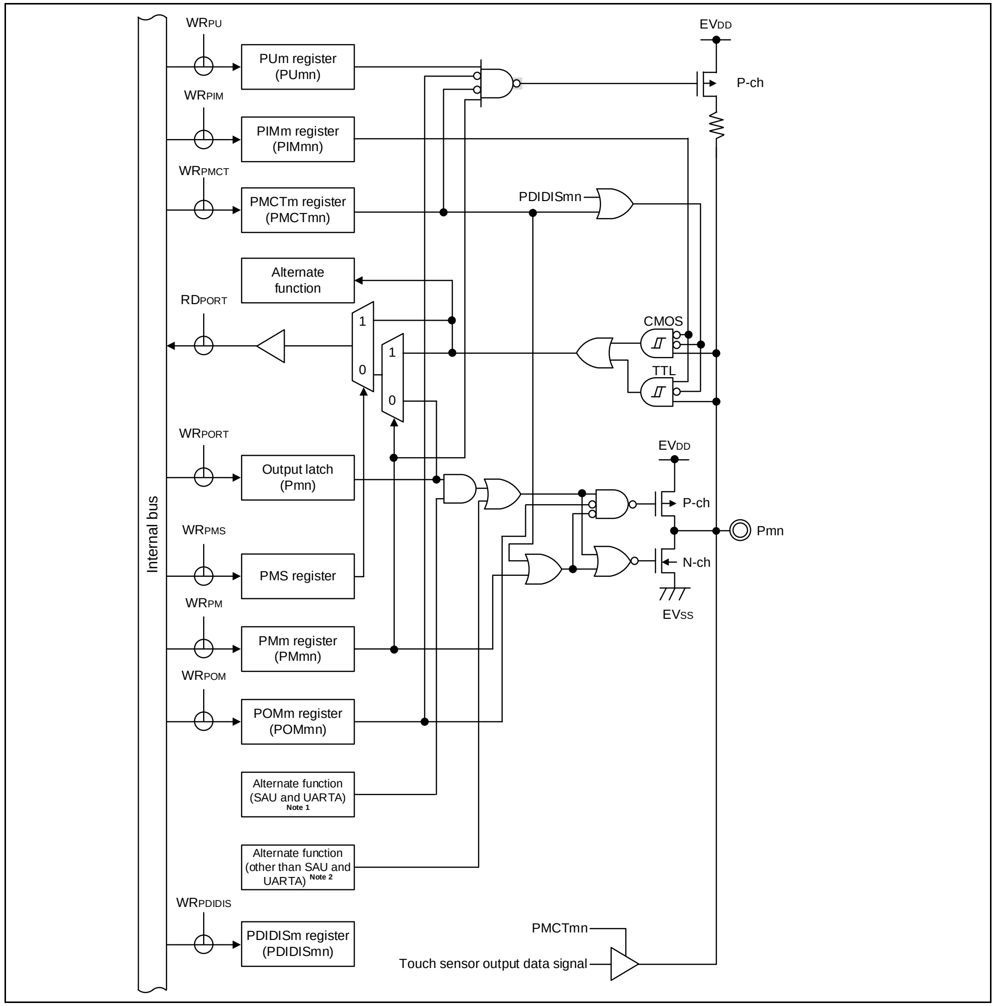
(Page 135)

Figure 2 - 28 Pin Block Diagram for Pin Type 8-31-2



(omitted)

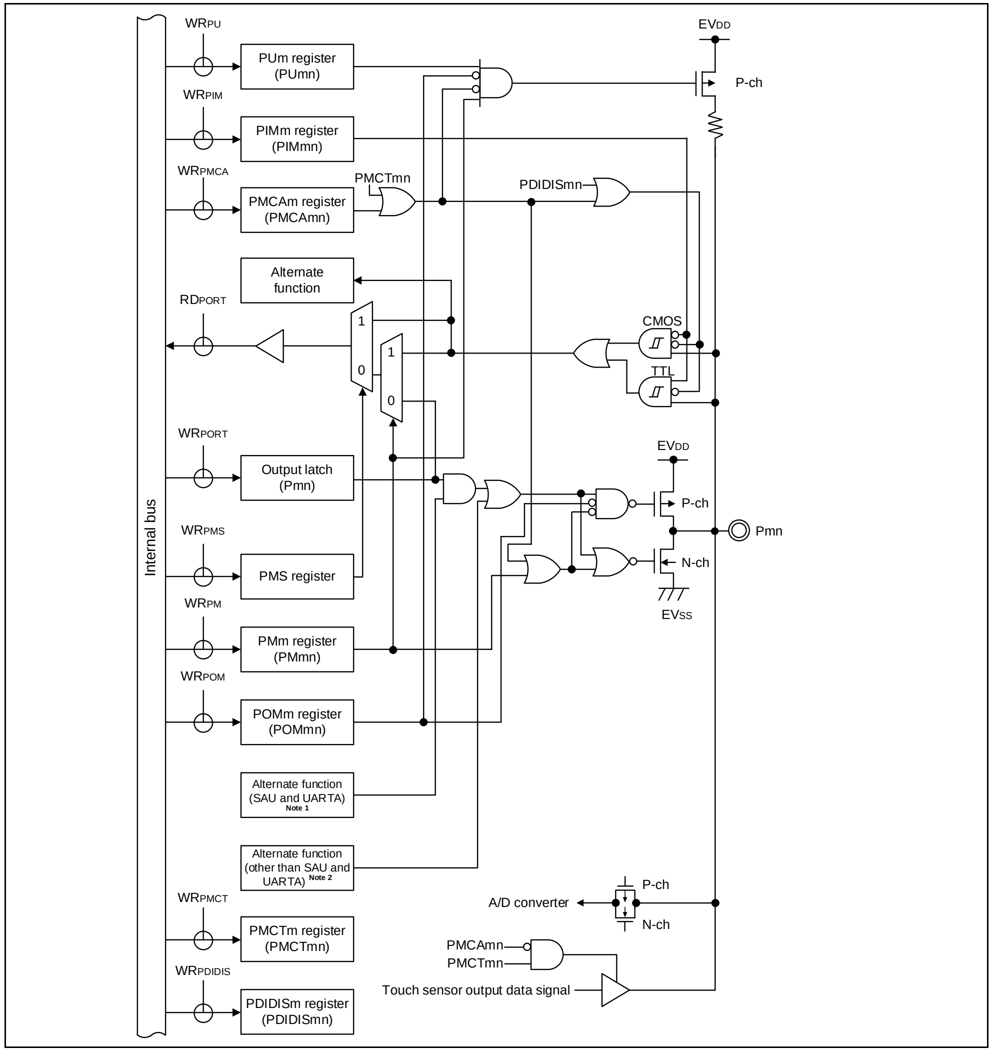
Figure 2 - 28 Pin Block Diagram for Pin Type 8-31-2



(omitted)

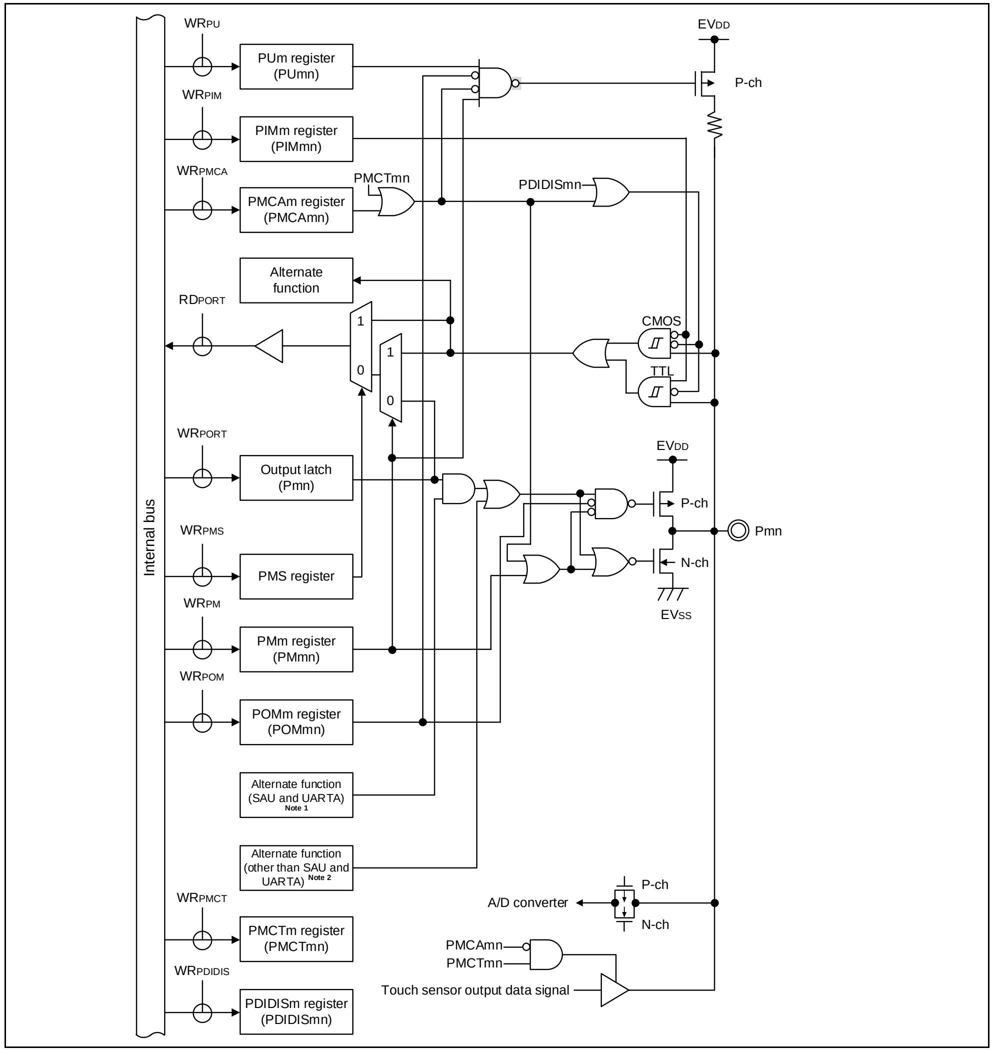
(Page 138)

Figure 2 - 30 Pin Block Diagram for Pin Type 8-33-3



(omitted)

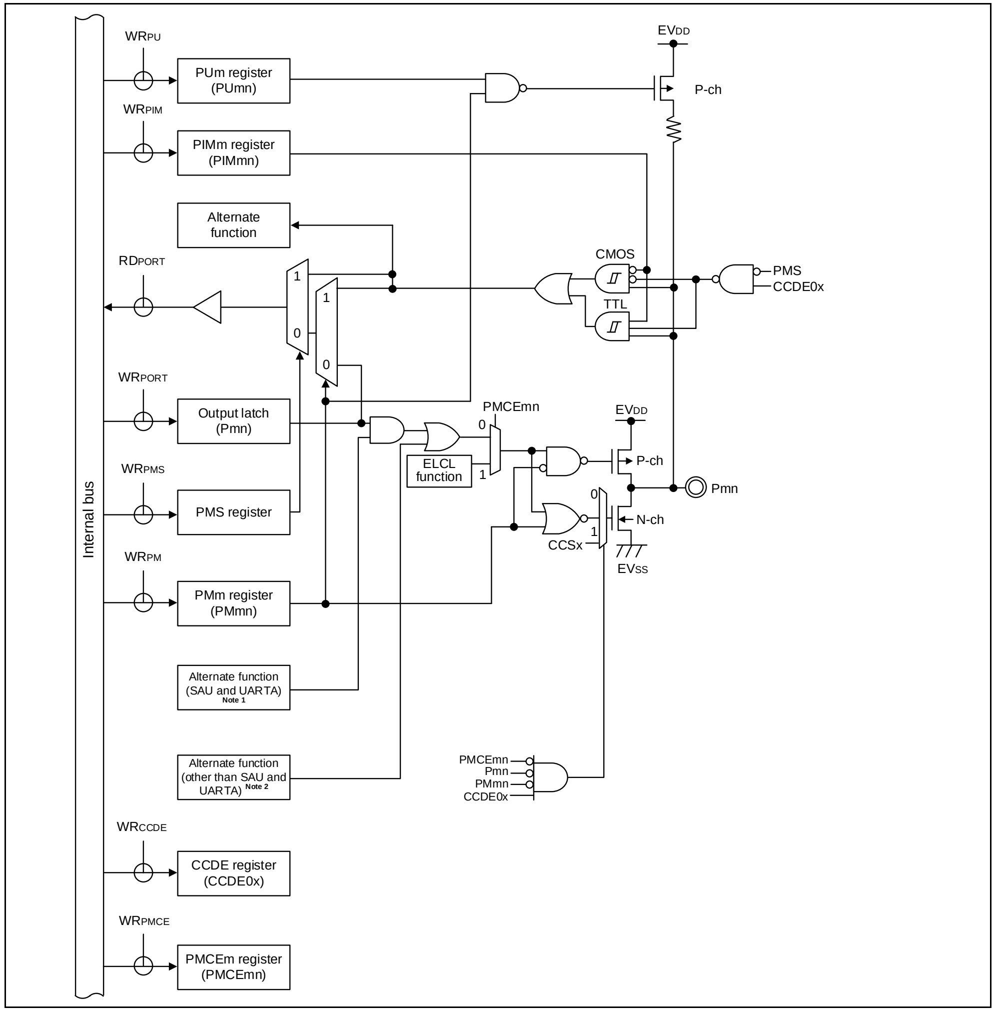
Figure 2 - 30 Pin Block Diagram for Pin Type 8-33-3



(omitted)

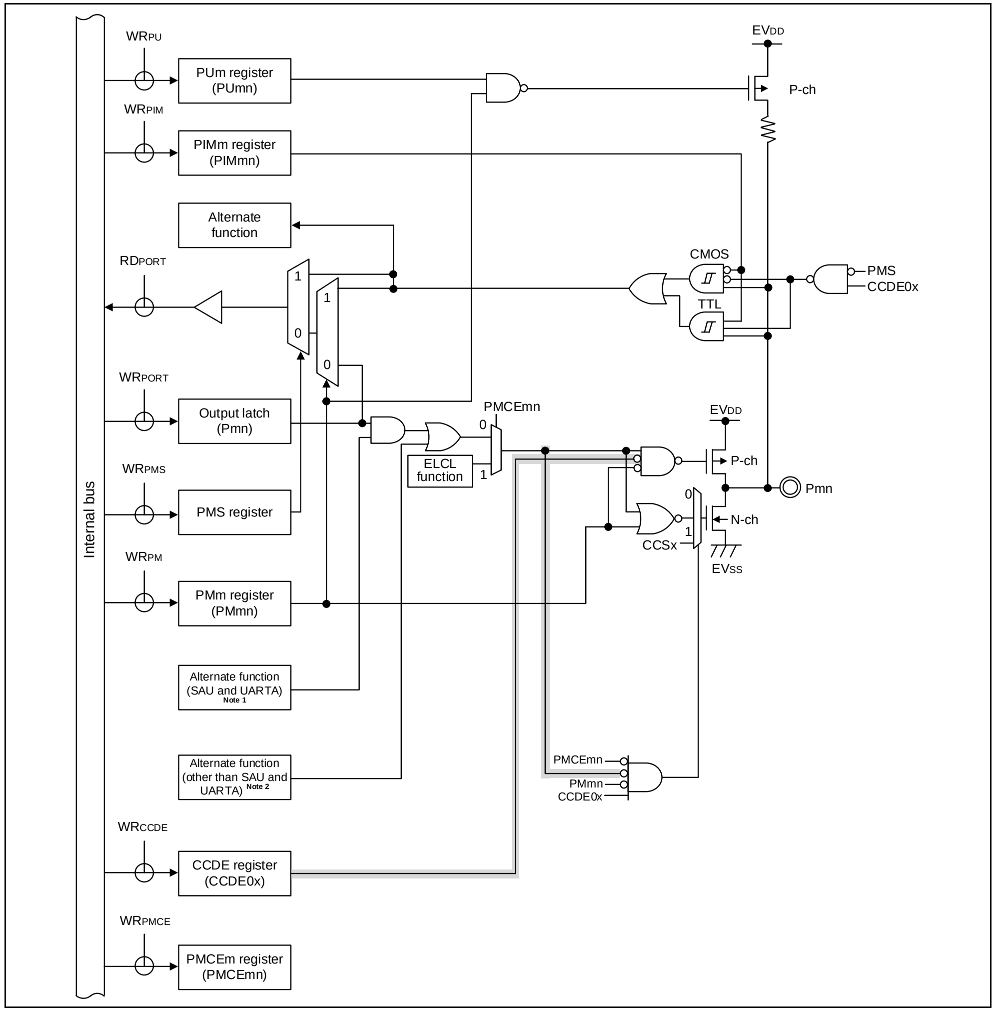
(Page 140)

Figure 2 - 31 Pin Block Diagram for Pin Type 8-38-1



(omitted)

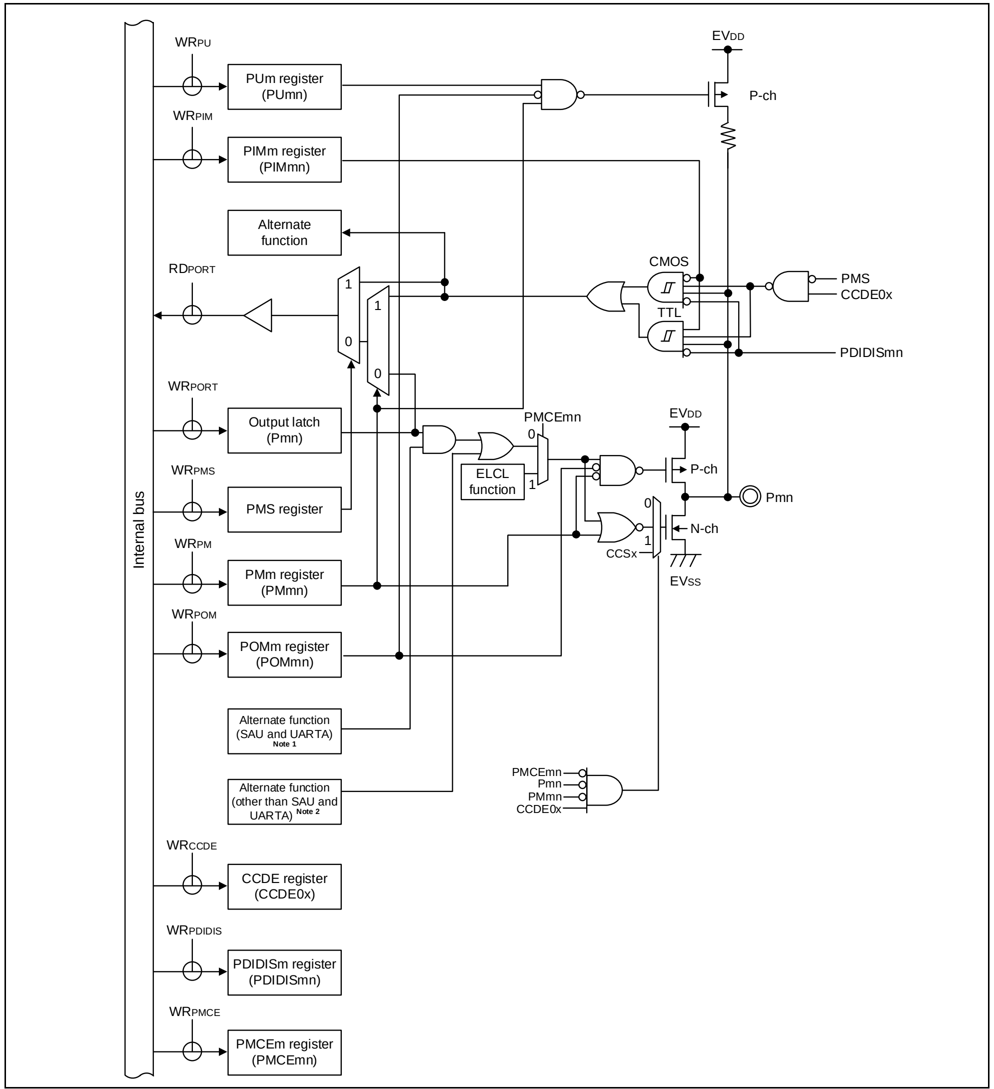
Figure 2 - 31 Pin Block Diagram for Pin Type 8-38-1



(omitted)

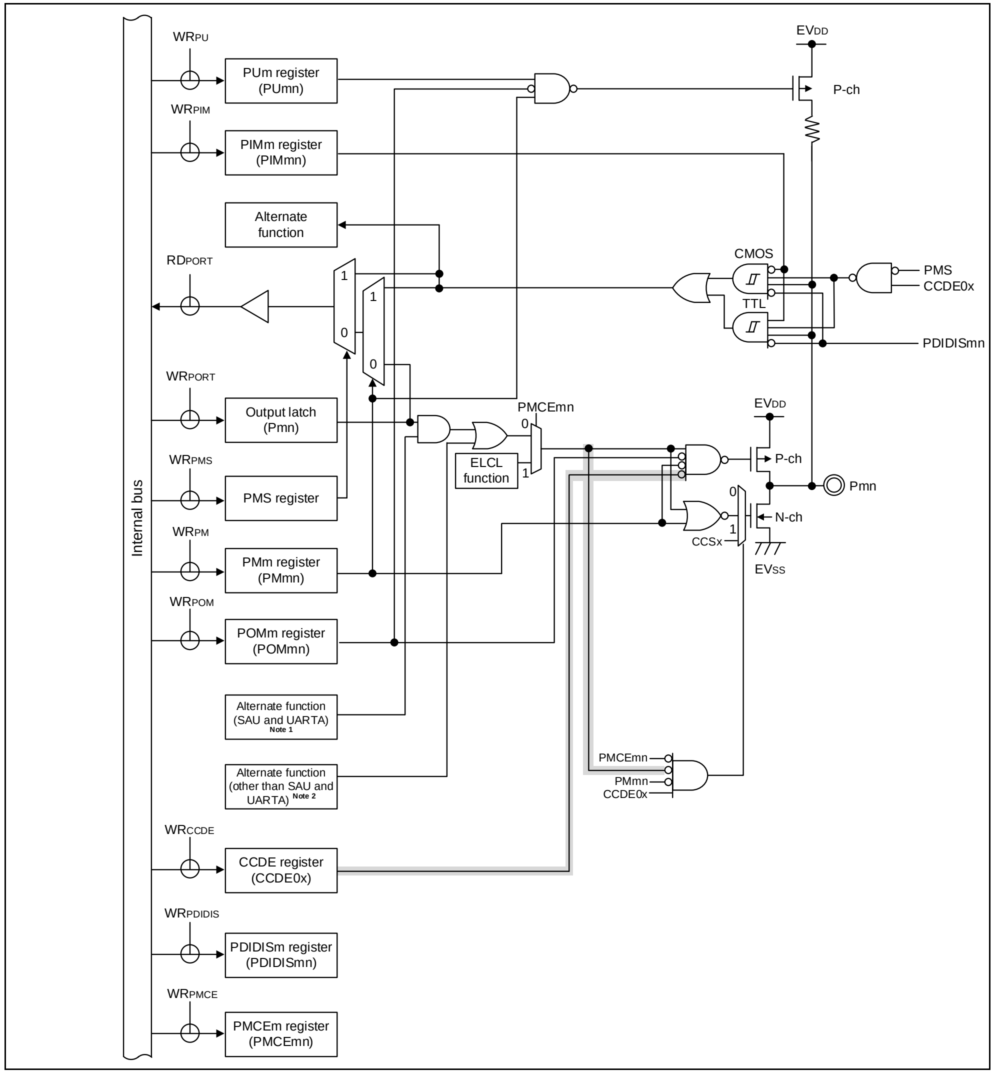
(Page 141)

Figure 2 - 32 Pin Block Diagram for Pin Type 8-38-2



(omitted)

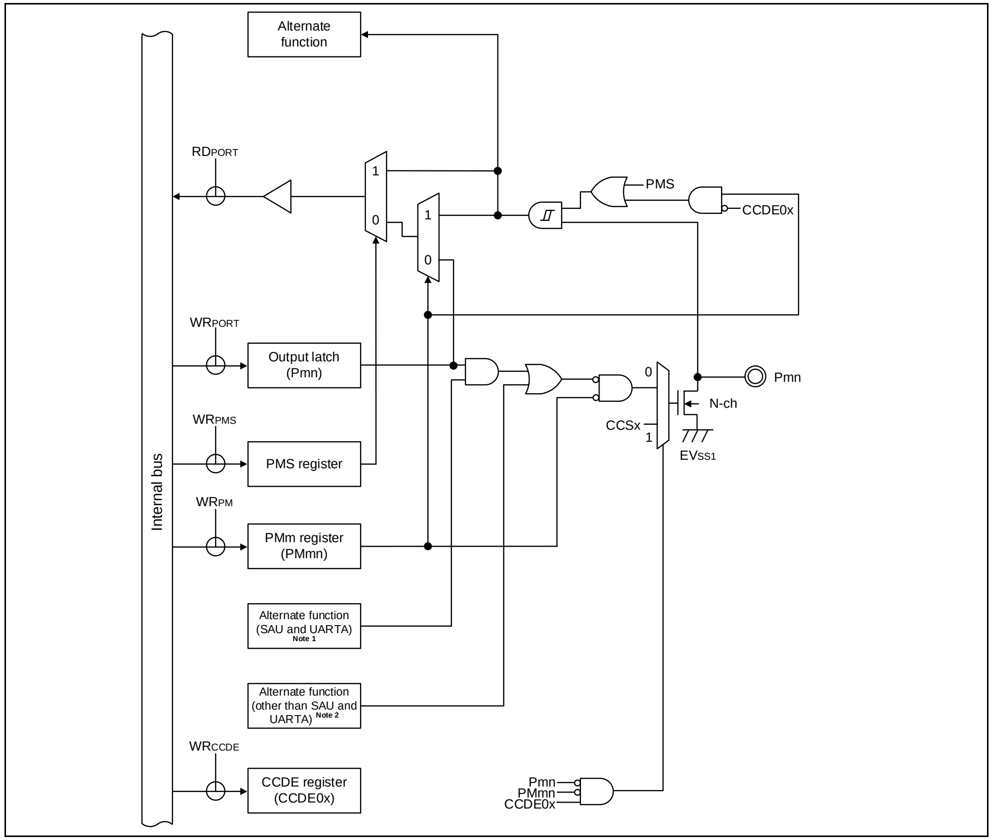
Figure 2 - 32 Pin Block Diagram for Pin Type 8-38-2



(omitted)

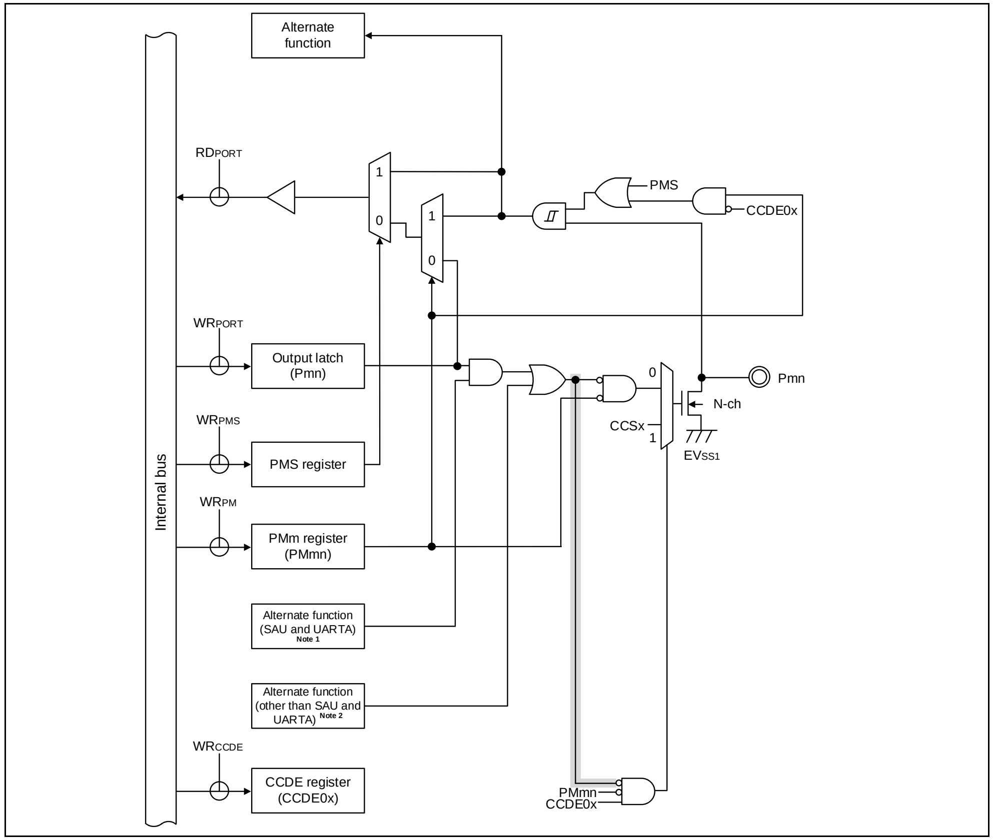
(Page 143)

Figure 2 - 33 Pin Block Diagram for Pin Type 12-38-1



(omitted)

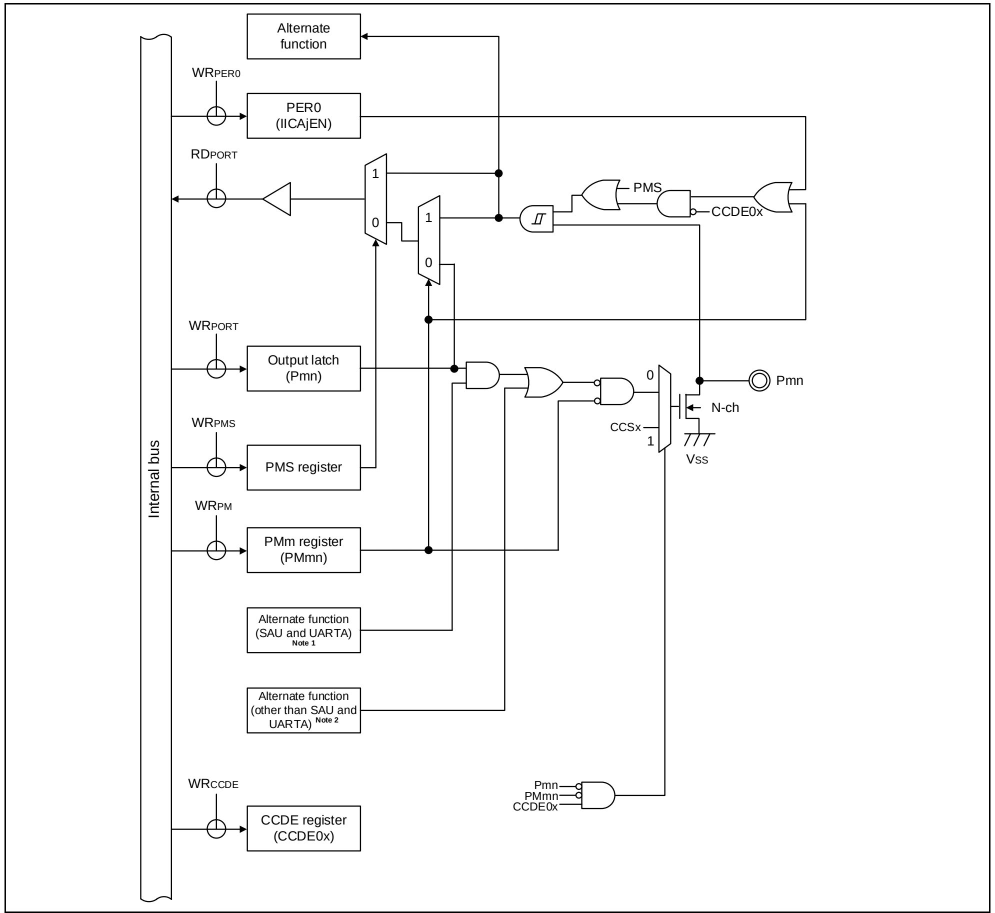
Figure 2 - 33 Pin Block Diagram for Pin Type 12-38-1



(omitted)

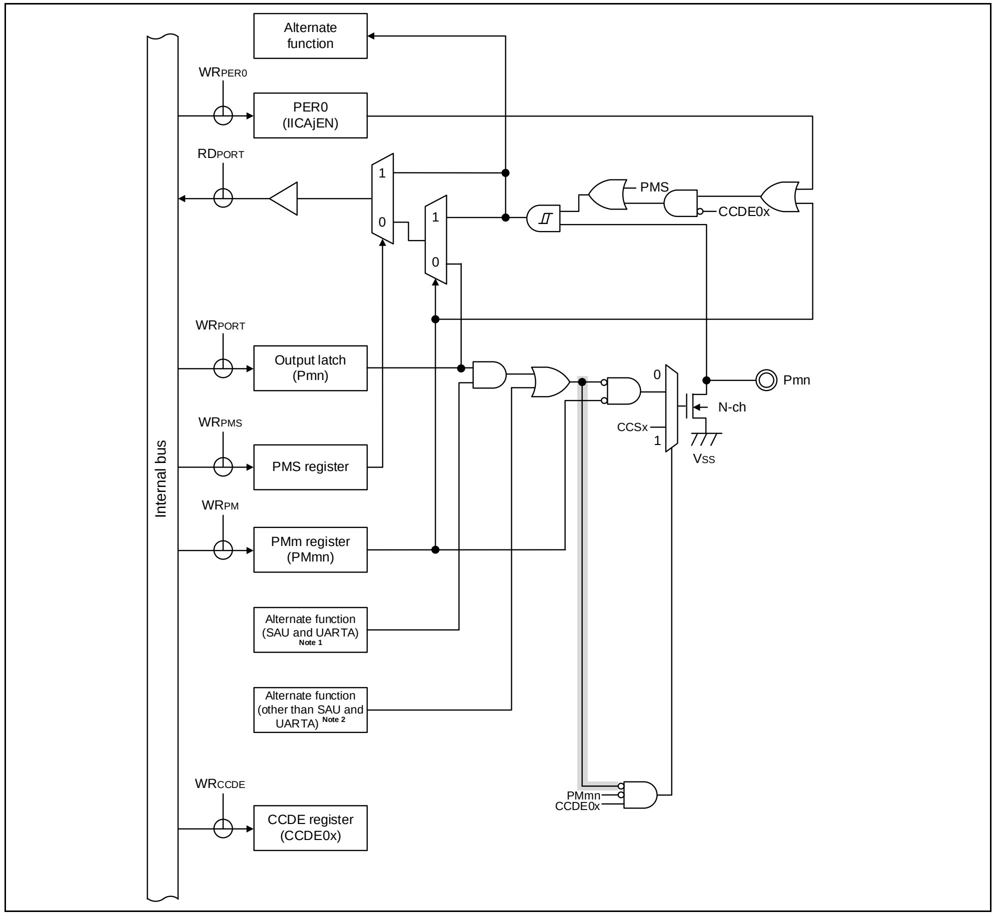
(Page 144)

Figure 2 - 34 Pin Block Diagram for Pin Type 12-38-2



(omitted)

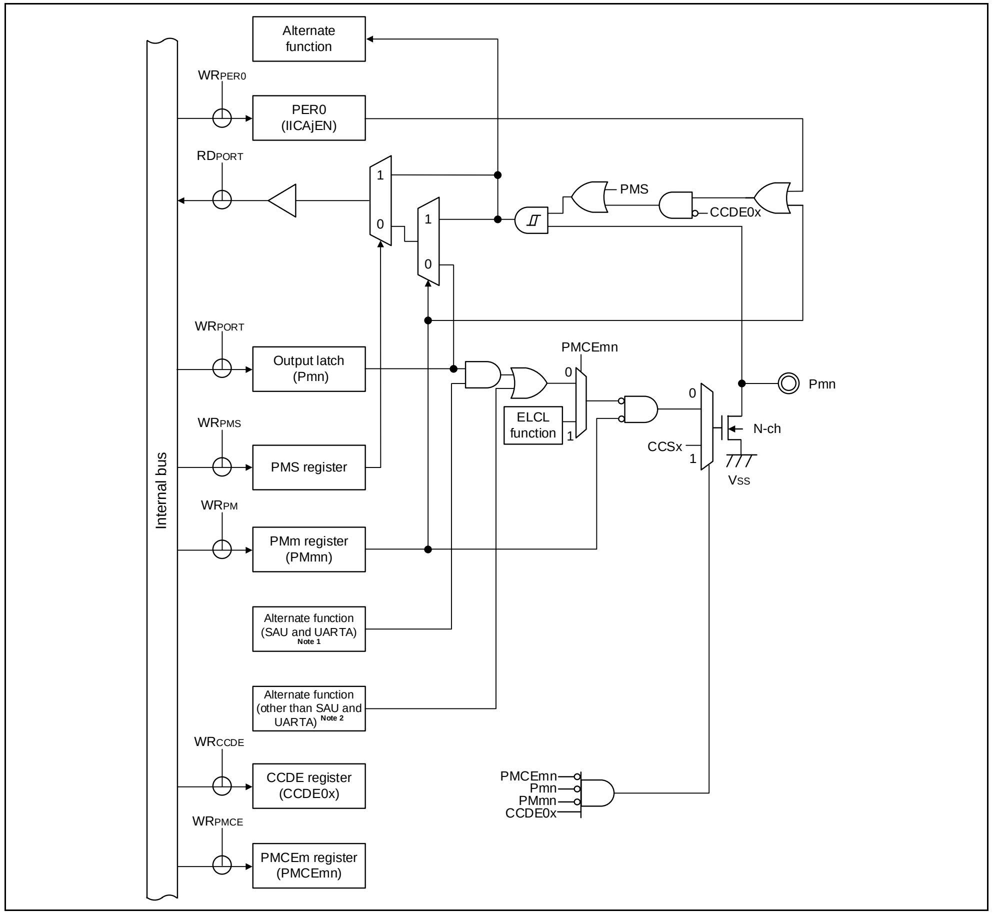
Figure 2 - 34 Pin Block Diagram for Pin Type 12-38-2



(omitted)

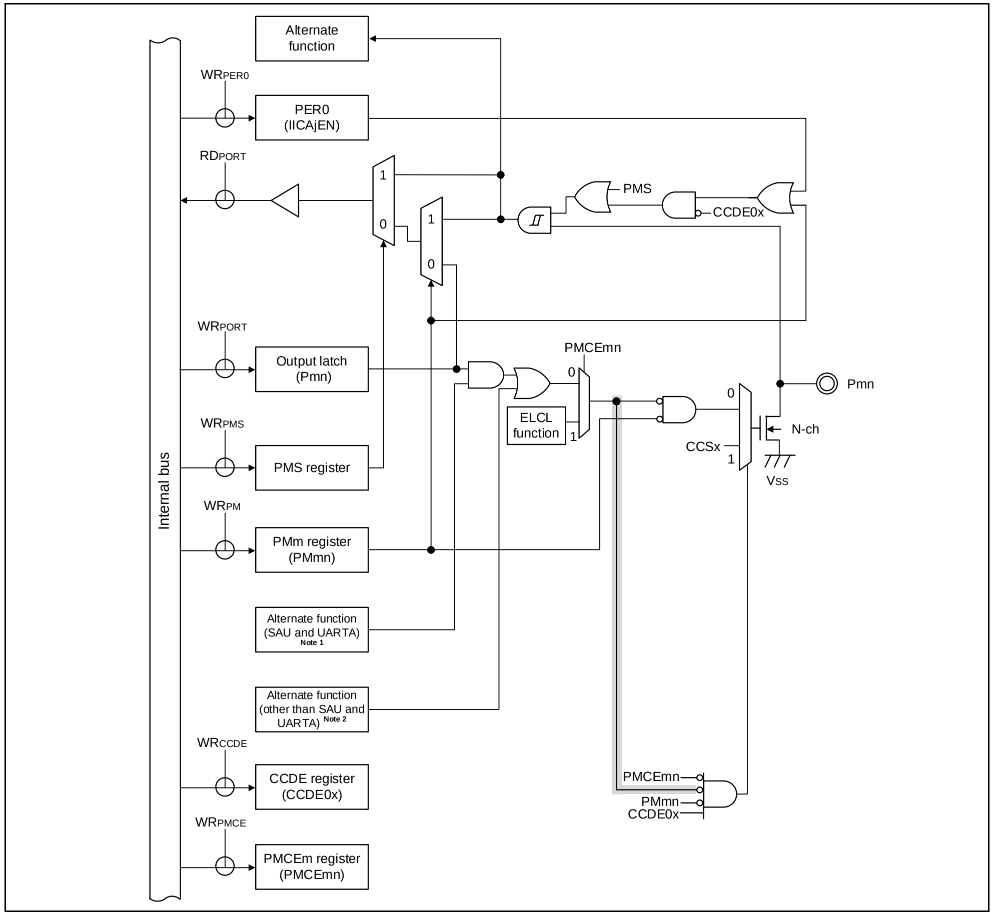
(Page 145)

Figure 2 - 35 Pin Block Diagram for Pin Type 12-38-3



(omitted)

Figure 2 - 35 Pin Block Diagram for Pin Type 12-38-3



(omitted)

8. 4.5.4 Examples of register settings for port and alternate functions (Page 262, Page 281)

Incorrect:
(Page 262)

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-pin to 64-pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (14/16)

Pin Name	Function Used: Function Name	Function Used: I/O	CMC: EXCLK, OSCSEL, EXCLKS, OSCSELS	CMC: XTSEL	PMxx	Pxx	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin
P121	P121	Input	00 xx / 10 xx / 11 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note										
		Output	00 xx / 10 xx / 11 xx	0	0	0/1								
			xx 00 / xx 10 / xx 11	1Note										
	EI121	Input	00 xx / 10 xx / 11 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note										
	VBAT	Input	00 xx / 10 xx / 11 xx	0	0	1	—	—	—	✓	✓	✓	✓	✓
	X1	—	01 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓
	XT1	—	xx 01	1	1	×	✓	✓	✓	—	—	—	—	—
	EXCLKS	Input	xx 11	0	—	×	—	—	—	✓	✓	✓	✓	✓

Note This setting is only applicable in the 30- to 36-pin products.

(omitted)

Correct:

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-pin to 64-pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (14/16)

Pin Name	Function Used: Function Name	Function Used: I/O	CMC: EXCLK, OSCSEL, EXCLKS, OSCSELS	CMC: XTSEL	PMxx	Pxx	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin
P121	P121	Input	00 xx / 10 xx / 11 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note										
		Output	00 xx / 10 xx / 11 xx	0	0	0/1								
			xx 00 / xx 10 / xx 11	1Note										
	EI121	Input	00 xx / 10 xx / 11 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note										
	VBAT	—	01 xx	0	1	x	—	—	—	✓	✓	✓	✓	✓
	X1	—	01 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓
	XT1	—	xx 01	1	1	×	✓	✓	✓	—	—	—	—	—
	EXCLKS	Input	xx 11	0	—	×	—	—	—	✓	✓	✓	✓	✓

Note This setting is only applicable in the 30- to 36-pin products.

(omitted)

(Page 281)

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-pin and 100-pin Products with 128-Kbyte Flash Memory) (18/21)

Pin Name	Function Used: Function Name	Function Used: I/O	CMC: EXCLK, OSCSEL, EXCLKS, OSCSELS	CMC: XTSEL	PMxx	Pxx	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
P121	P121	Input	00 xx / 10 xx / 11 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note													
		Output	00 xx / 10 xx / 11 xx	0	0	0/1											
			xx 00 / xx 10 / xx 11	1Note													
	EI121	Input	00 xx / 10 xx / 11 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note													
	VBAT	Input	00 xx / 10 xx / 11 xx	0	0	0	1	—	—	✓	✓	✓	✓	✓	✓	✓	✓
	X1	—	01 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	XT1	—	xx 01	1	1	×	✓	✓	✓	—	—	—	—	—	—	—	—
	EXCLKS	Input	xx 11	0	—	×	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓

Note This setting is only applicable in the 30- to 36-pin products.

(omitted)

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-pin and 100-pin Products with 128-Kbyte Flash Memory) (18/21)

Pin Name	Function Used: Function Name	Function Used: I/O	CMC: EXCLK, OSCSEL, EXCLKS, OSCSELS	CMC: XTSEL	PMxx	Pxx	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
P121	P121	Input	00 xx / 10 xx / 11 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note													
		Output	00 xx / 10 xx / 11 xx	0	0	0/1											
			xx 00 / xx 10 / xx 11	1Note													
	EI121	Input	00 xx / 10 xx / 11 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note													
	VBAT	—	01 xx	0	0	1	x	—	—	✓	✓	✓	✓	✓	✓	✓	✓
	X1	—	01 xx	0	1	×	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	XT1	—	xx 01	1	1	×	✓	✓	✓	—	—	—	—	—	—	—	—
	EXCLKS	Input	xx 11	0	—	×	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓

Note This setting is only applicable in the 30- to 36-pin products.

(omitted)

9. 12.3.8 Analog input channel specification register (ADS) (Page 574)

Incorrect:

(omitted)

Caution 7. When the setting of the ADISS bit is 1, the internal reference voltage cannot be used for the + side reference voltage. After the ADISS bit is set to 1, the initial conversion result cannot be used. For the setting flow, see 12.7.5 Example of using the ADC when selecting the temperature sensor output voltage or internal reference voltage, and software trigger no-wait mode and one-shot conversion mode. For details about the internal reference voltage, see Section 37 Electrical Characteristics.

Caution 8. Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in 37.3.2 Supply current characteristics will be added.

Caution 9. When the setting of the ADISS bit is 1, the hardware trigger wait mode and one-shot conversion mode cannot be used at the same time.

Correct:

(omitted)

Caution 7. When the setting of the ADISS bit is 1, the internal reference voltage cannot be used for the + side reference voltage. After the ADISS bit is set to 1, the initial conversion result cannot be used. For the setting flow, see 12.7.5 Example of using the ADC when selecting the temperature sensor output voltage or internal reference voltage, and software trigger no-wait mode and one-shot conversion mode. For details about the internal reference voltage, see Section 37 Electrical Characteristics.

Caution 8. Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in 37.3.2 Supply current characteristics will be added.

Caution 9. When the setting of the ADISS bit is 1, the hardware trigger wait mode and one-shot conversion mode cannot be used at the same time.

Caution 10. When the setting of the ADISS bit is 1, the software trigger wait mode and one-shot conversion mode cannot be used at the same time.

10. 12.6.6 Software trigger wait mode (select mode, one-shot conversion mode) (Page 586)

Incorrect:

(omitted)

Caution When <5> or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

(omitted)

Caution 1. When <5> or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Caution 2. The setting of ADISS being 1 (the input source is temperature sensor output voltage or internal reference voltage) cannot be used in the software trigger wait mode (one-shot conversion mode).

11. 15.3.8 Serial status register mn (SSRmn) (Page 666)

Incorrect:

(omitted)

Note 1. SSR00 to SSR03, SSR10, and SSR11 are present in all products.
SSR12 and SSR13 are only present in the 80- to 128-pin products.

Note 2. This bit is only present in the SSR01, SSR03, SSR11, and SSR13 registers.

Caution 1. If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVFmn = 1) is detected.

Caution 2. When the simplified SPI (CSI) is handling reception in the SNOOZE mode (SWCm = 1), the OVFmn flag will not change.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Correct:

(omitted)

Note 1. SSR00 to SSR03, SSR10, and SSR11 are present in all products.
SSR12 and SSR13 are only present in the 80- to 128-pin products.

Note 2. This bit is only present in the SSR01, SSR03, SSR11, and SSR13 registers.

Caution 1. If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVFmn = 1) is detected.

Caution 2. When the simplified SPI (CSI) is handling reception in the SNOOZE mode (SWCm = 1), the OVFmn and BFFmn flags will not change.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

12. 15.3.13 Serial output register m (SOm) (Page 671)

Incorrect:

Address: F0168H, F0169H (SO1)
After reset: 0F0FH[Note]
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
SO1	0	0	0	0	CKO13	CKO12	CKO11	CKO10

7	6	5	4	3	2	1	0
0	0	0	0	SO13	SO12	SO11	SO10

CKOmn	Serial clock output of channel n
0	Serial clock output value is 0.
1	Serial clock output value is 1.

SOmn	Serial data output of channel n
0	Serial data output value is 0.
1	Serial data output value is 1.

Note In the 30- to 64-pin products, the value of the SO1 register is 0303H following a reset.

Caution Be sure to clear bits 15 to 12 and 7 to 4 of the SO0 register to 0. Be sure to clear bits 15 to 10 and 7 to 2 of the SO1 register for 30- to 64-pin products and bits 15 to 12 and 7 to 4 of the SO1 register for 80- to 128-pin products to 0.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Correct:

Address: F0168H, F0169H (SO1)
After reset: 0F0FH[Note]
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
SO1	0	0	0	0	CKO13	CKO12	CKO11	CKO10

7	6	5	4	3	2	1	0
0	0	0	0	SO13	SO12	SO11	SO10

CKOmn	Serial clock output of channel n
0	Serial clock output value is 0.
1	Serial clock output value is 1.

SOmn	Serial data output of channel n
0	Serial data output value is 0.
1	Serial data output value is 1.

Note In the 30- to 64-pin products with the ROM of no more than 128 Kbytes, the value of the SO1 register is 0303H following a reset.

Caution Be sure to clear bits 15 to 12 and 7 to 4 of the SO0 register to 0. Be sure to clear bits 15 to 10 and 7 to 2 of the SO1 register for 30- to 64-pin products with the ROM of no more than 128 Kbytes and bits 15 to 12 and 7 to 4 of the SO1 register for 80- to 128-pin products to 0.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

13. 17.3.4 Baud Rate Generator (Page 943)

Incorrect:

After the start bit is detected, the latch timing of receive data is determined by the counter specified with the baud rate generator control register (BRGCAn). If the whole frame including the stop bit has been received before this latching, reception can proceed correctly. Assuming that 11 bits of data are received, the theoretical values can be calculated as follows.

- The relation between 1-bit data length and baud rate
  FL = (Brate) - 1
  Brate: Baud rate of UART
  k: Set value of BRGCAn register
  FL: 1-bit data length
  Margin of latch timing: 1 clock

- Minimum permissible data frame length (FLmin)

$$FLmin = 11 \times FL - \frac{k - 1}{2k} \times FL = \frac{21k + 1}{2k} FL$$

- Maximum permissible baud rate for reception on the transmitting side (BRmax)

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k + 1} Brate$$

- Maximum permissible data frame length (FLmax)

$$FLmax = \frac{21k+1}{20k} FL \times 11$$

- Minimum permissible baud rate for reception on the transmitting side (BRmin)

$$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k - 1} Brate$$

Table 17 - 5 shows the permissible baud rate error between UART and the transmitting side can be calculated from the above minimum and maximum baud rate expressions.

Table 17 - 5 Maximum/Minimum Permissible Baud Rate Error

Division ratio (k)	Maximum permissible baud rate error	Minimum permissible baud rate error
2	+2.32%	-2.43%
4	+3.52%	-3.61%
8	+4.14%	-4.19%
20	+4.51%	-4.53%
50	+4.66%	-4.67%
100	+4.71%	-4.71%
255	+4.74%	-4.74%

Remark 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the division ratio (k), the higher the permissible error.
Remark 2. k: Set value of BRGCAn register

Correct:

After the start bit is detected, the latch timing of receive data is determined by the counter specified with the baud rate generator control register (BRGCAn). If the whole frame including the stop bit has been received before this latching, reception can proceed correctly. Assuming that 11 bits of data are received, the theoretical values can be calculated as follows.

- The relation between 1-bit data length and baud rate
  FL = (Brate) - 1
  Brate: Baud rate of UART
  k: Set value of BRGCAn register
  FL: 1-bit data length
  Margin of latch timing: 2 clock

- Minimum permissible data frame length (FLmin)

k = 3 to 255: $$FLmin = 11 \times FL - \frac{k - 2}{2k} \times FL = \frac{21k + 2}{2k} FL$$

- Maximum permissible baud rate for reception on the transmitting side (BRmax)

k = 2: $$BRmax = Brate + \frac{1}{22k} Brate$$

k = 3 to 255: $$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k + 2} Brate$$

- Maximum permissible data frame length (FLmax)

k = 3 to 255: $$FLmax = \frac{21k + 2}{20k} FL \times 11$$

- Minimum permissible baud rate for reception on the transmitting side (BRmin)

k = 2: $$BRmin = Brate - \frac{1}{22k} Brate$$

k = 3 to 255: $$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k - 2} Brate$$

Table 17 - 5 shows the permissible baud rate error between UART and the transmitting side can be calculated from the above minimum and maximum baud rate expressions.

Table 17 - 5 Maximum/Minimum Permissible Baud Rate Error

Division ratio (k)	Maximum permissible baud rate error	Minimum permissible baud rate error
2	+2.27%	-2.27%
4	+2.33%	-2.44%
8	+3.53%	-3.61%
20	+4.27%	-4.31%
50	+4.56%	-4.58%
100	+4.66%	-4.67%
255	+4.72%	-4.73%

Remark 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the division ratio (k), the higher the permissible error.
Remark 2. k: Set value of BRGCAn register

14. 19.4.3 Repeat mode (Page 1024, Page 1025)

Incorrect:

(Page 1024)

(omitted)

1. Example 1 of using repeat mode: Outputting stepping motor control pulses using port pins
   The DTC is activated using the interval timer function of channel 0 of timer array unit 0, and the patterns of the motor control pulse stored in the code flash memory are transferred to the general-purpose port pins.
   · The vector address is **FFC14H** and control data is allocated at FFCD0H to FFCD7H.
   · Transfers 8-byte data at addresses from 02000H to 02007H of the code flash memory from the mirror area (F2000H to F2007H) to port register 1 (FFF01H).
   · A repeat mode interrupt is disabled.

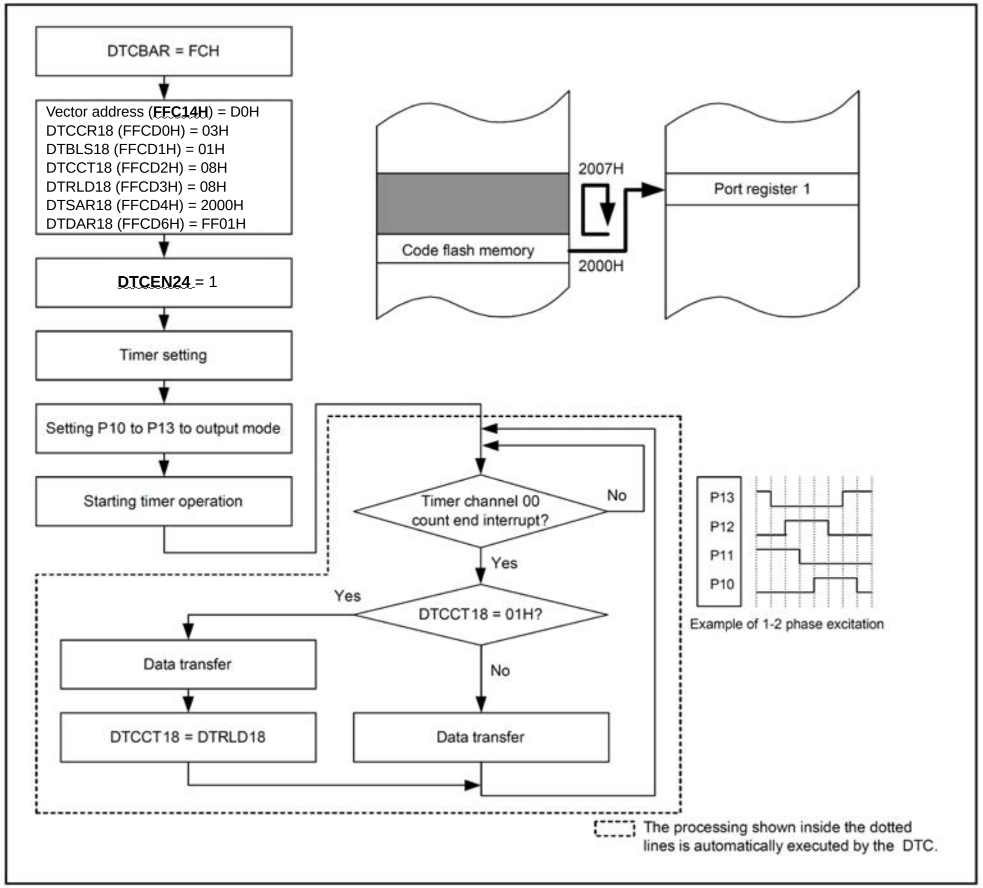
Correct:

(omitted)

1. Example 1 of using repeat mode: Outputting stepping motor control pulses using port pins
   The DTC is activated using the interval timer function of channel 0 of timer array unit 0, and the patterns of the motor control pulse stored in the code flash memory are transferred to the general-purpose port pins.
   · The vector address is FFC17H and control data is allocated at FFCD0H to FFCD7H.
   · Transfers 8-byte data at addresses from 02000H to 02007H of the code flash memory from the mirror area (F2000H to F2007H) to port register 1 (FFF01H).
   · A repeat mode interrupt is disabled.

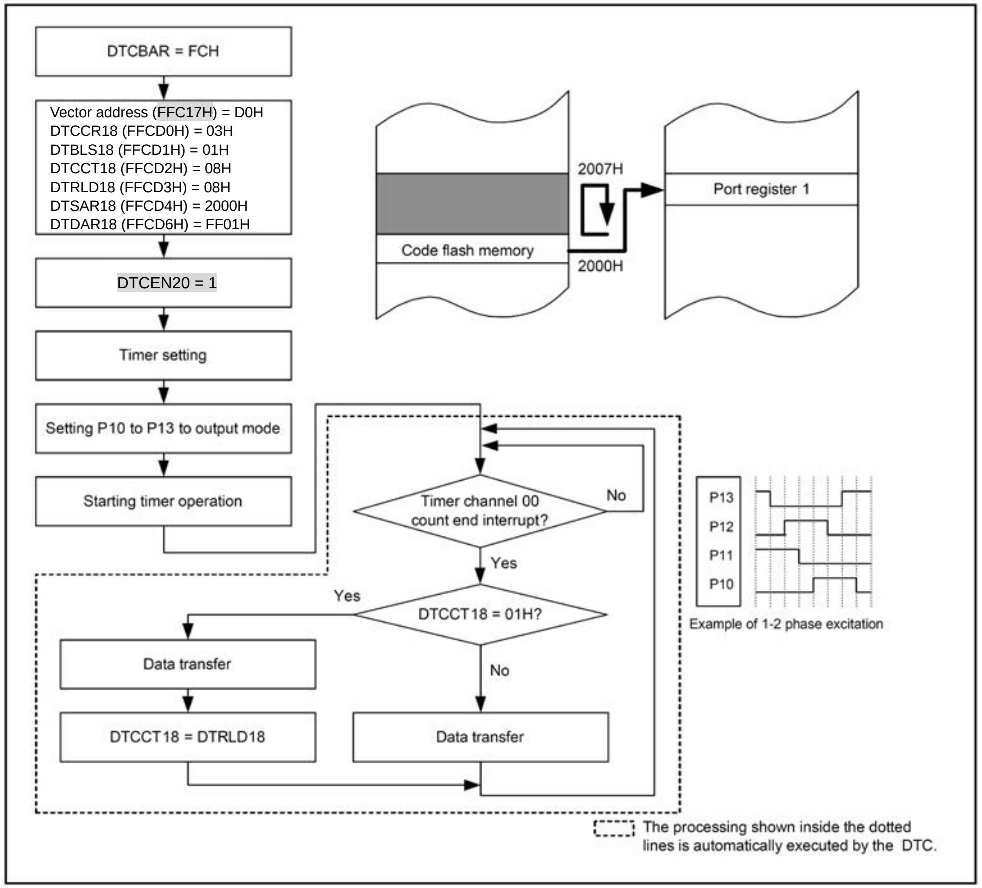
(Page 1024)

Figure 19 - 19 Example 1 of Using Repeat Mode: Outputting Stepping Motor Control Pulses Using Port Pins



To stop the output, stop the timer first and then clear **DTCEN24**.

Figure 19 - 19 Example 1 of Using Repeat Mode: Outputting Stepping Motor Control Pulses Using Port Pins



To stop the output, stop the timer first and then clear DTCEN20.

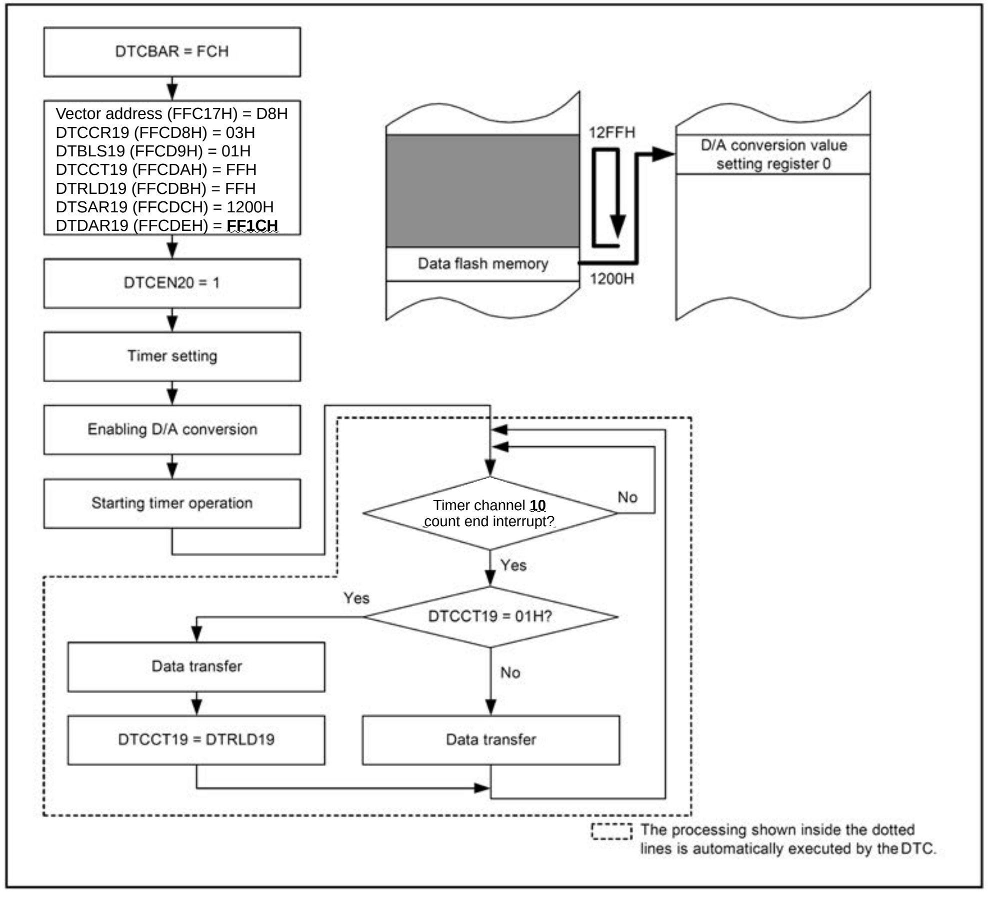
(Page 1025)

2. Example 2 of using repeat mode: Outputting a sine wave using the 8-bit D/A converter

The DTC is activated using an interrupt of the interval timer function of channel 0 of timer array unit **1**, and the table of the sine wave stored in the data flash memory is transferred to the 8-bit D/A conversion value setting register 0 (F0330H). The timer interval time is set to the D/A output setup time.

(omitted)

Figure 19 - 20 Example 2 of Using Repeat Mode: Outputting a Sine Wave Using the 8-bit D/A Converter



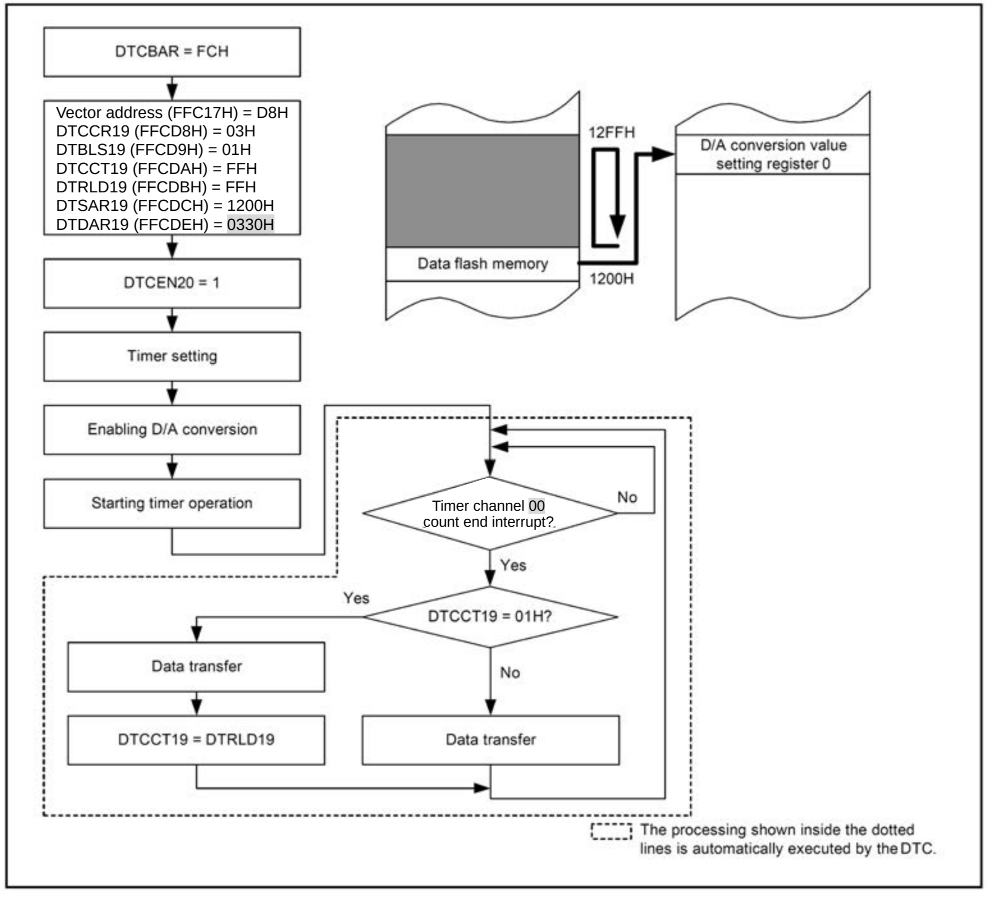
(omitted)

2. Example 2 of using repeat mode: Outputting a sine wave using the 8-bit D/A converter

The DTC is activated using an interrupt of the interval timer function of channel 0 of timer array unit 0, and the table of the sine wave stored in the data flash memory is transferred to the 8-bit D/A conversion value setting register 0 (F0330H). The timer interval time is set to the D/A output setup time.

(omitted)

Figure 19 - 20 Example 2 of Using Repeat Mode: Outputting a Sine Wave Using the 8-bit D/A Converter



(omitted)

15. 37.2.3 Characteristics of the On-chip Oscillators (Page 1401)

Incorrect:

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f_{IH}		1		32	MHz
Middle-speed on-chip oscillator clock frequency Note 3	f_{IM}		1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy Note 1			-12		+12	%
Middle-speed on-chip oscillator clock correction resolution				0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient					±0.17 Note 4	%/°C
Low-speed on-chip oscillator clock frequency Note 3	f_{IL}			32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy Note 1			-15		+15	%
Low-speed on-chip oscillator clock correction resolution				0.3		%
Low-speed on-chip oscillator frequency temperature coefficient					±0.21 Note 4	%/°C

Note 1. The accuracy values were obtained in testing of this product.

Note 2. The listed condition applies when the setting of the FRQSEL3 bit is 1.

Note 3. The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.

Note 4. **Guaranteed by characterization results.**

Correct:

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f_{IH}		1		32	MHz
Middle-speed on-chip oscillator clock frequency Note 3	f_{IM}		1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy Note 1			-12		+12	%
Middle-speed on-chip oscillator clock correction resolution				0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient					±0.17 Note 4	%/°C
Low-speed on-chip oscillator clock frequency Note 3	f_{IL}			32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy Note 1			-15		+15	%
Low-speed on-chip oscillator clock correction resolution				0.3		%
Low-speed on-chip oscillator frequency temperature coefficient					±0.21 Note 4	%/°C

Note 1. The accuracy values were obtained in testing of this product.

Note 2. The listed condition applies when the setting of the FRQSEL3 bit is 1.

Note 3. The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.

Note 4. These values are the results of characteristic evaluation and are not checked for shipment.

16. 37.3.1 Pin characteristics (Page 1406)

Incorrect:

(omitted)

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8 EV_{DD0}		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV_{DD0} ≤ 5.5 V	2.2		EV_{DD0}	V
			TTL input buffer 3.3 V ≤ EV_{DD0} < 4.0 V	2.0		EV_{DD0}	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	1.5		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P156		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 EV_{DD0}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2 EV_{DD0}	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD0} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P156		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 EV_{DD0}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0		0.2 V_{DD}	V

(omitted)

Correct:

(omitted)

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8 EV_{DD0}		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P17, P41, P43, P44, P53 to P55, P71, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV_{DD0} ≤ 5.5 V	2.2		EV_{DD0}	V
			TTL input buffer 3.3 V ≤ EV_{DD0} < 4.0 V	2.0		EV_{DD0}	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	1.5		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P156		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 EV_{DD0}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2 EV_{DD0}	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P17, P41, P43, P44, P53 to P55, P71, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD0} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P156		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 EV_{DD0}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0		0.2 V_{DD}	V

(omitted)

17. 37.3.2 Supply current characteristics (Page 1411, Page 1414, Page 1418, Page 1421, Page 1425, Page 1428)

Incorrect:
(Page 1411)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.3	—	mA
						V_{DD} = 1.8 V		1.3	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

Correct:

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.3	—	mA
						V_{DD} = 1.8 V		1.3	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1414)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.54	1.93	mA
					V_{DD} = 1.8 V		0.53	1.92	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.54	1.93	mA
					V_{DD} = 1.8 V		0.53	1.92	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1418)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.4	—	mA
						V_{DD} = 1.8 V		1.4	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.4	—	mA
						V_{DD} = 1.8 V		1.4	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1421)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.57	1.97	mA
					V_{DD} = 1.8 V		0.56	1.96	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.57	1.97	mA
					V_{DD} = 1.8 V		0.56	1.96	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1425)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.6	—	mA
						V_{DD} = 1.8 V		1.5	—	
					Normal operation	V_{DD} = 5.0 V		3.5	5.6	mA
						V_{DD} = 1.8 V		3.5	5.6	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.0	1.6	mA
						V_{DD} = 1.8 V		1.0	1.6	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.6	—	mA
						V_{DD} = 1.8 V		1.5	—	
					Normal operation	V_{DD} = 5.0 V		3.5	5.6	mA
						V_{DD} = 1.8 V		3.5	5.6	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.0	1.6	mA
						V_{DD} = 1.8 V		1.0	1.6	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the "Typ." column do not include the operating currents of the peripheral modules.

· The currents in the "Max." column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1428)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.60	2.00	mA
					V_{DD} = 1.8 V		0.59	1.99	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.22	0.59	mA
					V_{DD} = 1.8 V		0.21	0.58	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the “Typ.” column do not include the operating currents of the peripheral modules.

· The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.60	2.00	mA
					V_{DD} = 1.8 V		0.59	1.99	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.22	0.59	mA
					V_{DD} = 1.8 V		0.21	0.58	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

· The currents in the “Typ.” column do not include the operating currents of the peripheral modules.

· The currents in the “Max.” column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

18. 37.6.1 A/D converter characteristics (Page 1475, Page 1476)

Incorrect:
(Page 1475)

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		32	MHz
Overall error Notes 1, 2, 3, 4	AINL	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±7.5	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
Conversion time Note 5	t_{CONV}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			μs
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			μs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			μs
Zero-scale error Notes 1, 2, 3, 4, 6	E_{ZS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Full-scale error Notes 1, 2, 3, 4, 6	E_{FS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Integral linearity error Notes 1, 3, 4	ILE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
Differential linearity error Note 1	DLE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Correct:

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		32	MHz
Overall error Notes 1, 2, 3, 4	AINL	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±7.5	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
Conversion time Note 5	t_{CONV}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			μs
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			μs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			μs
Zero-scale error Notes 1, 2, 3, 4, 6	E_{ZS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Full-scale error Notes 1, 2, 3, 4, 6	E_{FS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Integral linearity error Notes 1, 3, 4	ILE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
Differential linearity error Note 1	DLE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. When pins ANI16 to ANI26 are selected as the target pins for conversion or the TSCAP voltage of the CTSU is to be A/D converted, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

(Page 1476)

2. Low-voltage modes 1 and 2

(TA = -40 to +105°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V,
reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1),
target pins ANI2 to ANI14, internal reference voltage[Note 1], and temperature sensor output voltage[Note 1])

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	fAD			1		24	MHz
Overall error[Notes 2, 3, 4, 5]	AINL	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±9	LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±9	LSB
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±11.5	LSB
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±12.0	LSB
Conversion time[Note 6]	tCONV	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V	3.33			μs
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V	5.0			μs
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V	10.0			μs
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V	20.0			μs
Zero-scale error[Notes 2, 3, 4, 5, 7]	EZS	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Full-scale error[Notes 2, 3, 4, 5, 7]	EFS	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Analog input voltage	VAIN			0		AVREFP	V

Note 1. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VDD must be at least 1.8 V.

Note 2. This value does not include the quantization error (±1/2 LSB).

Note 3. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

2. Low-voltage modes 1 and 2

(TA = -40 to +105°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V,
reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1),
target pins ANI2 to ANI14, internal reference voltage[Note 1], and temperature sensor output voltage[Note 1])

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	fAD			1		24	MHz
Overall error[Notes 2, 3, 4, 5]	AINL	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±9	LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±9	LSB
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±11.5	LSB
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±12.0	LSB
Conversion time[Note 6]	tCONV	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V	3.33			μs
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V	5.0			μs
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V	10.0			μs
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V	20.0			μs
Zero-scale error[Notes 2, 3, 4, 5, 7]	EZS	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Full-scale error[Notes 2, 3, 4, 5, 7]	EFS	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Analog input voltage	VAIN			0		AVREFP	V

Note 1. If the internal reference voltage, temperature sensor output voltage, or voltage on the TSCAP pin of the CTSU is to be A/D converted, VDD must be at least 1.8 V.

Note 2. This value does not include the quantization error (±1/2 LSB).

Note 3. When pins ANI16 to ANI26 are selected as the target pins for conversion or the TSCAP voltage of the CTSU is to be A/D converted, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

19. 23.3 Standby Function Operation (Page 1128, Page 1130, Page 1140, Page 1141)

Incorrect:
(Page 1128)

Table 23 - 1 Operating States in HALT Mode (1) (2/2)

HALT Mode Setting / Item		When a HALT Instruction is Executed While the CPU is Operating with the Main System Clock			
		When the CPU is Operating with the High-speed On-chip Oscillator Clock (f_{IH})	When the CPU is Operating with the Middle-speed On-chip Oscillator Clock (f_{IM})	When the CPU is Operating with the X1 Clock (f_X)	When the CPU is Operating with the External Main System Clock (f_{EX})
Clock output/buzzer output		Operation enabled			
A/D converter					
Power-on-reset function		Operation enabled			
Voltage detection function					
External interrupt					
Key interrupt function					
Capacitive sensing unit (CTSU2L)					
CRC operation function	High-speed CRC				
	General-purpose CRC	Capable of operation in response to access by the DTC or SMS to obtain data for calculations from the RAM area			
Illicit memory access detection function		Capable of operation in response to access by the DTC or SMS			
RAM parity error detection function					
RAM guard function					
SFR guard function					
True random number generator		Operation enabled			

(Omitted)

Correct:

Table 23 - 1 Operating States in HALT Mode When the Main System Clock Is Used as the CPU Clock (2/2)

HALT Mode Setting / Item		When a HALT Instruction is Executed While the CPU is Operating with the Main System Clock			
		When the CPU is Operating with the High-speed On-chip Oscillator Clock (f_{IH})	When the CPU is Operating with the Middle-speed On-chip Oscillator Clock (f_{IM})	When the CPU is Operating with the X1 Clock (f_X)	When the CPU is Operating with the External Main System Clock (f_{EX})
Clock output/buzzer output		Operation enabled			
A/D converter					
Power-on-reset function		Operation enabled			
Voltage detection function					
External interrupt					
Key interrupt function					
Capacitive sensing unit (CTSU2L) Note					
CRC operation function	High-speed CRC				
	General-purpose CRC	Capable of operation in response to access by the DTC or SMS to obtain data for calculations from the RAM area			
Illicit memory access detection function		Capable of operation in response to access by the DTC or SMS			
RAM parity error detection function					
RAM guard function					
SFR guard function					
True random number generator		Operation enabled			

Note The accuracy of measurement by the capacitive sensing unit (CTSU2L) depends on the accuracy of the operating clock. When the CTSU2L is to be used, we recommend selecting the high-speed on-chip oscillator clock (f_{IH}) or high-speed system clock (f_{MX}) as the CPU/peripheral hardware clock (f_{CLK}).

(Omitted)

(Page 1130)

Table 23 - 2 Operating States in HALT Mode (2) (2/2)

HALT Mode Setting / Item		When a HALT Instruction is Executed While the CPU is Operating with the Subsystem Clock		
		When the CPU is Operating with the XT1 Clock (fXT)	When the CPU is Operating with the External Subsystem Clock (fEXS)	When the CPU is Operating with the Low-speed On-chip Oscillator Clock (fIL)
SNOOZE mode sequencer		Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operation enabled
Logic and event link controller (ELCL)		Operation-enabled function blocks can be linked		
Power-on-reset function		Operation enabled		
Voltage detection function				
External interrupt				
Key interrupt function				
Capacitive sensing unit (CTSU2L)		Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operation enabled
CRC operation function	High-speed CRC	Operation disabled		
	General-purpose CRC	Capable of operation in response to access by the DTC or SMS to obtain data for calculations from the RAM area		
Illicit memory access detection function		Capable of operation in response to access by the DTC or SMS		
RAM parity error detection function				
RAM guard function				
SFR guard function				
True random number generator		Operation enabled		

(Omitted)

Table 23 - 2 Operating States in HALT Mode When the Subsystem Clock Is Used as the CPU Clock (2/2)

HALT Mode Setting / Item		When a HALT Instruction is Executed While the CPU is Operating with the Subsystem Clock		
		When the CPU is Operating with the XT1 Clock (fXT)	When the CPU is Operating with the External Subsystem Clock (fEXS)	When the CPU is Operating with the Low-speed On-chip Oscillator Clock (fIL)
SNOOZE mode sequencer		Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operation enabled
Logic and event link controller (ELCL)		Operation-enabled function blocks can be linked		
Power-on-reset function		Operation enabled		
Voltage detection function				
External interrupt				
Key interrupt function				
Capacitive sensing unit (CTSU2L)		Operation disabled		
CRC operation function	High-speed CRC	Operation disabled		
	General-purpose CRC	Capable of operation in response to access by the DTC or SMS to obtain data for calculations from the RAM area		
Illicit memory access detection function		Capable of operation in response to access by the DTC or SMS		
RAM parity error detection function				
RAM guard function				
SFR guard function				
True random number generator		Operation enabled		

(Omitted)

(Page 1140)

Table 23 - 4 Operating States in SNOOZE Mode (1/2)

Item / STOP Mode Setting			Generation of the Source Conditions Which Lead to Transitions to SNOOZE Mode during STOP Mode	
			When the CPU is Operating with the High-speed On-chip Oscillator Clock (f_{IH})	When the CPU is Operating with the Middle-speed On-chip Oscillator Clock (f_{IM})
System clock			Clock supply to the CPU is stopped	
	Main system clock	f_{IH}	Operation started	Stopped
		f_{IM}	Stopped	Operation started
		f_X	Stopped	
		f_{EX}		
	Subsystem clock	f_{XT}	Operation enabled	
		f_{EXS}		
		f_{IL}	Set by bits 0 (WDSTBYON) and 4 (WDTON) of the option byte (000C0H), and the WUTMMCK0 bit of the subsystem clock supply mode control register (OSMC) WUTMMCK0 = 1 or SELLOSC = 1: Oscillates (Setting of WUTMMCK0 = 1 and SELLOSC = 1 is prohibited when the subsystem clocks X (f_{SX}) and XR (f_{SXR}) are operating.) WUTMMCK0 = 0, SELLOSC = 0, and WDTON = 0: Stopped WUTMMCK0 = 0, SELLOSC = 0, WDTON = 1, and WDSTBYON = 1: Oscillates WUTMMCK0 = 0, SELLOSC = 0, WDTON = 1, and WDSTBYON = 0: Stopped	
Key interrupt function				
Capacitive sensing unit (CTSU2L)			Operation enabled	
CRC operation function	High-speed CRC		Operation stopped	
	General-purpose CRC		Capable of operation in response to access by the DTC or SMS to obtain data for calculations from the RAM area	

(Page 1141)

Table 23 - 4 Operating States in SNOOZE Mode (2/2)

Item / STOP Mode Setting	Generation of the Source Conditions Which Lead to Transitions to SNOOZE Mode during STOP Mode	
	When the CPU is Operating with the High-speed On-chip Oscillator Clock (f_{IH})	When the CPU is Operating with the Middle-speed On-chip Oscillator Clock (f_{IM})
Illicit memory access detection function	Capable of operation in response to access by the DTC or SMS	
RAM parity error detection function		
RAM guard function		
SFR guard function		
True random number generator		

(Omitted)

Table 23 - 4 Operating States in SNOOZE Mode (1/2)

Item / STOP Mode Setting			Generation of the Source Conditions Which Lead to Transitions to SNOOZE Mode during STOP Mode	
			When the CPU is Operating with the High-speed On-chip Oscillator Clock (f_{IH})	When the CPU is Operating with the Middle-speed On-chip Oscillator Clock (f_{IM})
System clock			Clock supply to the CPU is stopped	
	Main system clock	f_{IH}	Operation started	Stopped
		f_{IM}	Stopped	Operation started
		f_X	Stopped	
		f_{EX}		
	Subsystem clock	f_{XT}	Operation enabled	
		f_{EXS}		
		f_{IL}	Set by bits 0 (WDSTBYON) and 4 (WDTON) of the option byte (000C0H), and the WUTMMCK0 bit of the subsystem clock supply mode control register (OSMC) WUTMMCK0 = 1 or SELLOSC = 1: Oscillates (Setting of WUTMMCK0 = 1 and SELLOSC = 1 is prohibited when the subsystem clocks X (f_{SX}) and XR (f_{SXR}) are operating.) WUTMMCK0 = 0, SELLOSC = 0, and WDTON = 0: Stopped WUTMMCK0 = 0, SELLOSC = 0, WDTON = 1, and WDSTBYON = 1: Oscillates WUTMMCK0 = 0, SELLOSC = 0, WDTON = 1, and WDSTBYON = 0: Stopped	
Key interrupt function				
Capacitive sensing unit (CTSU2L)[Note]			Operation enabled	
CRC operation function	High-speed CRC		Operation stopped	
	General-purpose CRC		Capable of operation in response to access by the DTC or SMS to obtain data for calculations from the RAM area	

Table 23 - 4 Operating States in SNOOZE Mode (2/2)

Item / STOP Mode Setting	Generation of the Source Conditions Which Lead to Transitions to SNOOZE Mode during STOP Mode	
	When the CPU is Operating with the High-speed On-chip Oscillator Clock (f_{IH})	When the CPU is Operating with the Middle-speed On-chip Oscillator Clock (f_{IM})
Illicit memory access detection function	Capable of operation in response to access by the DTC or SMS	
RAM parity error detection function		
RAM guard function		
SFR guard function		
True random number generator		

Note The accuracy of measurement by the capacitive sensing unit (CTSU2L) depends on the accuracy of the operating clock. When the CTSU2L is to be used, we recommend selecting the high-speed on-chip oscillator clock (f_{IH}) or high-speed system clock (f_{MX}) as the CPU/peripheral hardware clock (f_{CLK}).

(Omitted)

20. Table 30-1 CTSU Functions (Page 1254)

Incorrect:

Table 30 - 1 CTSU Functions

Item		Configuration
CTSU operating voltage condition		V_{DD} = 1.8 to 5.5 V
Operating clock		f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, or $f_{CLK}/8$
Pins	Electrostatic capacitance measurement	TSm (m = 00 to 15, 20 to 35) up to 32 channels
	Connection pin to capacitor for measurement secondary power	TSCAP (10 nF) We recommend connecting a 10-nF capacitor.
Measurement mode	Self-capacitance measurement mode	Electrostatic capacitance is measured from the charged current that flows toward the electrode used in the self-capacitance method.
	Mutual capacitance measurement mode	Electrostatic capacitance is measured from the charged current that flows toward the capacitance generated between the transmit and receive electrodes used in the mutual capacitance method.
	Current measurement mode	Current from a measurement pin is measured.
Calibration mode		Characteristic correction of the current control oscillator for measurement
Noise prevention		**Synchronous noise prevention, high-pass noise prevention** Majority decision by multi-frequency measurement
Adjustment for each pin		Offset current adjustment function Sensor drive pulse frequency specification Measurement time specification
Measurement start conditions		Software trigger External trigger (**ELCL**)
Low-power function		SNOOZE mode supported
Interrupt requests	DTC activation source/ **DTC interrupt source**	Request to write to a configuration register of an individual CTSU channel Request to transfer data measured by the CTSU
	Interrupt source	**Measurement end interrupt**
Transmission power switching of mutual capacitance method		**The power for transmission in the mutual capacitance method is switchable.**

Correct:

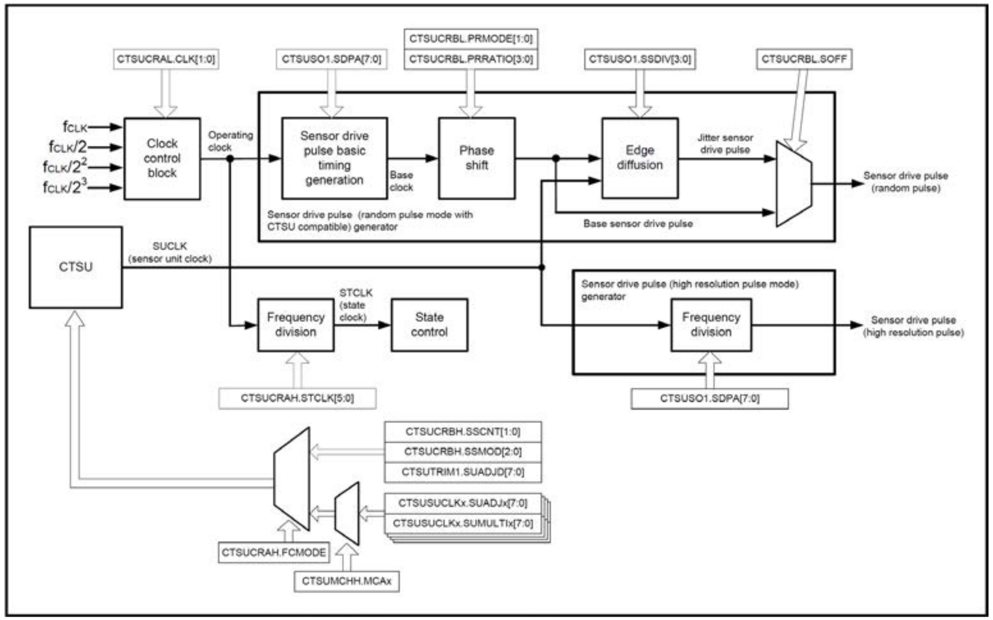
Table 30 - 1 CTSU Functions

Item		Configuration
Module type name		CTSU2L
Operating voltage		V_{DD} = 1.8 to 5.5 V
Operating clock Note		f_{CLK} (at least 1 MHz), $f_{CLK}/2$, $f_{CLK}/4$, or $f_{CLK}/8$
Pins	Electrostatic capacitance measurement	TSm (m = 00 to 15, 20 to 35) up to 32 channels
	Connection pin to capacitor for measurement secondary power	TSCAP (10 nF) We recommend connecting a 10-nF capacitor.
Measurement mode	Self-capacitance measurement mode	Electrostatic capacitance is measured from the charged current that flows toward the electrode used in the self-capacitance method.
	Mutual capacitance measurement mode	Electrostatic capacitance is measured from the charged current that flows toward the capacitance generated between the transmit and receive electrodes used in the mutual capacitance method.
	Current measurement mode	Current on a measurement pin is measured.
Calibration mode		Characteristic correction of the current control oscillator for measurement
Noise prevention		• Spread spectrum for sensor drive pulses • Random phase-shifting for sensor drive pulses • Majority decision from multi-frequency measurement
Adjustment for each pin		• Offset current adjustment • Sensor drive pulse frequency specification • Measurement time specification
Measurement start conditions		• Software trigger • External trigger (event input from the ELCL)
Low-power function		SNOOZE mode supported
Request outputs	DTC activation sources	• Request to write to a configuration register of an individual CTSU channel • Request to transfer data measured by the CTSU
	Interrupt source	• Write request interrupt for a configuration register of an individual CTSU channel (INTCTSUWR) • Request to transfer data measured by the CTSU (INTCTSURD) • CTSU measurement end (INTCTSUFN)
Transmission power switching of the mutual capacitance method		The source of power to the pins can be switched at the time of transmission.

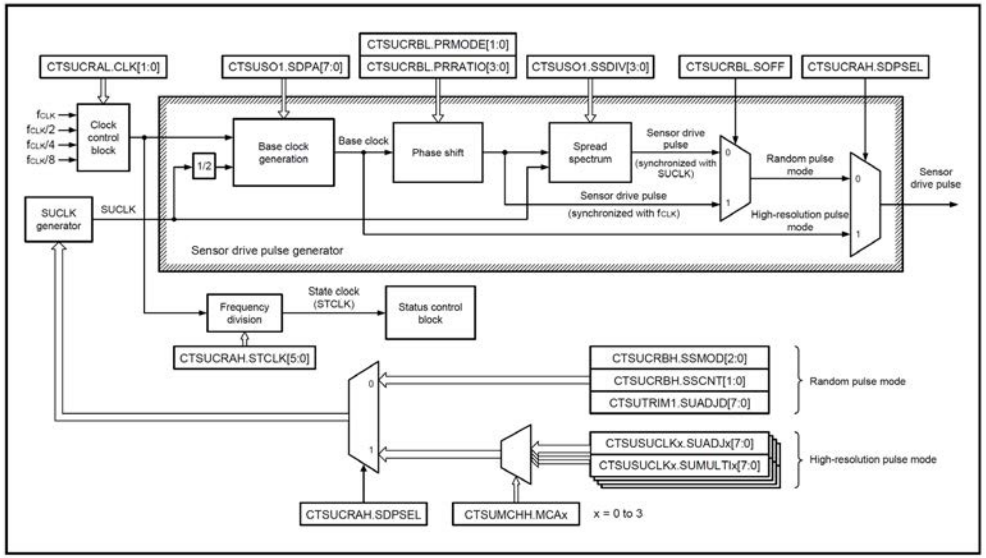
Note The accuracy of measurement by the capacitive sensing unit (CTSU2L) depends on the accuracy of the operating clock. When the CTSU2L is to be used, we recommend selecting the high-speed on-chip oscillator clock (f_{IH}) or high-speed system clock (f_{MX}) as the CPU/peripheral hardware clock (f_{CLK}). Do not select the subsystem clock (f_{SUB}) as the CPU/peripheral hardware clock (f_{CLK}).

21. Figure 30-4 Sensor Drive Pulse Output Clock Configuration (Page 1255)

Incorrect:



Correct:
Complete revision



22. 30.1.2 Measurement Status (new)

Incorrect:

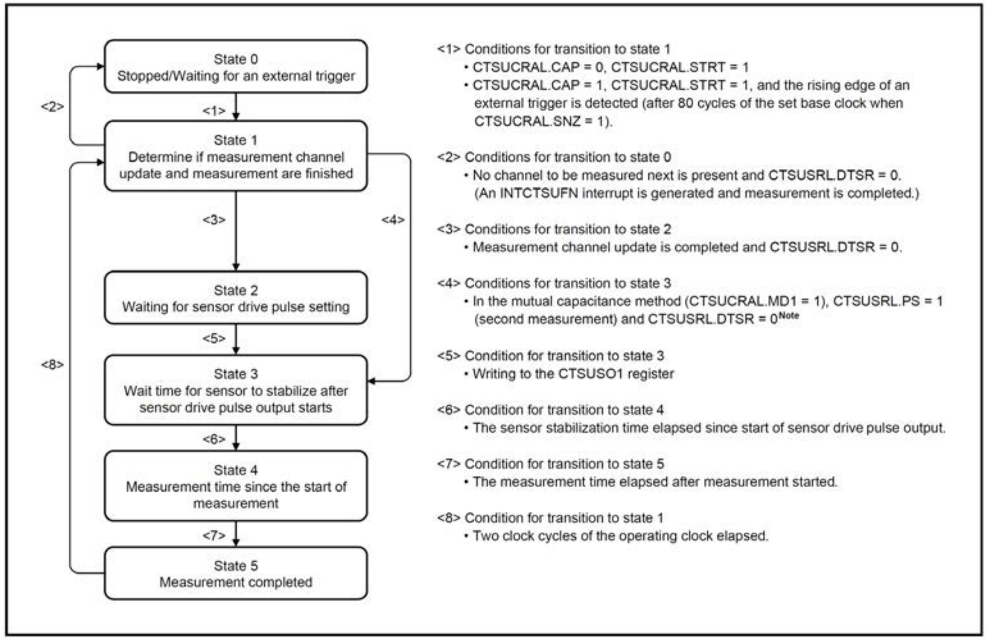
Not applicable

Correct:

30.1.2 Measurement states

The CTSU has a state controller. The measurement states are common to both modes of measurement. The measurement status counter indicates the current state of measurement, and its value can be read from the CTSUSRL.STC[2:0] bits. **Figure 30 - 5** shows the transitions between the measurement states.

Figure 30 - 5 Transitions between the Measurement States



Note When CTSUSRL.DTSR = 1, waiting until the reading of the previous measurement result is required.

The status counter makes the transition to state 0 when measurement has been completed on all of the specified measurement channels. The CTSUCRAL.STRT bit is set to 0 by hardware when the software trigger is to be used. When an external trigger is to be used, the STRT bit retains the value 1, and the CTSU waits for the next trigger. When operation is forcibly stopped (by writing 0 to the STRT bit and 1 to the CTSUCRAL.INIT bit at the same time) during measurement or is in the state of waiting for a trigger, the state makes the transition to state 0 and measurement is stopped. If no channels for measurement are set in the CTSUMCHL, CTSUMCHH, CTSUCHACAL, CTSUCHACAH, CTSUCHACBL, CTSUCHTRCAL, CTSUCHTRCAH, and CTSUCHTRCBL registers, a measurement end interrupt (INTCTSUFN) is generated immediately after the transition to state 1, and the state then makes the transition to state 0.

The following are the cases when there are no channels for measurement.

- No target measurement channels are specified in the CTSUCHACAL, CTSUCHACAH, and CTSUCHACBL registers.
- In single scan mode, no channels specified in the CTSUMCHL and CTSUMCHH registers are set as targets for measurement in the CTSUCHACAL, CTSUCHACAH, and CTSUCHACBL registers.
- In the self-capacitance method, there is no reception channel for measurement in the following combinations of registers: CTSUCHACAL/CTSUCHACAH/CTSUCHACBL and CTSUCHTRCAL/CTSUCHTRCAH/CTSUCHTRCBL.
- In the mutual capacitance method, there is no transmission channel or reception channel for measurement in the following combinations of registers: CTSUCHACAL/CTSUCHACAH/CTSUCHACBL and CTSUCHTRCAL/CTSUCHTRCAH/CTSUCHTRCBL.

23. 30.2.3 CTSU Control Registers AL and AH (CTSUCRAL, CTSUCRAH) (Page 1262 to Page 1265)

Incorrect:
(p.1262)

ATUNE2	Analog Adjustment 2
0	In accord with the setting of the ATUNE1 bit
1	When ATUNE1 is 0: 20 µA (1/1) When ATUNE1 is 1: 160 µA (1/8) current measurement mode
The ATUNE2 bit sets the current mirror ratio of the measurement power-supply current to the current control oscillator input current.	

MD1	Measurement Mode Select 1
0	Self-capacitance method (single measurement) When CHTRCx is set to 1 (transmission), the same phase pulse is output from the TSm pin for measurement. When multiple CHTRCx bits are set to 1, measurement is scanned.
1	Mutual capacitance method (double-measurement) Set the CHTRCx bit to 1 (transmission) to handle measurement. The same phase pulse is output from the TSm pin in the first measurement. The reverse phase pulse is output from the TSm pin in the second measurement.
Set the MD1 bit to 0 to select self-capacitance method. Set the MD1 bit to 1 to select mutual-capacitance method.	

Correct:

ATUNE2	Current Range Switching 2
0	When the ATUNE1 bit is 0: 80 µA When the ATUNE1 bit is 1: 40 µA
1	When the ATUNE1 bit is 0: 20 µA When the ATUNE1 bit is 1: 160 µA
Setting this bit in combination with the ATUNE1 bit specifies the maximum supply current (measurement range) by changing the amount of the resistive load on the measurement power supply.	

CTSUCRAH.ATUNE2	CTSUCRAL.ATUNE1	Measurement range
0	0	80 µA
0	1	40 µA
1	0	20 µA
1	1	160 µA

MD1	Measurement Mode Select 1
0	Self-capacitance method Set the pin to be used for reception in measurement (CTSUCHTRCAL.CHTRCm = 0, CTSUCHTRCAH.CHTRCm = 0). Set the pin to be used as an active shield for transmission (by setting CHTRCm to 1). If a pin set for transmission is present, the transmission pin outputs a pulse in the same phase as that for the channel being measured. When all TSm pins are set for reception, the measurement of reception pins only proceeds.
1	Mutual capacitance method The measurement proceeds with the TSm pin set for transmission (CHTRCm = 1) and the TSm pin set for reception (CHTRCm = 0). When all CHTRCm bits are set to 0, no measurement proceeds.
The MD1 bit selects the self-capacitance method or the mutual capacity method.	

(p.1262)

(Omitted)

ATUNE1	Analog Adjustment 1
0	80 µA (1/4)
1	40 µA (1/2)
The ATUNE1 bit sets the current mirror ratio of the measurement power-supply current to the current control oscillator input current.	

ATUNE0	Analog Adjustment 0
0	Measurement power-supply voltage = 1.5 V This setting cannot be used if VDD is less than 2.4 V.
1	Measurement power-supply voltage = 1.2 V
This bit is used to change voltage to suit the system's power supply specifications.	

(Omitted)

ATUNE1	Current Range Switching 1
0	When the ATUNE2 bit is 0: 80 µA When the ATUNE2 bit is 1: 40 µA
1	When the ATUNE2 bit is 0: 20 µA When the ATUNE2 bit is 1: 160 µA
Setting this bit in combination with the ATUNE2 bit specifies the maximum supply current (measurement range) by changing the amount of the resistive load on the measurement power supply. For details, see the description for the ATUNE2 bit.	

ATUNE0	Power Supply Voltage Setting
0	Measurement power supply voltage = 1.5 V
1	Measurement power supply voltage = 1.2 V Note 1
This bit is used to control the power supply voltage of the CTSU. Set this bit to 1 when VDD < 2.4 V. This bit can be set to either 0 or 1 when 2.4 V ≤ VDD.	

(p.1263)

(Omitted)

PON	Measurement Power On
0	Power off
1	Power on
The PON bit turns on the VDC for measurement to supply the power (internal voltage) for measurement. 1.2- or 1.5-V power is supplied depending on the setting of the ATUNE0 bit. Do not set this bit to 1 when the setting of CSW is 0.	

TXVSEL	TXVSEL2	Transmission Power Supply Select
0	0	Not recommended
0	1	This setting is recommended when transmission power of mutual capacitance method transmission is used.Note
1	0	Use tis setting when the active shield function is in use.
1	1	This setting is recommended when transmission power of mutual capacitance method transmission is used.Note

Note The same transmission power supply is selected when the setting of TXVSEL2 is 1.

(Omitted)

INIT	Control Block Initialization
0	—
1	Initializes the internal control registers.
To forcibly terminate operation, be sure to set the STRT bit to 0 and the INIT bit to 1 simultaneously. In this case, operation stops and the internal control registers are initialized. Do not set the STRT bit to 1 (CTSU operation start) and the INIT bit to 1 simultaneously. The TXVSEL2 bit is read as 0.	

(Omitted)

PON	Measurement Power On
0	Power off
1	Power on
The PON bit controls the supply of the power (1.5 V) for measurement. Before setting this bit to 1, set the PUMPON bit as required and set the CSW bit to 1. Do not set this bit to 1 while the CSW bit is set to 0.	

TXVSEL	TXVSEL2	Power for the Transmission Pin Select
0	0	Not recommended
1	0	Power for the internal logic circuits Use this setting when the active shield is to be used.
0	1	Dedicated power for the CTSU Use this setting when the mutual capacitance method is to be used.
1	1	

(Omitted)

INIT	Initialization of the Control Block
0	—
1	Initializes the internal control registers.
Setting this bit to 1 initializes the following registers. • CTSUSC, CTSUUC • CTSUMCHL, CTSUMCHH • All bits in CTSUSRL except bits ICOMP0 and ICOMP1 To forcibly stop operation, be sure to set the STRT bit to 0 and the INIT bit to 1 at the same time. Doing so stops the measurement and initializes the internal control registers. Do not set the STRT bit to 1 (starting measurement by the CTSU) and the INIT bit to 1 at the same time. This bit is read as 0.	

(p.1264)

SNZ	SNOOZE Enable
0	Disables the SNOOZE mode.
1	Enables the SNOOZE mode.

The SNZ bit enables or disables SNOOZE operation when an external trigger is selected (CAP = 1). Setting this bit to 1 drives the CTSU into the suspended state to enable low-power operation in the standby state.

<CTSU hardware state control>

PON	SNZ	CAP	STRT	Trigger	State of the CTSU
0	0	0	0	—	Stopped
1	0	0	0	—	State until measurement starts (VDC = ON)
1	0	0	1	—	Measurement in the normal mode (VDC = ON)
1	1	1	0	—	Prepared for measurement start by an external trigger (VDC = OFF)
1	1	1	1	Not present	Suspended (waiting for a trigger) (VDC = OFF)
1	1	1	1	Present	Measurement in the SNOOZE mode (VDC = ON)Note
1	1	0	0	—	Software suspended (VDC = OFF)
Other than above					Setting prohibited

Note When a trigger is generated in the STOP mode, measurement is handled in the SNOOZE mode.

The SNZ bit enables SNOOZE operation. In the external trigger waiting state enabled by setting the STRT bit to 1, the CPU can enter STOP mode. When a falling edge of the external trigger is detected during STOP mode, the CTSU sends a clock request to the clock generating block and enters the SNOOZE state to start measurement. After the measurement end interrupt, clear this bit to 0 by software.
The software suspended state in this table is used when the software of a system without SNOOZE mode suspends the CTSU to enable low-power operation. In this case, set the SNZ bit to 0 after the CPU returns to the previous state by an external interrupt, and then set the STRT bit to 1 to start measurement upon a software trigger.

(Omitted)

SNZ	SNOOZE Enable
0	Disables the SNOOZE mode.
1	Enables the SNOOZE mode.

Setting this bit to 1 places the CTSU in a suspended state, which reduces power consumption while on standby from measurement. The SNZ bit enables measurement in SNOOZE mode when an external trigger is selected (CAP = 1) as the condition for starting measurement.

- When an external trigger is selected as the condition for starting the measurement (CAP = 1)
  When the SNOOZE mode is to be used, set this bit to 1, then set STRT to 1 (starting measurement by the CTSU) to place the CPU in the STOP mode. If an external trigger is detected while in STOP mode, the CTSU is placed in the SNOOZE mode and starts measurement. After a measurement end interrupt, use software to clear this bit to 0.
- When a software trigger is selected as the condition for starting the measurement (CAP = 0)
  The CTSU is placed in the suspended state (low-power mode) under the conditions listed in the table below. An interrupt is used to cause the CPU to resume from the STOP mode while the CTSU is in the suspended state (low-power mode). To start measurement following resumption by the CPU, set this bit to 0 and then set the STRT bit to 1 to start measurement by the CTSU.

PON	SNZ	CAP	STRT	External trigger	State of the CTSU hardware
0	0	0	0	—	Stopped
1	0	0	0	—	State of waiting for the start of measurement
1	0	0	1	—	Measurement is proceeding in the normal mode
1	1	1	0	—	Preparing for an external trigger to start measurement
1	1	1	1	Not present (waiting)	Suspended (waiting for an external trigger)
1	1	1	1	Present (operating)	Measurement in the SNOOZE mode
1	1	0	0	—	Suspended (low-power mode)
Other than above					Setting prohibited

When using the SNOOZE mode function with the high-resolution pulse mode selected for the sensor drive pulses (SDPSEL = 1), the clock of the voltage boosting circuit cannot be selected for the sensor drive pulses (PCSEL = 0).

(Omitted)

(p.1265)

STRT	Measurement Operation Start
0	Measurement stopped
1	Measurement operating

The STRT bit specifies whether to start or stop CTSU operation.

When CAP is 0, writing 1 to the STRT bit starts measurement. At the end of measurement, this bit is cleared to 0 by hardware.

When CAP is 1, writing 1 to this bit drives the CTSU into the external trigger waiting state. Measurement starts at the falling edge of the external trigger. After the measurement is complete, the CTSU waits for the next external trigger and continues operation.

The following table shows the CTSU states.

<CTSU state>

STRT	CAP	CTSU state
0	0	Stopped
0	1	Stopped
1	0	Measurement in progress
1	1	Measurement in progress or waiting for an external trigger Note

Note The state can be read from the CTSUSRL.STC[2:0] bits. Measurement in progress: CTSUSRL.STC[2:0] ≠ 000B
While waiting for an external trigger: CTSUSRL.STC[2:0] = 000B

If 1 is written to the STRT bit by software when the STRT bit is already set to 1, this writing is ignored and operation continues.

To forcibly terminate operation by software when the STRT bit is set to 1, be sure to set the STRT bit to 0 and the INIT bit to 1 simultaneously.

STRT	Measurement Start
0	Stops measurement
1	Starts measurement (measurement in progress or waiting for an external trigger)

The STRT bit specifies whether to start or stop CTSU measurement.

- When a software trigger is selected as the condition for starting the measurement (CAP = 0)
  Writing 1 to the STRT bit starts measurement. At the end of measurement, this bit is cleared to 0 by hardware.
- When an external trigger is selected as the condition for starting the measurement (CAP = 1)
  Writing 1 to this bit drives the CTSU into the state of waiting for an external trigger. Measurement starts on detection of an external trigger. After the measurement is completed, the CTSU waits for the next external trigger. To release the CTSU from the state of waiting for an external trigger, set this bit to 0 and the INIT bit to 1 at the same time.

The following table shows the CTSU states.

STRT	CAP	CTSU state
0	0	Stopped
0	1	Stopped
1	0	Measurement in progress
1	1	Measurement in progress or waiting for an external trigger Note 2

If 1 is written to the STRT bit by software when the STRT bit is already set to 1, the writing is ignored and operation continues. To have software forcibly stop operation while the STRT bit is set to 1, be sure to set the STRT bit to 0 and the INIT bit to 1 at the same time.

Note 1. The active shield cannot be used when ATUNE0 = 1.

Note 2. The state in terms of the two alternatives can be read from the CTSUSRL.STC[2:0] bits.
−CTSUSRL.STC[2:0] ≠ 000B: Measurement in progress
−CTSUSRL.STC[2:0] = 000B: Waiting for an external trigger

Caution Set the bits of this register other than the STRT and INIT bits while STRT = 0 (measurement stopped).

Remark 1. x = 0 to 3

Remark 2. m = 00 to 15, 20 to 35

24. 30.2.4 CTSU Control Registers BL and BH (CTSUCRBL, CTSUCRBH) (Page 1266 to Page 1268)

Incorrect:
(Page 1266)

(Omitted)

SSCNT[1:0]		SUCLK **Diffusion** Control
0	0	**SSADJ + 0**
0	1	**SSADJ + 1**
1	0	**SSADJ + 2**
1	1	**SSADJ + 3**
The SSCNT[1:0] bits adjust the diffusion clock frequency. The setting of 11B is for random-pulse mode (CTSU compatible).		

(Omitted)

Correct:

(Omitted)

SSCNT[1:0]		SUCLK Spread Spectrum Control
0	0	CTSUCRAH.SDPSEL = 0: CTSUTRIMx.SUADJD[7:0] + 00H CTSUCRAH.SDPSEL = 1: CTSUSUCLKx.SUADJx[7:0] + 00H
0	1	CTSUCRAH.SDPSEL = 0: CTSUTRIMx.SUADJD[7:0] + 10H CTSUCRAH.SDPSEL = 1: CTSUSUCLKx.SUADJx[7:0] + 20H
1	0	CTSUCRAH.SDPSEL = 0: CTSUTRIMx.SUADJD[7:0] + 20H CTSUCRAH.SDPSEL = 1: CTSUSUCLKx.SUADJx[7:0] + 40H
1	1	CTSUCRAH.SDPSEL = 0: CTSUTRIMx.SUADJD[7:0] + 30H CTSUCRAH.SDPSEL = 1: CTSUSUCLKx.SUADJx[7:0] + 60H
These bits adjust the frequency of SUCLK.		

(Omitted)

(Page 1267)

SST[7:0]	Sensor Stabilization Wait Time Control

The SST[7:0] bits set the period from the start of sensor drive pulse supply until the TSCAP pin voltage becomes stable.

<When CTSUCRAH.SDPSEL = 0>

The table below shows the stabilization time in units of base sensor drive pulse cycles.

0	0	0	0	0	0	0	0	2 cycles
0	0	0	0	0	0	0	1	4 cycles
0	0	0	0	0	0	1	0	6 cycles
0	0	0	0	0	0	1	1	8 cycles
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	510 cycles
1	1	1	1	1	1	1	1	512 cycles

<When CTSUCRAH.SDPSEL = 1>

The table below shows the stabilization time in units of STCLK cycles.

0	0	0	0	0	0	0	0	1 cycle
0	0	0	0	0	0	0	1	2 cycles
0	0	0	0	0	0	1	0	3 cycles
0	0	0	0	0	0	1	1	4 cycles
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	255 cycles
1	1	1	1	1	1	1	1	256 cycles

The TSCAP pin voltage is stabilized by supplying sensor drive pulses. The SST[7:0] value is related to the number of cycles as shown below.

- When CTSUCRAH.SDPSEL = 0
  The stabilization wait time is specified by the number of cycles of the base sensor drive pulse.
  Number of cycles = 2 × (value of these bits + 1)
  Set the stabilization wait time within the following range.
  Number of cycles set by CTSUCRBL.SST[7:0] ≥ (CTSUCRBL.PRRATIO[3:0] + 1)

- When CTSUCRAH.SDPSEL = 1
  The stabilization wait time is specified by the number of STCLK cycles.
  Number of cycles = 1 × (value of these bits + 1)

SST[7:0]	Sensor Stabilization Wait Time Control

The SST[7:0] bits set the period from the start of sensor drive pulse supply until the TSCAP pin voltage becomes stable. The TSCAP pin voltage is stabilized by supplying sensor driving pulses. The following shows the correspondence between the setting of the SST[7:0] bits and the number of cycles.

- In random pulse mode (CTSUCRAH.SDPSEL = 0)
  The stabilization wait time is specified in units of the number of cycles of the sensor driving pulse.

0	0	0	0	0	0	0	0	2 cycles
0	0	0	0	0	0	0	1	4 cycles
0	0	0	0	0	0	1	0	6 cycles
0	0	0	0	0	0	1	1	8 cycles
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	510 cycles
1	1	1	1	1	1	1	1	512 cycles

  Number of cycles = 2 × (value of these bits + 1)
  Set the stabilization wait time so that the following relation is satisfied.
  Number of cycles set by CTSUCRBL.SST[7:0] ≥ (PRRATIO[3:0] + 1)

- In high-resolution pulse mode (CTSUCRAH.SDPSEL = 1)
  The stabilization wait time is specified in units of the number of the STCLK cycles.

0	0	0	0	0	0	0	0	Setting prohibited Note 1
0	0	0	0	0	0	0	1	2 cycles
0	0	0	0	0	0	1	0	3 cycles
0	0	0	0	0	0	1	1	4 cycles
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	255 cycles
1	1	1	1	1	1	1	1	256 cycles

  Number of cycles = 1 × (value of these bits + 1)

(Page 1267)

PROFF	Pseudo-Random Number Disable Control
0	Pseudo-random number control is enabled.
1	Pseudo-random number control is disabled.
The PROFF bit disables the pseudo-random number control. **A value of 1 or 0 is output per cycle to generate pseudo-random numbers (1-bit random number generation). When PROFF is 1, one cycle is added to the cycles specified by the PRMODE[1:0] bits.**	

PROFF	Pseudo-Random Number Disable Control
0	Pseudo-random number control is enabled.
1	Pseudo-random number control is disabled.
The PROFF bit disables the pseudo-random number control. A pseudo-random number is generated per cycle to output a value of 1 or 0 (1-bit random number generation).	

(Page 1268)

SOFF	Jitter Disable Control
0	Applies jitter.
1	Does not apply jitter.
The SOFF bit sets whether to apply jitter to the sensor drive pulse to prevent synchronous noise. The output of the sensor drive pulse is selected from the base sensor drive pulse or the jittered sensor drive pulse.	

PRMODE[1:0]		Pseudo-Random Number Generation Cycle
0	0	255 cycles (When PROFF = 1: 256 cycles)
0	1	63 cycles (When PROFF = 1: 64 cycles)
1	0	31 cycles (When PROFF = 1: 32 cycles)
1	1	3 cycles (When PROFF = 1: 4 cycles)

PRRATIO[3:0]	Phase Shift Frequency
The PRRATIO[3:0] bits specify the phase shift frequency of the base clock using a pseudo-random number. These bits become a factor to determine the measurement period.	

SOFF Note 2	Spread Spectrum Disable Control
0	Enables the spread spectrum.
1	Disables the spread spectrum.
The SOFF bit enables or disables the spread spectrum to prevent synchronous noise. Set this bit to 1 when sensor drive pulses (synchronized with f_{CLK}) are to be used. This bit is valid when CTSUCRAH.SDPSEL = 0 (random pulse mode).	

PRMODE[1:0] Note 2		Pseudo-random Number Generation Cycle
0	0	255 cycles
0	1	63 cycles
1	0	31 cycles
1	1	3 cycles
The PRMODE[1:0] bits set the number of cycles for updating the pseudo-random number generation. The number of basic pulses is twice the number of cycles selected by these bits. These bits are valid when CTSUCRAH.SDPSEL = 0 (random pulse mode).		

PRRATIO[3:0] Note 2	Phase Shift Frequency
The PRRATIO[3:0] bits set the phase shift cycle for pseudo-random number generation. The number of measurement pulses and measurement time are specified as follows depending on the setting of these bits. Number of measurement pulses = number of basic pulses (set by the PRMODE[1:0] bits) × (value of the PRRATIO[3:0] bits + 1) Measurement time = (number of measurement pulses) + (number of basic pulses – 2) × 0.25) × base clock cycle These bits are valid when CTSUCRAH.SDPSEL = 0 (random pulse mode).	

Note 1. Do not set the SST[7:0] bits to 00H when CTSUCRAH.SDPSEL = 1.

Note 2. The SOFF, PRMODE[1:0], and PRRATIO[3:0] bits are only valid when the CTSUCRAH.SDPSEL bit is 0 (random pulse mode).

Caution Set the CTSUCRBL and CTSUCRBH registers when the CTSUCRAL.STRT bit is 0.

Remark x = 0 to 3

25. 30.2.5 CTSU measurement channel registers L and H (CTSUMCHL, CTSUMCHH) (Page 1270)

Incorrect:

MCH1[5:0]	Measurement Channel 1

- In single scan mode (CTSUCRAL.MD0 = 0), the MCH1[5:0] bits set the transmit channel to be measured. Do not set **channels that are not to be measured using** the CTSUCHACAH, CTSUCHACAL, **CTSUCHACBH,** or CTSUCHACBL register. If such channels are set, measurement **is completed** immediately after it starts.
- In multi-scan mode (CTSUCRAL.MD0 = 1), the MCH0[5:0] bits indicate the value of the transmit channel that is being measured, and writing to these bits has no effect **(cleared at the beginning of measurement).**

0	0	0	0	0	0	TS0
0	0	0	0	0	1	TS1
0	0	0	0	1	0	TS2
0	0	0	0	1	1	TS3
:	:	:	:	:	:	:
1	1	1	1	1	0	TS62
1	1	1	1	1	1	TS63

Do not modify these bits during measurement (CTSUCRAL.STRT = 1). Otherwise, operation is not guaranteed. When measurement is stopped, these bits become 111111B.

Correct:

MCH1[5:0]	Measurement Channel 1

- In single scan mode (CTSUCRAL.MD0 = 0)
  The MCH1[5:0] bits set the transmit channel to be measured. Do not set the channels for which the measurement is disabled by the CTSUCHACAH, CTSUCHACAL, or CTSUCHACBL register. If such channels are set, measurement ends immediately after it starts.
- In multi-scan mode (CTSUCRAL.MD0 = 1)
  The MCH0[5:0] bits indicate the value of the transmit channel that is being measured, and writing to these bits has no effect.

0	0	0	0	0	0	TS00
0	0	0	0	0	1	TS01
0	0	0	0	1	0	TS02
0	0	0	0	1	1	TS03
:	:	:	:	:	:	:
0	0	0	1	1	1	TS15
0	0	1	0	0	0	Setting prohibited
:	:	:	:	:	:	
0	0	1	0	1	1	
0	0	1	1	0	0	TS20
:	:	:	:	:	:	:
1	0	0	0	1	0	TS34
1	0	0	0	1	1	TS35
1	0	0	1	0	0	Setting prohibited
:	:	:	:	:	:	
1	1	1	1	1	1	

MCH0[5:0]	Measurement Channel 0

- In single scan mode (CTSUCRAL.MD0 = 0), the MCH0[5:0] bits set the receive channel to be measured. Do not set **channels that are not to be measured using** the CTSUCHACAH, CTSUCHACAL, **CTSUCHACBH,** or CTSUCHACBL register. If such channels are set, measurement **is completed** immediately after it starts.
- In multi-scan mode (CTSUCRAL.MD0 = 1), the MCH1[5:0] bits indicate the value of the receive channel that is being measured, and writing to these bits has no effect **(cleared at the beginning of measurement).**

0	0	0	0	0	0	TS0
0	0	0	0	0	1	TS1
0	0	0	0	1	0	TS2
0	0	0	0	1	1	TS3
:	:	:	:	:	:	:
1	1	1	1	1	0	TS62
1	1	1	1	1	1	TS63

Do not modify these bits during measurement (CTSUCRAL.STRT = 1). Otherwise, operation is not guaranteed. When measurement is stopped, these bits become 111111B.

MCH0[5:0]	Measurement Channel 0

- In single scan mode (CTSUCRAL.MD0 = 0)
  The MCH0[5:0] bits set the reception channel to be measured. Do not set the channels for which the measurement is disabled by the CTSUCHACAH, CTSUCHACAL, or CTSUCHACBL register. If such channels are set, measurement ends immediately after it starts.
- In multi-scan mode (CTSUCRAL.MD0 = 1)
  The MCH1[5:0] bits indicate the value of the reception channel that is being measured, and writing to these bits has no effect.

0	0	0	0	0	0	TS00
0	0	0	0	0	1	TS01
0	0	0	0	1	0	TS02
0	0	0	0	1	1	TS03
:	:	:	:	:	:	:
0	0	0	1	1	1	TS15
0	0	1	0	0	0	Setting prohibited
:	:	:	:	:	:	
0	0	1	0	1	1	
0	0	1	1	0	0	TS20
:	:	:	:	:	:	:
1	0	0	0	1	0	TS34
1	0	0	0	1	1	TS35
1	0	0	1	0	0	Setting prohibited
:	:	:	:	:	:	
1	1	1	1	1	1	

Caution Do not modify the CH1[5:0] and MCH0[5:0] bits during measurement (CTSUCRAL.STRT = 1). Otherwise, operation is not guaranteed. The value of the CH1[5:0] and MCH0[5:0] bits is 111111B when the measurement is stopped.

Remark x = 0 to 3

26. 30.2.6 CTSU Channel Enable Control Registers AL, AH, BL, and BH (CTSUCHACAL, CTSUCHACAH, CTSUCHACBL, CTSUCHACBH) (Page 1272)

Incorrect:

(Omitted)

CHACx	Channel Enable Control
0	Do not measure pins.
1	Measure pins.
The CHACx bits set whether TSm pin measurement is required.	

Caution 1. CHAC63 to CHAC0 are used for setting measurement of TS63 to TS0 pins. Write 0 to unassigned bits. These bits are read as 0.

Caution 2. Set the CHACx bits to 1 for transmit and receive pins whose electrostatic capacitance is to be measured.

Caution 3. Set the CTSUCHACAH, CTSUCHACAL, CTSUCHACBH, and CTSUCHACBL registers when CTSUCRAL.STRT is 0.

Correct:

(Omitted)

CHACm	Channel Enable Control
0	Do not measure pins.
1	Measure pins.
The CHACm bit enables or disables the measurement of the TSm pin. Setting the CHACm bit to 1 enables the capacitance measurement of the TSm pin (both transmission and reception).	

Caution 1. Make sure that the bits to which no measurement pins have been assigned are set to 0.

Caution 2. Set the CTSUCHTRCAH, CTSUCHTRCAL, CTSUCHTRCBH, and CTSUCHTRCBL registers when CTSUCRAL.STRT is 0.

Remark m = 00 to 15, 20 to 35

27. 30.2.7 CTSU Channel Transmit/Receive Control Registers AL, AH, BL, and BH (CTSUCHTRCAL, CTSUCHTRCAH, CTSUCHTRCBL, CTSUCHTRCBH) (Page 1274)

Incorrect:

(Omitted)

CHTRCx	Channel Transmit/Receive Control
0	Reception
1	Transmission
The CHTRCx bits assign the TSm pins to reception or transmission.	

Caution 1. **CHTRC63 to CHTRC0 are used for setting transmit/receive control of TS63 to TS0 pins. Write 0 to unassigned bits. These bits are read as 0.**

Caution 2. The CHTRCx bits assign the TSm pins to reception or transmission. When MD1 is set to 0, if one of these bits is set to 1 (transmission), the corresponding pin can be used for shield signal output. However, when setting as a shield output, do not set two or more bits to 1.

Caution 3. Set the CHTRCx bits to 1 for the TSm pin whose electrostatic capacitance is to be measured. In mutual-capacitance method, set the CHTRCx bits to 1 for transmit and receive pins whose electrostatic capacitance is to be measured.

Caution 4. Set the CTSUCHTRCAH, CTSUCHTRCAL, CTSUCHTRCBH, and CTSUCHTRCBL registers when CTSUCRAL.STRT is 0.

Correct:

(Omitted)

CHTRCm	Channel Transmit/Receive Control
0	Reception
1	Transmission
The CHTRCm bit assigns the TSm pin for use in transmission or reception. When the self-capacitance method is in use (CTSUCRAL.MD1 = 0), setting this bit to 1 (transmission) allows the corresponding pin to be used as an active shield signal output.[Note]	

Note When the active shield output is to be used, do not set multiple bits to 1 at the same time.

Caution 1. Make sure that the bits to which no measurement pins have been assigned are set to 0.

Caution 2. Set the CTSUCHTRCAH, CTSUCHTRCAL, CTSUCHTRCBH, and CTSUCHTRCBL registers when CTSUCRAL.STRT is 0.

Remark m = 00 to 15, 20 to 35

28. 30.2.8 CTSU Status Register L (CTSUSRL) (Page 1276)

Incorrect:

(Omitted)

MFC[1:0]		Multi-clock Counter
0	0	**Multi-clock 0**
0	1	**Multi-clock 1**
1	0	**Multi-clock 2**
1	1	**Multi-clock 3**
The MFC[1:0] bits indicate the clock **that is being measured during** multi-clock measurement (**CTSUCRAH.FCMODE = 1**).		

Correct:

(Omitted)

MFC[1:0]		Multi-clock Counter
0	0	MCA0 (SUCLK0)
0	1	MCA1 (SUCLK1)
1	0	MCA2 (SUCLK2)
1	1	MCA3 (SUCLK3)
The MFC[1:0] bits indicate the clock being used for the multi-clock measurement, i.e., when CTSUCRAH.SDPSEL = 1, CTSUCRAH.PCSEL = 1, and two or more of the CTSUMCH.MCAn bits (n = 0 to 3) are set to 1. Only writing 00B is allowed.		

Note 1. This bit is read-only.

Note 2. To clear the SUCKOVF and SENSOVF bits while CTSUCRAL.INIT is set to 1, do so when the setting of the CTSUCRAL.STRT bit is 0.

Caution Only write to the CTSUSRL register while the setting the CTSUCRAL.STRT bit is 0.

29. 30.2.9 CTSU Sensor Offset Registers 0 and 1 (CTSUSO0, CTSUSO1) (Page 1277, Page 1278)

Incorrect:
(Page 1277)

30.2.9 CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)

(Omitted)

Symbol	15	14	13	12	11	10	9	8
CTSUSO0	SNUM[5:0]						SO[9:8]	

	7	6	5	4	3	2	1	0
	SO[7:0]							

Correct:

30.2.9 CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)

(Omitted)

Symbol	15	14	13	12	11	10	9	8
CTSUSO0	SNUM[5:0]						SO[9:8]	

	7	6	5	4	3	2	1	0
	SO[7:0]							

Write to the CTSUSO0 and CTSUSO1 registers after an INTCTSUWR interrupt is generated. Writing to the CTSUSO1 register causes a transition to state 3. Be sure to write to the CTSUSO0 register before writing to the CTSUSO1 register.
Also, set all 16 bits of the CTSUSO1 register at once.

(Page 1277)

SDPA[7:0]	Sensor Driving Pulse Divisor Setting

• When CTSUCRAH.SDPSEL = 0

The operating clock is divided to generate a base clock to be the source of sensor drive pulse.
These bits are also available for setting the voltage stabilization time of the CTSU.

0	0	0	0	0	0	0	0	Operating clock divided by 2[Note]
0	0	0	0	0	0	0	1	Operating clock divided by 4
0	0	0	0	0	0	1	0	Operating clock divided by 6
0	0	0	0	0	0	1	1	Operating clock divided by 8
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	Operating clock divided by 510
1	1	1	1	1	1	1	1	Operating clock divided by 512

Note When jitter application is disabled (CTSUCRBL.SOFF bit = 1) in the mutual capacitance method, setting of SDPA[7:0] = 00000000B is prohibited.

• When CTSUCRAH.SDPSEL = 1

The SUCLK clock is divided to generate a sensor drive pulse.

0	0	0	0	0	0	0	0	SUCLK divided by 1
0	0	0	0	0	0	0	1	SUCLK divided by 2
0	0	0	0	0	0	1	0	SUCLK divided by 3
0	0	0	0	0	0	1	1	SUCLK divided by 4
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	SUCLK divided by 255
1	1	1	1	1	1	1	1	SUCLK divided by 256

SDPA[7:0]	Base Clock (Sensor Drive Pulse Frequency Divisor) Setting

• In random pulse mode (CTSUCRAH.SDPSEL = 0)

The operating clock is divided to generate a base clock to be the source of sensor drive pulse. These bits are also available for setting the voltage stabilization time of the CTSU. When the setting of these bits is n, the base clock is obtained by frequency-dividing the operating clock by 2 (n+1).

0	0	0	0	0	0	0	0	Operating clock divided by 2 Note 1
0	0	0	0	0	0	0	1	Operating clock divided by 4
0	0	0	0	0	0	1	0	Operating clock divided by 6
0	0	0	0	0	0	1	1	Operating clock divided by 8
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	Operating clock divided by 510
1	1	1	1	1	1	1	1	Operating clock divided by 512

• In high-resolution pulse mode (CTSUCRAH.SDPSEL = 1)

The SUCLK clock is divided to generate a sensor drive pulse. The frequency of SUCLK is determined by the following equation.

SUCLK = STCLK × SUCLK multiplication rate setting made by the CTSUSUCLKx.SUMULTIx[7:0] bits

When the setting of these bits is n, the sensor drive pulses are obtained by frequency-dividing the SUCLK clock by 2 (n+1).

0	0	0	0	0	0	0	0	SUCLK divided by 2
0	0	0	0	0	0	0	1	SUCLK divided by 4
0	0	0	0	0	0	1	0	SUCLK divided by 6
0	0	0	0	0	0	1	1	SUCLK divided by 8
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	SUCLK divided by 510
1	1	1	1	1	1	1	1	SUCLK divided by 512

(Page 1278)

SSDIV[3:0]				Spectrum Diffusion Sampling Cycle Control
The SSDIV[3:0] bits are valid only when CTSUCRAH.SDPSEL is 0. **Sampling cycle (divided by 1 to 16) can be set for the jitter application function.**				
0	0	0	0	Divided by 1
0	0	0	1	Divided by 2
:	:	:	:	:
1	1	1	0	Divided by 15
1	1	1	1	Divided by 16
The SSDIV[3:0] bits set the sampling cycle of the **jitter application function**. Set the sampling cycle to less than 1/4 of the sensor drive pulse cycle. **Set these bits for the pin to be measured after a request to write to a configuration register of an individual CTSU channel (INTCTSUWR) is generated.**				

(Omitted)

After a request to write to a configuration register of an individual CTSU channel (INTCTSUWR) is generated, write to the CTSUSO register, which causes a transition to Status 3. Therefore, when writing a value to the CTSUSO register, set all bits at a time.

SSDIV[3:0]Note 2				Spectrum Diffusion Sampling Cycle Control
0	0	0	0	Divided by 1
0	0	0	1	Divided by 2
:	:	:	:	:
1	1	1	0	Divided by 15
1	1	1	1	Divided by 16
The SSDIV[3:0] bits set the sampling cycle of the spread spectrum. Set the clock division ratio for resampling the sensor drive pulse (synchronized with fCLK) with SUCLK. Set these bits so that the sampling cycle is less than 1/4 of the sensor drive pulse cycle. Set these bits for the pin to be measured next after an INTCTSUWR interrupt is generated.				

(Omitted)

Note 1. When the mutual capacitance method is selected (CTSUCRAL.MD1 = 1) or the spread spectrum is disabled (CTSUCRBL.SOFF = 1), setting SDPA[7:0] = 00000000B is prohibited.

Note 2. The SSDIV[3:0] bits are only valid when the CTSUCRAH.SDPSEL bit is 0 (random pulse mode).

30. 30.2.10 CTSU Sensor Counter Registers L and H (CTSUSC, CTSUUC) (Page 1279)

Incorrect:

30.2.10 CTSU sensor counter registers **L and H** (CTSUSC, CTSUUC)

(Omitted)

SC[15:0]	Sensor Counter
This register shows the measurement result of the sensor counter. When an overflow occurs, this counter shows FFFH.	

Correct:

30.2.10 CTSU sensor counter registers (CTSUSC, CTSUUC)

(Omitted)

SC[15:0]	Sensor Counter
This register shows the measurement result of the sensor counter. When an overflow occurs, this counter indicates FFFH.	

Read these registers when an INTCTSURD interrupt is generated. Reading these registers the number of times specified by the CTSUDBGR0.CNTRDSEL bit causes measurement to transition to state 0 or 2. The register value is cleared immediately before transition to state 4 (CTSUSRL.STC[2:0] = 100B) in the next measurement. This register is also cleared by writing 1 to the CTSUCRAL.INIT bit.

- When CTSUDBGR0.CNTRDSEL = 0

  Reading the CTSUSC register or CTSUUC register once causes measurement to transition to the next state and both registers are cleared before transition to state 4. If the user require the measurement result, be sure to read the CTSUSC register.

- When CTSUDBGR0.CNTRDSEL = 1

  Reading the CTSUSC or CTSUUC register twice causes measurement to transition to the next state. Use this setting if the user require the results of both the CTSUSC and CTSUUC registers by 16-bit access.

31. 30.2.13 CTSU Trimming Registers AL and AH (CTSUTRIM0, CTSUTRIM1) (Page 1285, Page 1286)

Incorrect:
(Page 1285)

(Omitted)

Address: F0600H, F0601H (CTSUTRIM0), F0602H, F0603H (CTSUTRIM1)

After reset: 0000H, 0000H

R/W: R/W

(Omitted)

DACTRIM[7:0]	Offset Current DAC Upper/Lower Matching Variation Adjustment

The DACTRIM[7:0] bits adjust the upper/lower matching variation (coefficient of the lower current source) of the offset current DAC. These bits hold the initial value set at the factory. Do not modify this value.

0	0	0	0	0	0	0	0	× 0.0
:	:	:	:	:	:	:	:	:
0	1	1	0	0	0	0	0	× 0.875
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	× 1.0
:	:	:	:	:	:	:	:	:
1	0	0	1	0	0	0	0	× 1.125
:	:	:	:	:	:	:	:	:
1	0	1	0	0	0	1	1	× 1.273
Other than above: Setting prohibited								

Correct:

(Omitted)

Address: F0600H, F0601H (CTSUTRIM0), F0602H, F0603H (CTSUTRIM1)

After reset: Note

R/W: R/W

(Omitted)

DACTRIM[7:0]	Offset Current Adjustment

The DACTRIM[7:0] bits are used to adjust the DAC coefficient for offset current. These bits hold the initial value set as shipped. Do not modify this value.

(Page 1286)

RTRIM[7:0]	Reference Resistance Adjustment

The RTRIM[7:0] bits adjust the reference resistance value.
These bits hold the initial value set at the factory. Do not modify this value.

RTRIM[7:0]								Resistance value
0	0	0	0	0	0	0	0	Low
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	High

RTRIM[7:0]	Reference Resistance Adjustment

The RTRIM[7:0] bits are used to adjust the value of the internal reference resistor. These bits hold the initial value set as shipped. Do not modify this value.

Note The value following a reset is the value adjusted as shipped.

32. 30.2.14 CTSU Trimming Registers BL and BH (CTSUTRIM2, CTSUTRIM3) (Page 1287)

Incorrect:

Figure 30 - 18 Format of CTSU Trimming Registers BL and BH (CTSUTRIM2, CTSUTRIM3)

Address: F0604H, F0605H (CTSUTRIM2), F0606H, F0607H (CTSUTRIM3)
After reset: **0000H, 0000H**
R/W: R/W

(Omitted)

Correct:

Figure 30 - 18 Format of CTSU Trimming Registers BL and BH (CTSUTRIM2, CTSUTRIM3)

Address: F0604H, F0605H (CTSUTRIM2), F0606H, F0607H (CTSUTRIM3)
After reset: Note
R/W: R/W

(Omitted)

Note The value following a reset is the value adjusted as shipped.

33. Added Description of TSCAP pin (new)

Incorrect:

Not applicable

Correct:

30.4.2 TSCAP pin

A capacitor must be connected to the TSCAP pin to stabilize the internal voltage of the CTSU. Make sure the wiring between the TSCAP pin and the capacitor, and between the capacitor and GND, is as thick and as short as possible.

Table 30 - 3 states the condition for the capacitor to be connected to the TSCAP pin.

Table 30 - 3 Condition for the Capacitor to be Connected to the TSCAP Pin

Item	Symbol	Condition
Capacitance of the smoothing capacitor to be externally connected to the TSCAP pin	C_{TSCAP}	10 nF ±10%Note

Note Use a multilayer ceramic capacitor with a stated capacitance of 10 nF and a capacitance tolerance no greater than ±10%. Select from among those with a capacitance change limited to ±15% in accord with the usage environment, such as X7R as specified by the EIA standard.

Before setting the CTSUCRAL.CSW bit to 1 (the external capacitance connection switch turned on), the capacitor connected to the TSCAP pin must output a low level from the port to which the TSCAP function is assigned and be fully discharged.