Date: May 22, 2025

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0144A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G22 Descriptions in the User's Manual: Hardware Rev. 1.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G22 Group	Lot No. All lots	Reference Document	RL78/G22 User's Manual: Hardware Rev. 1.10 R01UH0978EJ0110 (Jun. 2024)		

This document describes misstatements found in the RL78/G22 User's Manual: Hardware Rev. 1.10 (R01UH0978EJ0110).

Corrections

Applicable Item	Applicable Page	Contents
Table 1 - 9 Multiplexed Pin Functions of the 40-pin Products (1/2)	Page 23	Incorrect descriptions revised
Table 1 - 10 Multiplexed Pin Functions of the 44-pin Products (1/2)	Page 26	Incorrect descriptions revised
2.2.3.2 Connecting the VBAT pin to the battery for use in backing up	Page 62	Incorrect descriptions revised
2.2.3.3 Using the VBAT pin	Page 63	Incorrect descriptions revised
2.4 Block Diagrams of Pins	Page 83, Page 86	Incorrect descriptions revised
4.5.4 Examples of register settings for port and alternate functions	Page 178	Incorrect descriptions revised
6.1 Functions of Clock Generator	Page 193	Incorrect descriptions revised
12.6.7 Hardware trigger no-wait mode (scan mode, sequential conversion mode)	Page 474	Incorrect descriptions revised
12.6.9 Hardware trigger wait mode (select mode, sequential conversion mode)	Page 476	Incorrect descriptions revised
Figure 13 - 1 Block Diagram of Serial Array Unit 0	Page 503	Incorrect descriptions revised
13.3.13 Serial output register m (SOm)	Page 525	Incorrect descriptions revised
15.3.4 Baud rate generator	Page 797	Incorrect descriptions revised
16.4.3 Repeat mode	Page 824	Incorrect descriptions revised
Table 18 - 2 Flags Corresponding to Interrupt Request Sources (3/4)	Page 847	Incorrect descriptions revised
34.2.3 Characteristics of the On-chip Oscillators	Page 1150	Incorrect descriptions revised
34.3.2 Characteristics of the supply current	Page 1156, Page1159	Incorrect descriptions revised
34.6.1 Characteristics of the A/D converter for TA = -40 to +85°C	Page 1202	Incorrect descriptions revised
34.6.2 Characteristics of the A/D converter for TA = -40 to +105°C	Page 1208	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No.	English	R01UH0978EJ0110
1	Table 1 - 9 Multiplexed Pin Functions of the 40-pin Products (1/2)			Page 23	Page 3
2	Table 1 - 10 Multiplexed Pin Functions of the 44-pin Products (1/2)			Page 26	Page 4
3	2.2.3.2 Connecting the VBAT pin to the battery for use in backing up			Page 62	Page 5
4	2.2.3.3 Using the VBAT pin			Page 63	Page 6
5	2.4 Block Diagrams of Pins			Page 83, Page 86	Page 7, Page8
6	4.5.4 Examples of register settings for port and alternate functions			Page 178	Page 9
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10	Figure 13 - 1 Block Diagram of Serial Array Unit 0			Page 503	Page 12
11	13.3.13 Serial output register m (SOm)			Page 525	Page 12
12	15.3.4 Baud rate generator			Page 797	Page 13
13	16.4.3 Repeat mode			Page 824	Page 14 ,Page 15
14	Table 18 - 2 Flags Corresponding to Interrupt Request Sources (3/4)			Page 847	Page 16
15	34.2.3 Characteristics of the On-chip Oscillators			Page 1150	Page 17
16	34.3.2 Characteristics of the supply current			Page 1156, Page1159	Page 18, Page 19
17	34.6.1 Characteristics of the A/D converter for TA = -40 to +85°C			Page 1202	Page 20
18	34.6.2 Characteristics of the A/D converter for TA = -40 to +105°C			Page 1208	Page 21

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G22 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0144A/E	May 22, 2025	First edition issued Corrections No.1 to No.18 revised

1. Table 1 - 9 Multiplexed Pin Functions of the 40-pin Products (1/2) (Page 23)

Incorrect:

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
40HWQFN	Digital port		A/D converter (ADC)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P40	TOOL0	—	—	—	—	—	—	—	—	—
2	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
3	P124	XT2/EXCLKS	—	—	—	—	—	—	—	—	—
4	P123	XT1	—	—	—	—	—	—	—	—	—
5	P137	—	—	INTP0	—	—	—	—	—	—	—
6	P122	X2/EXCLK	—	—	—	—	—	—	—	—	—
7	P121	X1/VBAT	—	—	—	—	—	—	—	—	—
8	—	REGC	—	—	—	—	—	—	—	—	—
9	—	V_{SS}	—	—	—	—	—	—	—	—	—
10	—	V_{DD}	—	—	—	—	—	—	—	—	—
11	P60	—	—	—	—	—	—	—	—	SCLA0	—
12	P61	—	—	—	—	—	—	—	—	SDAA0	—
13	P62	—	—	—	—	—	—	—	—	—	—
14	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
15	P73	—	—	—	KR3	TS05	—	—	—	—	—
16	P72	—	—	—	KR2	TS04	—	—	SO21	—	~~TxDA1~~
17	P71	—	—	—	KR1	TS03	—	—	SI21/ SDA21	—	RxDA0

(omitted)

Correct:

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
40HWQFN	Digital port		A/D converter (ADC)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P40	TOOL0	—	—	—	—	—	—	—	—	—
2	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
3	P124	XT2/EXCLKS	—	—	—	—	—	—	—	—	—
4	P123	XT1	—	—	—	—	—	—	—	—	—
5	P137	—	—	INTP0	—	—	—	—	—	—	—
6	P122	X2/EXCLK	—	—	—	—	—	—	—	—	—
7	P121	X1/VBAT	—	—	—	—	—	—	—	—	—
8	—	REGC	—	—	—	—	—	—	—	—	—
9	—	V_{SS}	—	—	—	—	—	—	—	—	—
10	—	V_{DD}	—	—	—	—	—	—	—	—	—
11	P60	—	—	—	—	—	—	—	—	SCLA0	—
12	P61	—	—	—	—	—	—	—	—	SDAA0	—
13	P62	—	—	—	—	—	—	—	—	—	—
14	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
15	P73	—	—	—	KR3	TS05	—	—	—	—	—
16	P72	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0
17	P71	—	—	—	KR1	TS03	—	—	SI21/ SDA21	—	RxDA0

(omitted)

2. Table 1 - 9 Multiplexed Pin Functions of the 44-pin Products (1/2) (Page 26)

Incorrect:

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
44LQFP	Digital port		A/D converter (ADC)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P41	—	—	—	—	—	TI07/TO07	—	—	—	—
2	P40	TOOL0	—	—	—	—	—	—	—	—	—
3	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
4	P124	XT2/EXCLKS	—	—	—	—	—	—	—	—	—
5	P123	XT1	—	—	—	—	—	—	—	—	—
6	P137	—	—	INTP0	—	—	—	—	—	—	—
7	P122	X2/EXCLK	—	—	—	—	—	—	—	—	—
8	P121	X1/VBAT	—	—	—	—	—	—	—	—	—
9	—	REGC	—	—	—	—	—	—	—	—	—
10	—	V_{SS}	—	—	—	—	—	—	—	—	—
11	—	V_{DD}	—	—	—	—	—	—	—	—	—
12	P60	—	—	—	—	—	—	—	—	SCLA0	—
13	P61	—	—	—	—	—	—	—	—	SDAA0	—
14	P62	—	—	—	—	—	—	—	—	—	—
15	P63	—	—	—	—	—	—	—	—	—	—
16	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
17	P73	—	—	—	KR3	TS05	—	—	—	—	—
18	P72	—	—	—	KR2	TS04	—	—	SO21	—	TxDA1
19	P71	—	—	—	KR1	TS03	—	—	SI21/ SDA21	—	RxDA0

(omitted)

Correct:

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI			Timers		Communications Interfaces		
44LQFP	Digital port		A/D converter (ADC)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2La)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P41	—	—	—	—	—	TI07/TO07	—	—	—	—
2	P40	TOOL0	—	—	—	—	—	—	—	—	—
3	—	$\overline{\text{RESET}}$	—	—	—	—	—	—	—	—	—
4	P124	XT2/EXCLKS	—	—	—	—	—	—	—	—	—
5	P123	XT1	—	—	—	—	—	—	—	—	—
6	P137	—	—	INTP0	—	—	—	—	—	—	—
7	P122	X2/EXCLK	—	—	—	—	—	—	—	—	—
8	P121	X1/VBAT	—	—	—	—	—	—	—	—	—
9	—	REGC	—	—	—	—	—	—	—	—	—
10	—	V_{SS}	—	—	—	—	—	—	—	—	—
11	—	V_{DD}	—	—	—	—	—	—	—	—	—
12	P60	—	—	—	—	—	—	—	—	SCLA0	—
13	P61	—	—	—	—	—	—	—	—	SDAA0	—
14	P62	—	—	—	—	—	—	—	—	—	—
15	P63	—	—	—	—	—	—	—	—	—	—
16	P31	PCLBUZ0	—	INTP4	—	TS01	TI03/TO03	—	—	—	—
17	P73	—	—	—	KR3	TS05	—	—	—	—	—
18	P72	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0
19	P71	—	—	—	KR1	TS03	—	—	SI21/ SDA21	—	RxDA0

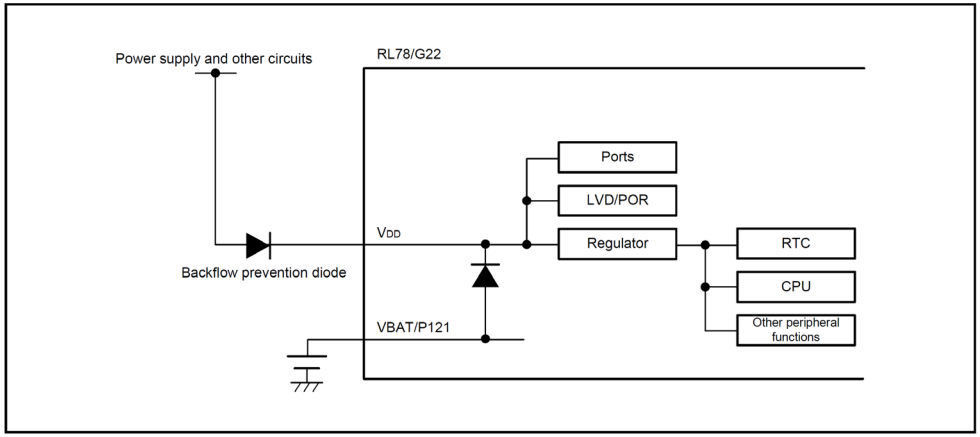
(omitted)

3. **2.2.3.2 Connecting the VBAT pin to the battery for use in backing up (Page 62)**

Incorrect:

(omitted)

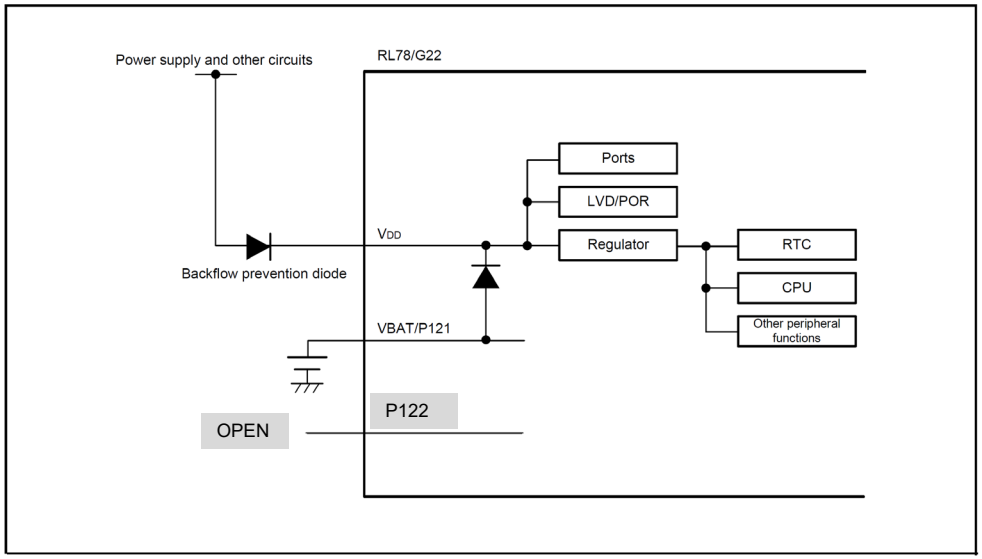
Figure 2 - 1 Example of the Connection of the VBAT Pin



Correct:

(omitted)

Figure 2 - 1 Example of the Connection of the VBAT Pin



4. 2.2.3.3 Using the VBAT pin (Page 63)

Incorrect:

How to make the initial settings for the VBAT pin and an example of the procedure for switching the power supply pin to the VBAT pin are described below. This processing is to be completed before the voltage on the VDD pin falls below that supplied from the VBAT pin. In addition, Figure 2 - 2 shows the state transitions in switching the power supply pin between the VDD and VBAT pins.

1. Making the initial settings for the VBAT pin
   Set the P121 pin to X1 oscillation mode (by setting the EXCLK and OSCSEL bits of the CMC register to 0 and 1,
   respectively, and the MSTOP bit of the CSC register to **0**) in the initial settings.

(omitted)

Correct:

How to make the initial settings for the VBAT pin and an example of the procedure for switching the power supply pin to the VBAT pin are described below. This processing is to be completed before the voltage on the VDD pin falls below that supplied from the VBAT pin. In addition, Figure 2 - 2 shows the state transitions in switching the power supply pin between the VDD and VBAT pins.

1. Making the initial settings for the VBAT pin
   Set the P121 pin to X1 oscillation mode (by setting the EXCLK and OSCSEL bits of the CMC register to 0 and 1,
   respectively, and the MSTOP bit of the CSC register to 1) in the initial settings.

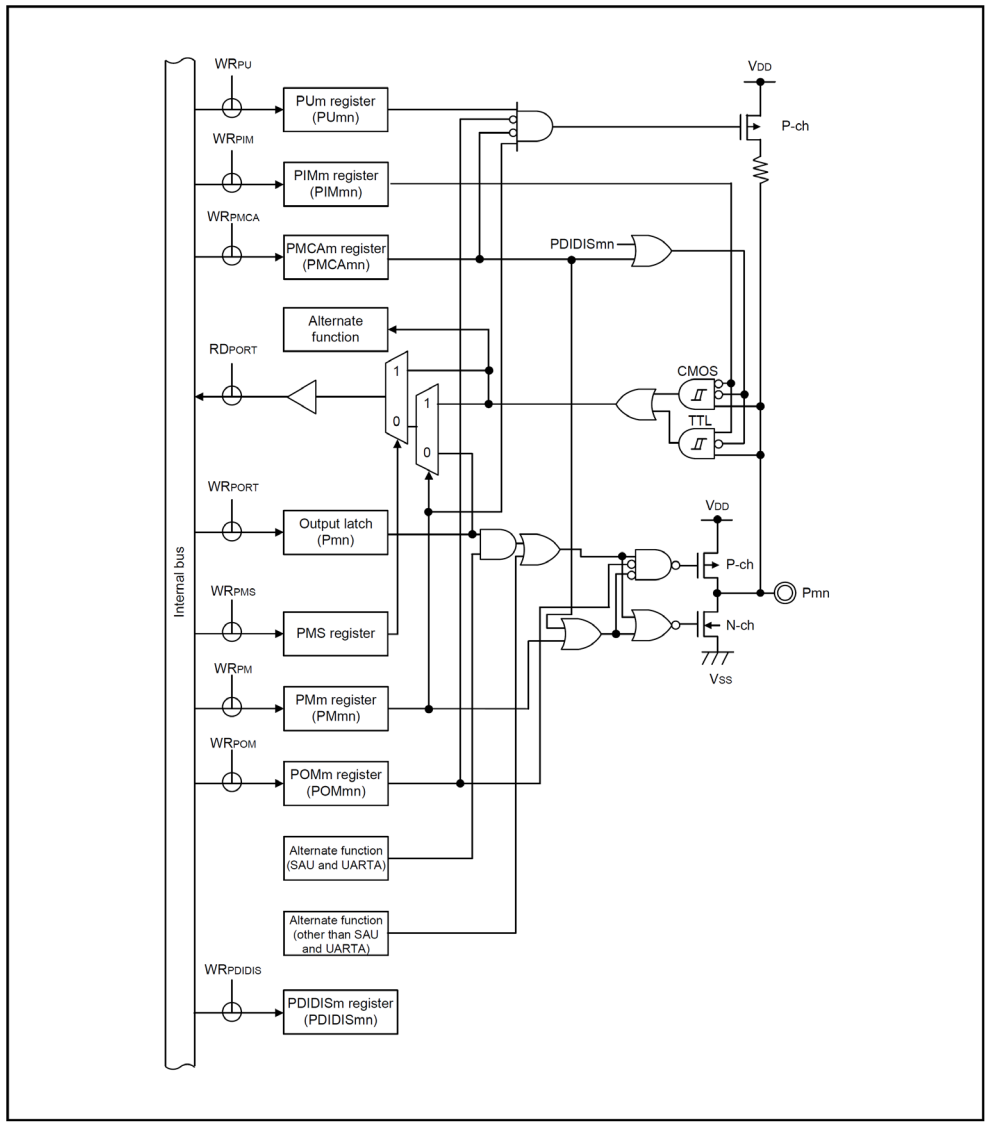
(omitted)

5. 2.4 Block Diagrams of Pins

Incorrect:

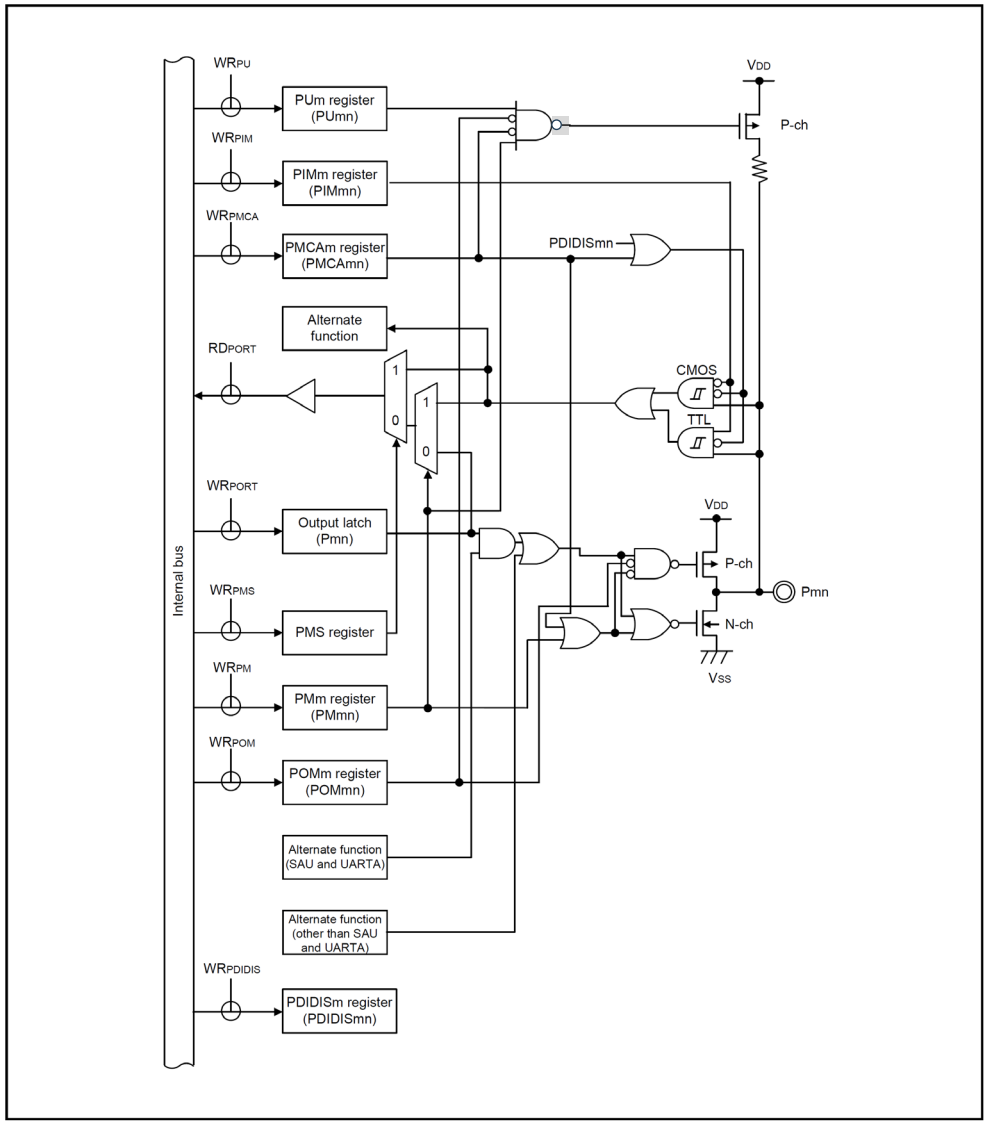
(page 83)

Figure 2 - 22 Pin Block Diagram for Pin Type 8-6-9



Correct:

Figure 2 - 22 Pin Block Diagram for Pin Type 8-6-9



(page 86)

Figure 2 - 24 Pin Block Diagram for Pin Type 8-31-2

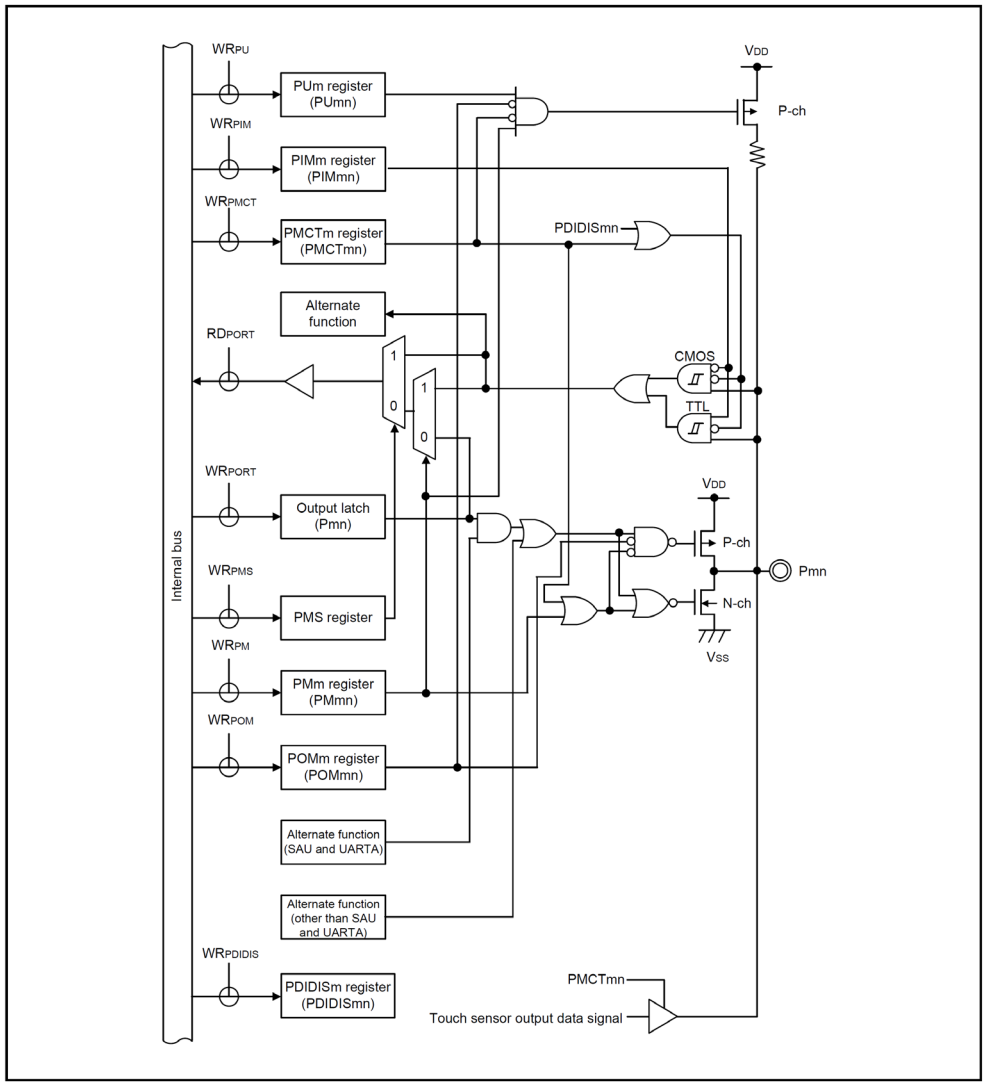
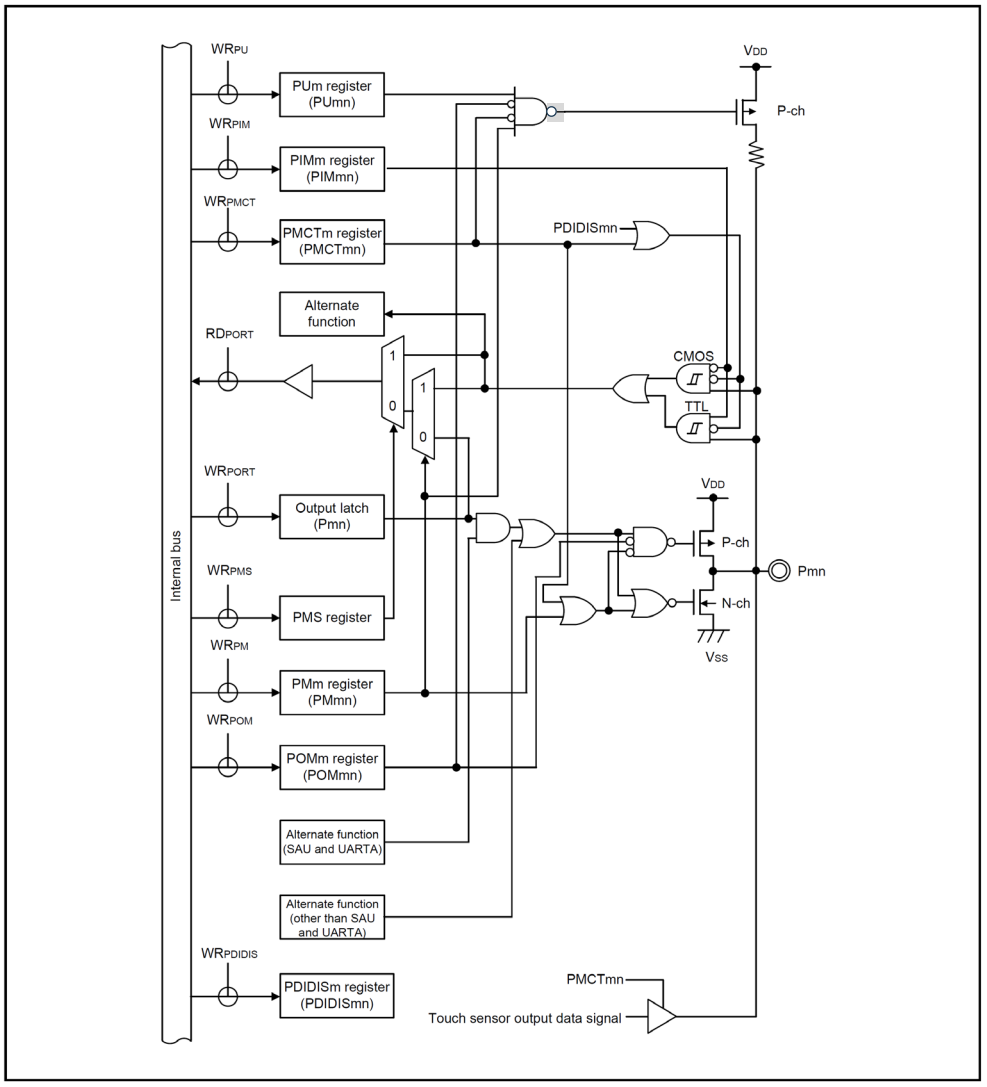


Figure 2 - 24 Pin Block Diagram for Pin Type 8-31-2



6. 4.5.4 Examples of register settings for port and alternate functions (Page 178)

Incorrect:

Table 4 - 5 Examples of Register and Output Latch Settings for Alternate Functions (13/15)

Pin Name	Function Used		CMC		PMxx	Pxx	16-pin	20-pin	24-pin	25-pin	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
	Function Name	I/O	EXCLK, OSCSEL, EXCLKS, OSCSELS	XTSEL												
P121	P121	Input	00xx/10xx/11xx	0	1	×	√	√	√	√	√	√	√	√	√	√
			xx00/xx10/xx11	1Note												
		Output	00xx/10xx/11xx	0	0	0/1										
			xx00/xx10/xx11	1Note												
	VBAT	**Input**	**00xx/10xx/11xx**	0	**0**	**1**	—	—	—	—	—	—	—	√	√	√
	X1	—	01xx	0	1	×	√	√	√	√	√	√	√	√	√	√
	XT1	—	xx01	1	1	×	√	√	√	√	√	√	√	—	—	—
P122	P122	Input	00xx/10xx	0	1	×	√	√	√	√	√	√	√	√	√	√
			xx00/xx10	1Note												
		Output	00xx/10xx	0	0	0/1										
			xx00/xx10	1Note												
	X2	—	01xx	0	1	×	√	√	√	√	√	√	√	√	√	√
	XT2	—	xx01	1	1	×	√	√	√	√	√	√	√	—	—	—
	EXCLK	Input	11xx	0	1	×	√	√	√	√	√	√	√	√	√	√
	EXCLKS	Input	xx11	1	1	×	√	√	√	√	√	√	√	√	√	√
P123	P123	Input	xx00/xx10/xx11	0	—	×	—	—	—	—	—	—	—	√	√	√
	XT1	—	xx01	0	—	×	—	—	—	—	—	—	—	√	√	√
P124	P124	Input	xx00/xx10	0	—	×	—	—	—	—	—	—	—	√	√	√
	XT2	—	xx01	0	—	×	—	—	—	—	—	—	—	√	√	√
	EXCLKS	Input	xx11	0	—	×	—	—	—	—	—	—	—	√	√	√

Note This setting is only applicable in the 16- to 36-pin products.

Correct:

Table 4 - 5 Examples of Register and Output Latch Settings for Alternate Functions (13/15)

Pin Name	Function Used		CMC		PMxx	Pxx	16-pin	20-pin	24-pin	25-pin	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
	Function Name	I/O	EXCLK, OSCSEL, EXCLKS, OSCSELS	XTSEL												
P121	P121	Input	00xx/10xx/11xx	0	1	×	√	√	√	√	√	√	√	√	√	√
			xx00/xx10/xx11	1Note												
		Output	00xx/10xx/11xx	0	0	0/1										
			xx00/xx10/xx11	1Note												
	VBAT	—	01xx	0	1	0	—	—	—	—	—	—	—	√	√	√
	X1	—	01xx	0	1	×	√	√	√	√	√	√	√	√	√	√
	XT1	—	xx01	1	1	×	√	√	√	√	√	√	√	—	—	—
P122	P122	Input	00xx/10xx	0	1	×	√	√	√	√	√	√	√	√	√	√
			xx00/xx10	1Note												
		Output	00xx/10xx	0	0	0/1										
			xx00/xx10	1Note												
	X2	—	01xx	0	1	×	√	√	√	√	√	√	√	√	√	√
	XT2	—	xx01	1	1	×	√	√	√	√	√	√	√	—	—	—
	EXCLK	Input	11xx	0	1	×	√	√	√	√	√	√	√	√	√	√
	EXCLKS	Input	xx11	1	1	×	√	√	√	√	√	√	√	√	√	√
P123	P123	Input	xx00/xx10/xx11	0	—	×	—	—	—	—	—	—	—	√	√	√
	XT1	—	xx01	0	—	×	—	—	—	—	—	—	—	√	√	√
P124	P124	Input	xx00/xx10	0	—	×	—	—	—	—	—	—	—	√	√	√
	XT2	—	xx01	0	—	×	—	—	—	—	—	—	—	√	√	√
	EXCLKS	Input	xx11	0	—	×	—	—	—	—	—	—	—	√	√	√

Note This setting is only applicable in the 16- to 36-pin products.

7. 6.1 Functions of Clock Generator (Page 193)

Incorrect:

The clock generator generates clocks to be supplied to the CPU and peripheral hardware.
The following kinds of system clocks and clock oscillators are selectable.

(omitted)

The frequencies that can be specified for the high-speed on-chip oscillator by using the option byte and the high-speed on-chip oscillator frequency select register (HOCODIV) are shown below.

Power Supply Voltage	Oscillation Frequency (MHz)									
	1	2	3	4	6	8	12	16	24	32
1.8 V ≤ V_{DD} ≤ 5.5 V	√	√	√	√	√	√	√	√	√	√
1.6 V ≤ V_{DD} ≤ 5.5 V	√	√	⎓	⎓	—	—	—	—	—	—

(omitted)

Correct:

The clock generator generates clocks to be supplied to the CPU and peripheral hardware.
The following kinds of system clocks and clock oscillators are selectable.

(omitted)

The frequencies that can be specified for the high-speed on-chip oscillator by using the option byte and the high-speed on-chip oscillator frequency select register (HOCODIV) are shown below.

Power Supply Voltage	Oscillation Frequency (MHz)									
	1	2	3	4	6	8	12	16	24	32
1.8 V ≤ V_{DD} ≤ 5.5 V	√	√	√	√	√	√	√	√	√	√
1.6 V ≤ V_{DD} ≤ 5.5 V	√	√	√	√	—	—	—	—	—	—

(omitted)

8. **12.6.7 Hardware trigger no-wait mode (scan mode, sequential conversion mode) (Page 474)**

Incorrect:

<1> Setting the ADCE bit of A/D converter mode register 0 (ADM0) to 1 in the stop state places the A/D converter in the standby state.

(omitted)

<9> When ADCE is cleared to 0 while in the A/D conversion standby state, the A/D converter enters the stop state. **When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start.**

(omitted)

Correct:

<1> Setting the ADCE bit of A/D converter mode register 0 (ADM0) to 1 in the stop state places the A/D converter in the standby state.

(omitted)

<9> When ADCE is cleared to 0 while in the A/D conversion standby state, the A/D converter enters the stop state. In this state, input of a hardware trigger is ignored and A/D conversion does not start.

(omitted)

9. **12.6.9 Hardware trigger wait mode (select mode, sequential conversion mode) (Page 476)**

Incorrect:

<1> Setting the ADCE bit of A/D converter mode register 0 (ADM0) to 1 in the stop state places the A/D converter in the hardware trigger standby state.

(omitted)

<7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the hardware trigger standby state is entered, and the A/D converter is placed in the stop state. **When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.**

(omitted)

Correct:

<1> Setting the ADCE bit of A/D converter mode register 0 (ADM0) to 1 in the stop state places the A/D converter in the hardware trigger standby state.

(omitted)

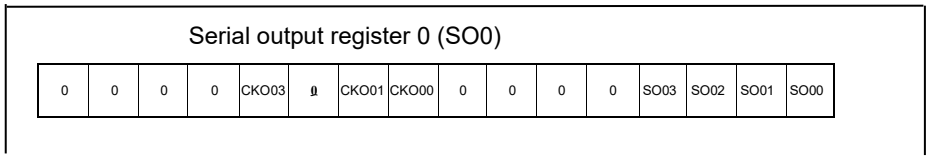
<7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the hardware trigger standby state is entered, and the A/D converter is placed in the stop state.

<8> When ADCE is cleared to 0 in the hardware trigger standby state, the A/D converter is placed in the stop state. When ADCE = 0, input of a hardware trigger is ignored and A/D conversion does not start.

(omitted)

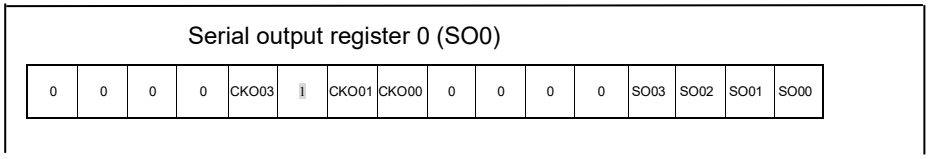
10. Figure 13 - 1 Block Diagram of Serial Array Unit 0 (Page 503)

Incorrect:



(omitted)

Correct:



(omitted)

11. 13.3.13 Serial output register m (SOm) (Page 525)

Incorrect:

(omitted)

Caution Be sure to clear bits 15 to 12, **10**, and 7 to 4 of the SO0 register to 0.
Be sure to clear bits 15 to 10 and 7 to 2 of the SO1 register to 0.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)

Correct:

(omitted)

Caution Be sure to clear bits 15 to 12, and 7 to 4 of the SO0 register to 0. Be sure to set bit 10 of the SO0 register to 1. Be sure to clear bits 15 to 10 and 7 to 2 of the SO1 register to 0.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3)

12. 15.3.4 Baud rate generator (Page 797)

Incorrect:

After the start bit is detected, the latch timing of receive data is determined by the counter specified with the baud rate generator control register (BRGCAn). If the whole frame including the stop bit has been received before this latching, reception can proceed correctly. Assuming that 11 bits of data are received, the theoretical values can be calculated as follows.

- The relation between 1-bit data length and baud rate
  FL = (Brate) - 1
  Brate: Baud rate of UART
  k: Set value of BRGCAn register
  FL: 1-bit data length
  Margin of latch timing: 1 clock

- Minimum permissible data frame length (FLmin)

$$FLmin = 11 \times FL - \frac{k - 1}{2k} \times FL = \frac{21k + 1}{2k} FL$$

- Maximum permissible baud rate for reception on the transmitting side (BRmax)

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k + 1} Brate$$

- Maximum permissible data frame length (FLmax)

$$FLmax = \frac{21k+1}{20k} FL \times 11$$

- Minimum permissible baud rate for reception on the transmitting side (BRmin)

$$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k - 1} Brate$$

Table 15 - 5 shows the permissible baud rate error between UART and the transmitting side can be calculated from the above minimum and maximum baud rate expressions.

Table 15 - 5 Maximum/Minimum Permissible Baud Rate Error

Division ratio (k)	Maximum permissible baud rate error	Minimum permissible baud rate error
2	+2.32%	-2.43%
4	+3.52%	-3.61%
8	+4.14%	-4.19%
20	+4.51%	-4.53%
50	+4.66%	-4.67%
100	+4.71%	-4.71%
255	+4.74%	-4.74%

Remark 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the division ratio (k), the higher the permissible error.
Remark 2. k: Set value of BRGCAn register

Correct:

After the start bit is detected, the latch timing of receive data is determined by the counter specified with the baud rate generator control register (BRGCAn). If the whole frame including the stop bit has been received before this latching, reception can proceed correctly. Assuming that 11 bits of data are received, the theoretical values can be calculated as follows.

- The relation between 1-bit data length and baud rate
  FL = (Brate) - 1
  Brate: Baud rate of UART
  k: Set value of BRGCAn register
  FL: 1-bit data length
  Margin of latch timing: 2 clock

- Minimum permissible data frame length (FLmin)

k = 3 to 255: $FLmin = 11 \times FL - \frac{k - 2}{2k} \times FL = \frac{21k + 2}{2k} FL$

- Maximum permissible baud rate for reception on the transmitting side (BRmax)

k = 2: $BRmax = Brate + \frac{1}{22k} Brate$

k = 3 to 255: $BRmax = (FLmin/11)^{-1} = \frac{22k}{21k + 2} Brate$

- Maximum permissible data frame length (FLmax)

k = 3 to 255: $FLmax = \frac{21k + 2}{20k} FL \times 11$

- Minimum permissible baud rate for reception on the transmitting side (BRmin)

k = 2: $BRmin = Brate - \frac{1}{22k} Brate$

k = 3 to 255: $BRmin = (FLmax/11)^{-1} = \frac{20k}{21k - 2} Brate$

Table 15 - 5 shows the permissible baud rate error between UART and the transmitting side can be calculated from the above minimum and maximum baud rate expressions.

Table 15 - 5 Maximum/Minimum Permissible Baud Rate Error

Division ratio (k)	Maximum permissible baud rate error	Minimum permissible baud rate error
2	+2.27%	-2.27%
4	+2.33%	-2.44%
8	+3.53%	-3.61%
20	+4.27%	-4.31%
50	+4.56%	-4.58%
100	+4.66%	-4.67%
255	+4.72%	-4.73%

Remark 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the division ratio (k), the higher the permissible error.
Remark 2. k: Set value of BRGCAn register

13. 16.4.3 Repeat mode (Page 824)

Incorrect:

(omitted)

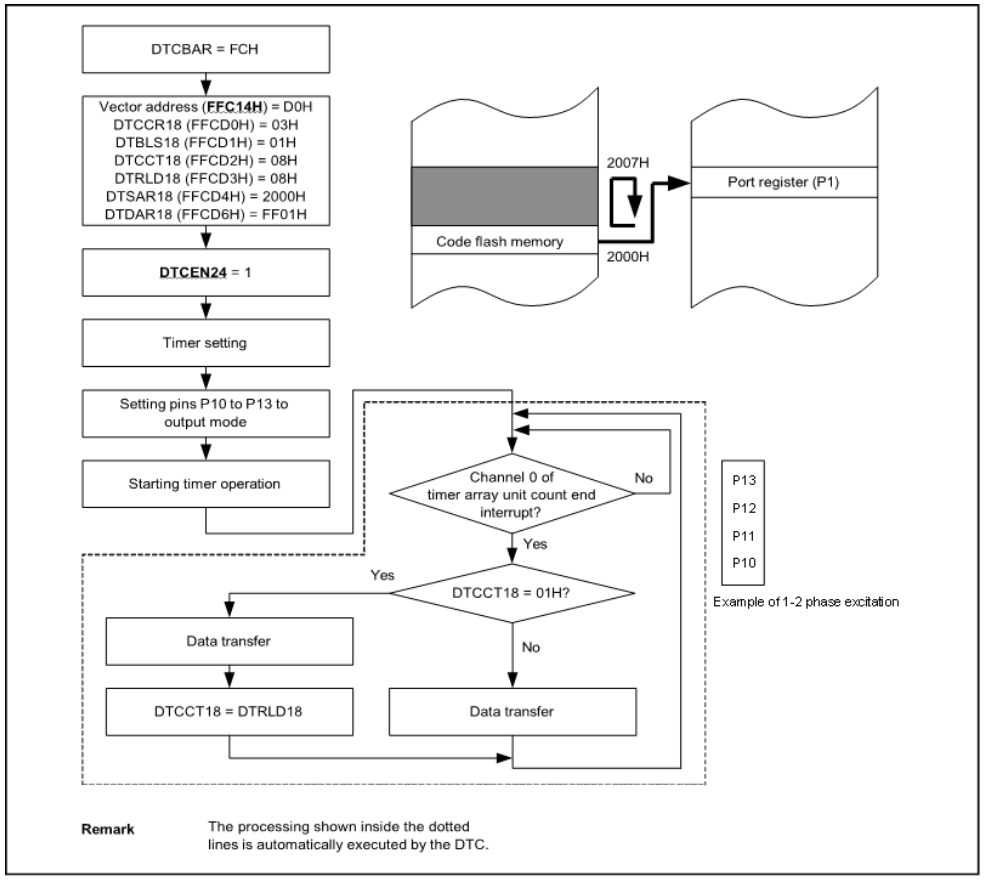
(1) Example 1 of using repeat mode: Outputting stepping motor control pulses using port pins
The DTC is activated using the interval timer function of channel 0 of timer array unit 0, and the patterns of the motor control pulse stored in the code flash memory are transferred to the general-purpose port pins.
- The vector address is **FFC14H** and control data is allocated at FFCD0H to FFCD7H.
- Transfers 8-byte data at addresses from 02000H to 02007H of the code flash memory from the mirror area (F2000H to F2007H) to port register 1 (FFF01H).
- A repeat mode interrupt is disabled.

Correct:

(omitted)

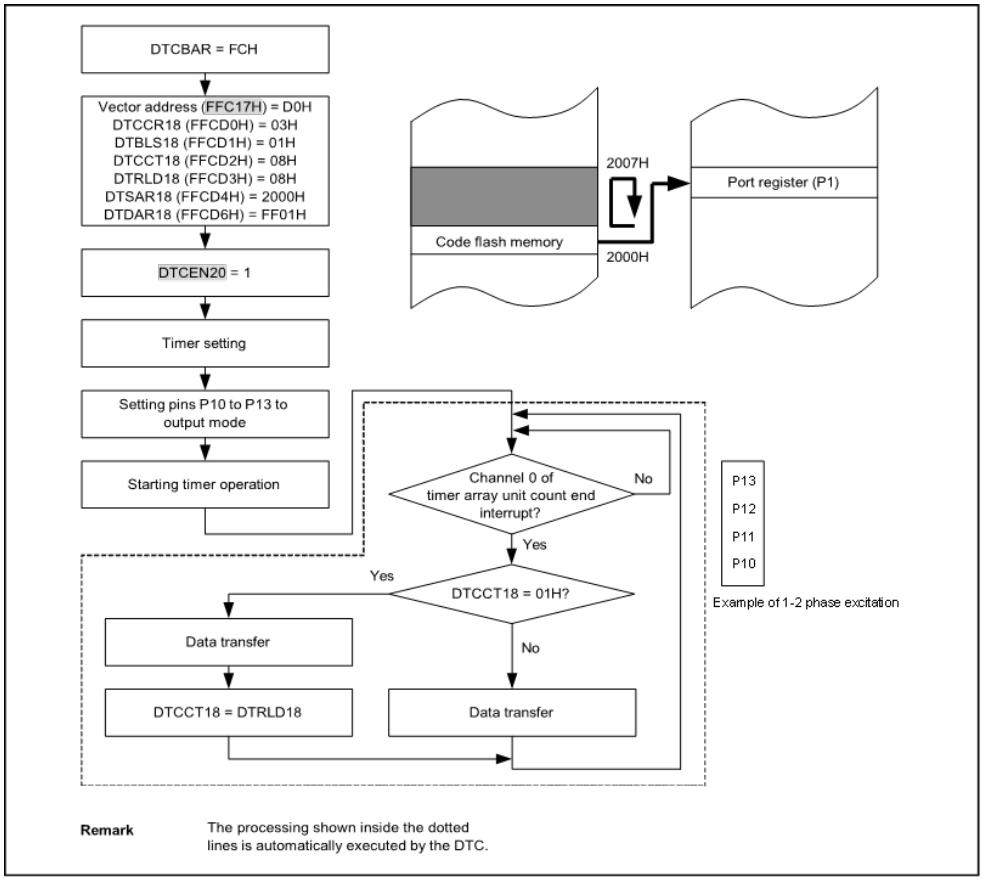
(1) Example 1 of using repeat mode: Outputting stepping motor control pulses using port pins
The DTC is activated using the interval timer function of channel 0 of timer array unit 0, and the patterns of the motor control pulse stored in the code flash memory are transferred to the general-purpose port pins.
- The vector address is FFC17H and control data is allocated at FFCD0H to FFCD7H.
- Transfers 8-byte data at addresses from 02000H to 02007H of the code flash memory from the mirror area (F2000H to F2007H) to port register 1 (FFF01H).
- A repeat mode interrupt is disabled.

Figure 16 - 19 Example 1 of Using Repeat Mode: Outputting Stepping Motor Control Pulses Using Port Pins



To stop the output, stop the timer first and then clear the **DTCEN24** bit.

Figure 16 - 19 Example 1 of Using Repeat Mode: Outputting Stepping Motor Control Pulses Using Port Pins



To stop the output, stop the timer first and then clear the DTCEN20 bit.

14. Table 18 - 2 Flags Corresponding to Interrupt Request Sources (3/4) (Page 847)

Incorrect:

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	48-pin	44-pin	40-pin	36-pin	32-pin	30-pin	25-pin	24-pin	20-pin	16-pin
INTST1	STIF1	IF1L	STMK1	MK1L	STPR01, STPR11	PR01L, PR11L	√	√	√	√	√	√	√	√	√	—
INTSR1 Note 1	SRIF1 Note 1		SRMK1 Note 1		SRPR01, SRPR11 Note 1		√	√	√	√	√	√	√	√	√	—
INTCSI11 Note 1	CSIIF11 Note 1		CSIMK11 Note 1		CSIPR011, CSIPR111 Note 1		√	√	√	√	√	√	√	√	√	—
INTIIC11 Note 1	IICIF11 Note 1		IICMK11 Note 1		IICPR011, IICPR111 Note 1		√	√	√	√	√	√	√	√	√	√
INTSRE1 Note 2	SREIF1 Note 2		SREMK1 Note 2		SREPR01, SREPR11 Note 2		√	√	√	√	√	√	√	√	√	—
INTTM03H Note 2	TMIF03H Note 2		TMMK03H Note 2		TMPR003H,TMPR103H Note 2		√	√	√	√	√	√	√	√	√	√
INTIICA0	IICAIF0		IICAMK0		IICAPR00, IICAPR10		√	√	√	√	√	√	√	√	—	—
INTSR0 Note 3	SRIF0 Note 3		SRMK0 Note 3		SRPR00, SRPR10 Note 3		√	√	√	√	√	√	√	√	√	√
INTCSI01 Note 3	CSIIF01 Note 3		CSIMK01 Note 3		CSIPR001, CSIPR101 Note 3		√	—	—	—	—	—	—	—	—	—
INTIIC01 Note 3	IICIF01 Note 3		IICMK01 Note 3		IICPR001, IICPR101 Note 3		√	—	—	—	—	—	—	—	—	—
INTTM01	TMIF01		TMMK01		TMPR001, TMPR101		√	√	√	√	√	√	√	√	√	√
INTTM02	TMIF02		TMMK02		TMPR002, TMPR102		√	√	√	√	√	√	√	√	√	√
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103		√	√	√	√	√	√	√	√	√	√
INTAD	ADIF	IF1H	ADMK	MK1H	ADPR0, ADPR1	PR01H, PR11H	√	√	√	√	√	√	√	√	√	√
INTRTC	RTCIF		RTCMK		RTCPR0, RTCPR1		√	√	√	√	√	√	√	√	√	√
INTTML	ITLIF		ITLMK		ITLPR0, ITLPR1		√	√	√	√	√	√	√	√	√	√
INTKR	KRIF		KRMK		KRPR0, KRPR1		√	√	√	—	—	—	—	—	—	—
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104		√	√	√	√	√	√	√	√	√	√

Note 1. If any of the interrupt sources INTSR1, INTCSI11, and INTIIC11 is generated, bit 1 of the IF1L register is set to 1. Bit 1 of the MK1L, PR01L, and PR11L registers supports these three interrupt sources.

Note 2. Do not use a UART1 reception error interrupt and an interrupt of channel 3 of TAU0 (at higher 8-bit timer operation) at the same time because they share flags for the interrupt request sources. If the UART1 reception error interrupt is not used (EOC03 = 0), UART1 and channel 3 of TAU0 (at higher 8-bit timer operation) can be used at the same time. If either of the interrupt source INTSRE1 or INTTM03H is generated, bit 2 of the IF1L register is set to 1. Bit 2 of the MK1L, PR01L, and PR11L registers supports these two interrupt sources.

Note 3. If any of the interrupt sources INTSR0, INTCSI01, and INTIIC01 is generated, bit 4 of the IF1L register is set to 1. Bit 4 of the MK1L, PR01L, and PR11L registers supports these three interrupt sources.

Correct:

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	48-pin	44-pin	40-pin	36-pin	32-pin	30-pin	25-pin	24-pin	20-pin	16-pin
INTST1	STIF1	IF1L	STMK1	MK1L	STPR01, STPR11	PR01L, PR11L	√	√	√	√	√	√	√	√	√	—
INTSR1 Note 1	SRIF1 Note 1		SRMK1 Note 1		SRPR01, SRPR11 Note 1		√	√	√	√	√	√	√	√	√	—
INTCSI11 Note 1	CSIIF11 Note 1		CSIMK11 Note 1		CSIPR011, CSIPR111 Note 1		√	√	√	√	√	√	√	√	√	—
INTIIC11 Note 1	IICIF11 Note 1		IICMK11 Note 1		IICPR011, IICPR111 Note 1		√	√	√	√	√	√	√	√	√	√
INTSRE1 Note 2	SREIF1 Note 2		SREMK1 Note 2		SREPR01, SREPR11 Note 2		√	√	√	√	√	√	√	√	√	—
INTTM03H Note 2	TMIF03H Note 2		TMMK03H Note 2		TMPR003H,TMPR103H Note 2		√	√	√	√	√	√	√	√	√	√
INTIICA0	IICAIF0		IICAMK0		IICAPR00, IICAPR10		√	√	√	√	√	√	√	√	—	—
INTSR0 Note 3	SRIF0 Note 3		SRMK0 Note 3		SRPR00, SRPR10 Note 3		√	√	√	√	√	√	√	√	√	√
INTCSI01 Note 3	CSIIF01 Note 3		CSIMK01 Note 3		CSIPR001, CSIPR101 Note 3		√	—	—	—	—	—	—	—	—	—
INTIIC01 Note 3	IICIF01 Note 3		IICMK01 Note 3		IICPR001, IICPR101 Note 3		√	—	—	—	—	—	—	—	—	—
INTTM01	TMIF01		TMMK01		TMPR001, TMPR101		√	√	√	√	√	√	√	√	√	√
INTTM02	TMIF02		TMMK02		TMPR002, TMPR102		√	√	√	√	√	√	√	√	√	√
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103		√	√	√	√	√	√	√	√	√	√
INTAD	ADIF	IF1H	ADMK	MK1H	ADPR0, ADPR1	PR01H, PR11H	√	√	√	√	√	√	√	√	√	√
INTRTC	RTCIF		RTCMK		RTCPR0, RTCPR1		√	√	√	√	√	√	√	√	√	√
INTITL	ITLIF		ITLMK		ITLPR0, ITLPR1		√	√	√	√	√	√	√	√	√	√
INTKR	KRIF		KRMK		KRPR0, KRPR1		√	√	√	—	—	—	—	—	—	—
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104		√	√	√	√	√	√	√	√	√	√

Note 1. If any of the interrupt sources INTSR1, INTCSI11, and INTIIC11 is generated, bit 1 of the IF1L register is set to 1. Bit 1 of the MK1L, PR01L, and PR11L registers supports these three interrupt sources.

Note 2. Do not use a UART1 reception error interrupt and an interrupt of channel 3 of TAU0 (at higher 8-bit timer operation) at the same time because they share flags for the interrupt request sources. If the UART1 reception error interrupt is not used (EOC03 = 0), UART1 and channel 3 of TAU0 (at higher 8-bit timer operation) can be used at the same time. If either of the interrupt source INTSRE1 or INTTM03H is generated, bit 2 of the IF1L register is set to 1. Bit 2 of the MK1L, PR01L, and PR11L registers supports these two interrupt sources.

Note 3. If any of the interrupt sources INTSR0, INTCSI01, and INTIIC01 is generated, bit 4 of the IF1L register is set to 1. Bit 4 of the MK1L, PR01L, and PR11L registers supports these three interrupt sources.

15. 34.2.3 Characteristics of the On-chip Oscillators (Page 1150)

Incorrect:

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f_{IH}				1		32	MHz
High-speed on-chip oscillator clock frequency accuracy Note 1		HIPREC = 1	+85 to +105°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-2.0		+2.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-6.0		+6.0	%
			-20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-5.0		+5.0	%
			-40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
				1.6 V ≤ V_{DD} ~~≤~~ 5.5 V	-5.5		+5.5	%
		HIPREC = 0 ~~Note 4~~			-15		0	%
High-speed on-chip oscillator clock correction resolution						0.05		%
Middle-speed on-chip oscillator clock frequency ~~Note 2~~	f_{IM}				1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy Note 1					-12		+12	%
Middle-speed on-chip oscillator clock correction resolution						0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient							±0.17 ~~Note 3~~	%/°C
Low-speed on-chip oscillator clock frequency ~~Note 2~~	f_{IL}					32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy Note 1					-15		+15	%
Low-speed on-chip oscillator clock correction resolution						0.3		%
Low-speed on-chip oscillator frequency temperature coefficient							±0.21 ~~Note 3~~	%/°C

Note 1. The accuracy values were obtained in testing of this product.

Note 2. The listed values only indicate the characteristics of the oscillators. See 34.4 AC Characteristics for instruction execution time. Note 3. Guaranteed by characterization results.

Note 4. The listed condition applies when the setting of the FRQSEL3 bit is 1.

Correct:

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f_{IH}				1		32	MHz
High-speed on-chip oscillator clock frequency accuracy Note 1		HIPREC = 1	+85 to +105°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-2.0		+2.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-6.0		+6.0	%
			-20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-5.0		+5.0	%
			-40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-5.5		+5.5	%
		HIPREC = 0 Note 2			-15		0	%
High-speed on-chip oscillator clock correction resolution						0.05		%
Middle-speed on-chip oscillator clock frequency Note 3	f_{IM}				1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy Note 1					-12		+12	%
Middle-speed on-chip oscillator clock correction resolution						0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient							±0.17 Note 4	%/°C
Low-speed on-chip oscillator clock frequency Note 3	f_{IL}					32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy Note 1					-15		+15	%
Low-speed on-chip oscillator clock correction resolution						0.3		%
Low-speed on-chip oscillator frequency temperature coefficient							±0.21 Note 4	%/°C

Note 1. The accuracy values were obtained in testing of this product.

Note 2. This condition applies when the setting of the FRQSEL3 bit of the user option byte is 1.

Note 3. The listed values only indicate the characteristics of the oscillators. See 34.4 AC Characteristics for instruction execution time.

Note 4. These values are the results of characteristic evaluation and are not checked for shipment.

16. 34.3.2 Characteristics of the supply current

Incorrect:

(Page 1156)

(TA = -40 to +105℃, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.2		mA
						V_{DD} = 1.8 V		1.2		
					Normal operation	V_{DD} = 5.0 V		2.7	4.6	mA
						V_{DD} = 1.8 V		2.7	4.6	
			LS (low-speed main) mode	f_{MX} = 20 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		1.5	2.7	mA
						V_{DD} = 1.8 V		1.5	2.7	
				f_{MX} = 20 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.7	3.0	mA
						V_{DD} = 1.8 V		1.7	3.0	
				f_{MX} = 10 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.8	1.5	mA
						V_{DD} = 1.8 V		0.8	1.4	
				f_{MX} = 10 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.6	mA
						V_{DD} = 1.8 V		0.9	1.6	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.7	1.2	mA
						V_{DD} = 1.8 V		0.7	1.2	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.8	1.3	mA
						V_{DD} = 1.8 V		0.8	1.3	

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low power main) modes.

- The currents in the "Typ." column do not include the operating currents of the peripheral modules.
- **The currents in the "Max." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

Correct:

(TA = -40 to +105℃, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.2		mA
						V_{DD} = 1.8 V		1.2		
					Normal operation	V_{DD} = 5.0 V		2.7	4.6	mA
						V_{DD} = 1.8 V		2.7	4.6	
			LS (low-speed main) mode	f_{MX} = 20 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		1.5	2.7	mA
						V_{DD} = 1.8 V		1.5	2.7	
				f_{MX} = 20 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.7	3.0	mA
						V_{DD} = 1.8 V		1.7	3.0	
				f_{MX} = 10 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.8	1.5	mA
						V_{DD} = 1.8 V		0.8	1.4	
				f_{MX} = 10 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.6	mA
						V_{DD} = 1.8 V		0.9	1.6	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.7	1.2	mA
						V_{DD} = 1.8 V		0.7	1.2	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.8	1.3	mA
						V_{DD} = 1.8 V		0.8	1.3	

Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low power main) modes.

- The currents in the "Typ." column do not include the operating currents of the peripheral modules.
- The currents in the "Max." column include the operating currents of the PCLBUZ, TAU, SAU, and IICA modules. The operating currents of other peripheral modules are not included.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1159)

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	fIH = 32 MHz Note 3	VDD = 5.0 V		0.49	1.87	mA
					VDD = 1.8 V		0.49	1.87	
			LS (low-speed main) mode	fMX = 20 MHz Note 5, Square wave input	VDD = 5.0 V		0.19	1.03	mA
					VDD = 1.8 V		0.16	0.99	
				fMX = 20 MHz Note 5, Resonator connection	VDD = 5.0 V		0.38	1.26	mA
					VDD = 1.8 V		0.37	1.25	
				fMX = 10 MHz Note 5, Square wave input	VDD = 5.0 V		0.12	0.54	mA
					VDD = 1.8 V		0.10	0.52	
				fMX = 10 MHz Note 5, Resonator connection	VDD = 5.0 V		0.22	0.67	mA
					VDD = 1.8 V		0.22	0.66	
				fMX = 8 MHz Note 5, Square wave input	VDD = 5.0 V		0.10	0.45	mA
					VDD = 1.8 V		0.09	0.43	
				fMX = 8 MHz Note 5, Resonator connection	VDD = 5.0 V		0.20	0.57	mA
					VDD = 1.8 V		0.20	0.56	

Note 1. The listed currents are the total currents flowing into VDD, including the input leakage currents flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (lowpower main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- **The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	fIH = 32 MHz Note 3	VDD = 5.0 V		0.49	1.87	mA
					VDD = 1.8 V		0.49	1.87	
			LS (low-speed main) mode	fMX = 20 MHz Note 5, Square wave input	VDD = 5.0 V		0.19	1.03	mA
					VDD = 1.8 V		0.16	0.99	
				fMX = 20 MHz Note 5, Resonator connection	VDD = 5.0 V		0.38	1.26	mA
					VDD = 1.8 V		0.37	1.25	
				fMX = 10 MHz Note 5, Square wave input	VDD = 5.0 V		0.12	0.54	mA
					VDD = 1.8 V		0.10	0.52	
				fMX = 10 MHz Note 5, Resonator connection	VDD = 5.0 V		0.22	0.67	mA
					VDD = 1.8 V		0.22	0.66	
				fMX = 8 MHz Note 5, Square wave input	VDD = 5.0 V		0.10	0.45	mA
					VDD = 1.8 V		0.09	0.43	
				fMX = 8 MHz Note 5, Resonator connection	VDD = 5.0 V		0.20	0.57	mA
					VDD = 1.8 V		0.20	0.56	

Note 1. The listed currents are the total currents flowing into VDD, including the input leakage currents flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (lowpower main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the PCLBUZ, TAU, SAU, and IICA modules. The operating currents of other peripheral modules are not included.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

17. 34.6.1 Characteristics of the A/D converter for TA = -40 to +85°C (Page 1202)

Incorrect:

(T_A = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V) (2/2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Analog input voltage	V_{AIN}	ANI2 to ANI7	0		AV_{REFP}	V
		Internal reference voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)	V_{BGR} Note 5			V
		Temperature sensor output voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)	V_{TMPS25} Note 5			V
		TSCAP voltage of the CTSU (1.8 V ≤ V_{DD} ≤ 5.5 V)	V_{TSCAP}			V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. **When reference voltage (+) = V_{DD} and reference voltage (–) = V_{SS}, the maximum values are as follows.**

Overall error: Add ±10 LSB to the maximum value when V_{DD} = AV_{REFP}.

Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when V_{DD} = AV_{REFP}.

Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when V_{DD} = AV_{REFP}.

Note 4. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 μs and 95 μs.

Note 5. See 34.6.3 Characteristics of the temperature sensor and internal reference voltage.

Correct:

(T_A = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (-) = AV_{REFM} = 0 V) (2/2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Analog input voltage	V_{AIN}	ANI2 to ANI7	0		AV_{REFP}	V
		Internal reference voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)	V_{BGR} Note 5			V
		Temperature sensor output voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)	V_{TMPS25} Note 5			V
		TSCAP voltage of the CTSU (1.8 V ≤ V_{DD} ≤ 5.5 V)	V_{TSCAP}			V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AV_{REFP} < V_{DD}, the maximum values are as follows.

Overall error: Add ±10 LSB to the maximum value when V_{DD} = AV_{REFP}.

Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when V_{DD} = AV_{REFP}.

Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when V_{DD} = AV_{REFP}.

Note 4. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 μs and 95 μs.

Note 5. See 34.6.3 Characteristics of the temperature sensor and internal reference voltage.

18. 34.6.2 Characteristics of the A/D converter for TA = -40 to +105°C (Page 1208)

Incorrect:

(3) Reference voltage (+) = VDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = VSS (ADREFM = 0), conversion target: ANI0 to ANI7, and ANI16 to ANI19, internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V, reference voltage (+) = VDD, reference voltage (–) = VSS)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	Bit
Overall error Note 1	AINL	10-bit resolution	2.4 V ≤ AVREFP ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution conversion target: ANI0 to ANI7, ANI16 to ANI19	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	µs
		10-bit resolution conversion target: Internal reference voltage, temperature sensor output voltage, and and TSCAP voltage of the CTSU	3.6 V ≤ VDD ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ VDD ≤ 5.5 V	3.5625		39	µs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.4 V ≤ AVREFP ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.4 V ≤ AVREFP ≤ 5.5 V			±2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI7, ANI16 to ANI19		0		VDD	V
		Internal reference voltage		VBGR Note 3			V
		Temperature sensor output voltage		VTMPS25 Note 3			V
		TSCAP voltage of the CTSU		VTSCAP			V

Note 1. This value does not include the quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. See **34.6.3 Characteristics of the temperature sensor and internal reference voltage**.

Correct:

(3) Reference voltage (+) = VDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = VSS (ADREFM = 0), conversion target: ANI0 to ANI7, and ANI16 to ANI19, internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V, reference voltage (+) = VDD, reference voltage (–) = VSS)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	Bit
Overall error Note 1	AINL	10-bit resolution	2.4 V ≤ VDD ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution conversion target: ANI0 to ANI7, ANI16 to ANI19	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	µs
		10-bit resolution conversion target: Internal reference voltage, temperature sensor output voltage, and and TSCAP voltage of the CTSU	3.6 V ≤ VDD ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ VDD ≤ 5.5 V	3.5625		39	µs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI7, ANI16 to ANI19		0		VDD	V
		Internal reference voltage		VBGR Note 3			V
		Temperature sensor output voltage		VTMPS25 Note 3			V
		TSCAP voltage of the CTSU		VTSCAP			V

Note 1. This value does not include the quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. See **34.6.3 Characteristics of the temperature sensor and internal reference voltage**.