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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0093A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G1F Descriptions in the Hardware User's Manual Rev. 1.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G1F Group	Lot No. All lots	Reference Document	RL78/G1F User's Manual: Hardware Rev.1.10 R01UH0516EJ0110 (Aug. 2016)		

This document describes misstatements found in the RL78/G1F User's Manual: Hardware Rev.1.10 (R01UH0516EJ0110).

Corrections

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Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items				Pages in this document for corrections
		Document No.	English	R01UH0516EJ0110	
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Incorrect,OLD: Bold with underline; Correct,NEW: Gray hatched

Revision History

RL78/G1F User's Manual: Hardware Rev.1.10 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A0093A/E	Apr. 3, 2020	First edition issued No.1 to 6 in corrections (This notice)

1. 4.3.5 Port output mode registers (POMxx)
   Figure 4 - 5 Format of Port output mode register (Page 117)

Incorrect:

Figure 4 - 5 Format of Port output mode register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM0	0	0	0	POM04	POM03	POM02	POM01 Note 1	POM00	F0050H	00H	R/W
POM1	POM17	0	POM15	POM14	POM13	0	POM11	POM10	F0051H	00H	R/W
POM3	0	0	0	0	0	0	POM31 Note 2	POM30	F0053H	00H	R/W
POM5	0	0	POM55	0	0	0	POM51	POM50	F0055H	00H	R/W
POM7	0	0	0	POM74	0	POM72 Note 1	POM71	0	F0057H	00H	R/W

POMmn	Pmn pin output mode selection (m = 0, 1, 3, 5, 7; n = 0 to 5, 7)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance[Note 1]/EV_{DD} tolerance[Note 2]) mode

Note 1. For **24-, 32-, and 48-pin** products
Note 2. For **36- and 64-pin** products

(Omitted)

Correct:

Figure 4 - 5 Format of Port output mode register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM0	0	0	0	POM04	POM03	POM02	POM01 Note 1	POM00	F0050H	00H	R/W
POM1	POM17	0	POM15	POM14	POM13	0	POM11	POM10	F0051H	00H	R/W
POM3	0	0	0	0	0	0	POM31 Note 2	POM30	F0053H	00H	R/W
POM5	0	0	POM55	0	0	0	POM51	POM50	F0055H	00H	R/W
POM7	0	0	0	POM74	0	POM72 Note 1	POM71	0	F0057H	00H	R/W

POMmn	Pmn pin output mode selection (m = 0, 1, 3, 5, 7; n = 0 to 5, 7)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance[Note 1]/EV_{DD} tolerance[Note 2]) mode

Note 1. For 24-pin products
Note 2. For 32-pin products

(Omitted)

2. 4.3.7 Peripheral I/O redirection register 0 (PIOR0)
Figure 4 - 7 Format of Peripheral I/O redirection register 0 (PIOR0) (Page 120)

Incorrect:

Figure 4 - 7 Format of Peripheral I/O redirection register 0 (PIOR0)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR0	PIOR07 Note 1	PIOR06 Note 2	PIOR05 Note 3	PIOR04 Note 1	PIOR03 Note 4	PIOR02	PIOR01 Note 5	PIOR00 Note 6

Bit	Function	64-pin		48-pin		36-pin		32-pin		24-pin	
		Setting value		Setting value		Setting value		Setting value		Setting value	
		0	1	0	1	0	1	0	1	0	1
(Omitted)											
PIOR01 Note5	INTP10	P76	P05	P01	P01	P01	P01	P01	P01	This area cannot be used. Be set to 0 (default value).	
	INTP11	P77	P06	P20	P20	P20	P20	P20	P20		
	RxD2	P14	P76	This area cannot be used (controlled in PIOR06). Be set to 0 (default value).							
	TxD2	P13	P77								
	SCL20	P15	—								
	SDA20	P14	—								
	SI20	P14	—								
	SO20	P13	—								
	SCK20	P15	—								
	TxD0	P51	P17	P51	P17	P51	P17	P51	P17		
	RxD0	P50	P16	P50	P16	P50	P16	P50	P16		
	SCL00	P30	—	P30	—	P30	—	P30	—		
	SDA00	P50	—	P50	—	P50	—	P50	—		
	SI00	P50	P16	P50	—	P50	—	P50	—		
	SO00	P51	P17	P51	**P17**	P51	**P17**	P51	**P17**		
	SCK00	P30	P55	P30	**P16**	P30	**P16**	P30	**P16**		
(Omitted)											

Correct:

Figure 4 - 7 Format of Peripheral I/O redirection register 0 (PIOR0)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR0	PIOR07 Note 1	PIOR06 Note 2	PIOR05 Note 3	PIOR04 Note 1	PIOR03 Note 4	PIOR02	PIOR01 Note 5	PIOR00 Note 6

Bit	Function	64-pin		48-pin		36-pin		32-pin		24-pin	
		Setting value		Setting value		Setting value		Setting value		Setting value	
		0	1	0	1	0	1	0	1	0	1
(Omitted)											
PIOR01 Note5	INTP10	P76	P05	P01	P01	P01	P01	P01	P01	This area cannot be used. Be set to 0 (default value).	
	INTP11	P77	P06	P20	P20	P20	P20	P20	P20		
	RxD2	P14	P76	This area cannot be used (controlled in PIOR06). Be set to 0 (default value).							
	TxD2	P13	P77								
	SCL20	P15	—								
	SDA20	P14	—								
	SI20	P14	—								
	SO20	P13	—								
	SCK20	P15	—								
	TxD0	P51	P17	P51	P17	P51	P17	P51	P17		
	RxD0	P50	P16	P50	P16	P50	P16	P50	P16		
	SCL00	P30	—	P30	—	P30	—	P30	—		
	SDA00	P50	—	P50	—	P50	—	P50	—		
	SI00	P50	P16	P50	—	P50	—	P50	—		
	SO00	P51	P17	P51	—	P51	—	P51	—		
	SCK00	P30	P55	P30	—	P30	—	P30	—		
(Omitted)											

3. 4.3.10 Peripheral I/O redirection register 3 (PIOR3)
Figure 4 - 11 Assignment of the redirect function when using UATR2 or IrDA (Page 124)

Incorrect:

<24-pin products>

PIOR06	PIOR30	RxD2 and TxD2 pins of UART2, IrRxD and IrTxD pins of IrDA select
0	0	RxD2/IrRxD is multiplexed with the P14 pin, and TxD2/IrTxD is multiplexed with the P13 pin.
0	1	RxD2 and TxD2 are disabled, IrRxD is multiplexed with the P01 pin, and IrTxD is multiplexed with the P00 pin[Note]
1	0	RxD2 is multiplexed with the P14 pin, TxD2 is multiplexed with the **P13** pin, and IrRxD and IrTxD are disabled.
1	1	Setting prohibited

Note CSI20 and IIC20 are also disabled.

Correct:

<24-pin products>

PIOR06	PIOR30	RxD2 and TxD2 pins of UART2, IrRxD and IrTxD pins of IrDA select
0	0	RxD2/IrRxD is multiplexed with the P14 pin, and TxD2/IrTxD is multiplexed with the P13 pin.
0	1	RxD2 and TxD2 are disabled, IrRxD is multiplexed with the P01 pin, and IrTxD is multiplexed with the P00 pin[Note]
1	0	RxD2 is multiplexed with the P14 pin, TxD2 is multiplexed with the P10 pin, and IrRxD and IrTxD are disabled.
1	1	Setting prohibited

Note CSI20 and IIC20 are also disabled.

4. 4.5.3 Register setting examples for used port and alternate functions
Table 4 - 8 Setting Examples of Registers When Using P00 to P17 Pin Function (64-pin Products) (1/4) (Page 133)

Incorrect:

Table 4 - 8 Setting Examples of Registers When Using P00 to P17 Pin Function (64-pin Products) (1/4)

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU Output Function	Other than SAU
P00	P00	Input	—	x	—	1	x	x	—
		Output	x	0	—	0	0/1	—	(TRJO0) = 0
		Nch OD output		1	—	0	0/1		
	TRGCLKA	Input	—	x	—	1	x	x	—
	(TRJO0)	Output	PIOR13, PIOR12 = 10B	0	—	0	0	—	—
(Omitted)									
P01	P01	Input	—	—	—	1	x	—	—
		Output	x	—	—	0	0/1	—	TRJIO0 = 0
	TRGCLKB	Input	—	—	—	1	x	—	—
	TRJIO0	Input	PIOR11, PIOR10 = 00B	—	—	1	x	—	—
		Output	—	—	—	0	0	—	—
	(INTP10)	Input	PIOR07 = 1	—	—	1	x	—	—
(Omitted)									

Correct:

Table 4 - 8 Setting Examples of Registers When Using P00 to P17 Pin Function (64-pin Products) (1/4)

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU Output Function	Other than SAU
P00	P00	Input	—	x	—	1	x	x	—
		Output	x	0	—	0	0/1	—	(TRJO0) = 0
		Nch OD output		1	—	0	0/1		
	TRGCLKA	Input	—	x	—	1	x	x	—
	TI00	Input	—	x	—	1	x	x	—
	(TRJO0)	Output	PIOR13, PIOR12 = 10B	0	—	0	0	—	—
(Omitted)									
P01	P01	Input	—	—	—	1	x	—	—
		Output	x	—	—	0	0/1	—	TRJIO0 = 0
	TRGCLKB	Input	—	—	—	1	x	—	—
	TO00	Output	x	—	—	0	0	—	—
	TRJIO0	Input	PIOR11, PIOR10 = 00B	—	—	1	x	—	—
		Output	—	—	—	0	0	—	—
	(INTP10)	Input	PIOR07 = 1	—	—	1	x	—	—
(Omitted)									

5. 6.3.7 Timer channel stop register m (TTm)
Figure 6 - 19 Format of Timer channel stop register m (TTm)products (Page 221)

Incorrect:

Figure 6 - 19 Format of Timer channel stop register m (TTm)

Address: F01B4H, F01B5H (TT0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTm	0	0	0	0	TTHm3	0	TTHm1	0	0	0	0	0	TTm3	TTm2	TTm1	TTm0

TTHm3	Trigger to stop operation of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	TEHm3 bit is cleared to 0 and the count operation is stopped.

TTHm1	Trigger to stop operation of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	TEHm1 bit is cleared to 0 and the count operation is stopped.

TTmn	Operation stop trigger of channel n
0	**TEmn bit is cleared to 0 and the count operation is stopped.**
1	**Operation is stopped (stop trigger is generated).** **This bit is the trigger to stop operation of the lower 8-bit timer for TTm1 and TTm3 when channel 1 or 3 is in the 8-bit timer mode.**

Correct:

Figure 6 - 19 Format of Timer channel stop register m (TTm)

Address: F01B4H, F01B5H (TT0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTm	0	0	0	0	TTHm3	0	TTHm1	0	0	0	0	0	TTm3	TTm2	TTm1	TTm0

TTHm3	Trigger to stop operation of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	TEHm3 bit is cleared to 0 and the count operation is stopped.

TTHm1	Trigger to stop operation of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	TEHm1 bit is cleared to 0 and the count operation is stopped.

TTmn	Operation stop trigger of channel n
0	No trigger operation
1	TEmn bit is cleared to 0 and the count operation is stopped. Operation is stopped (stop trigger is generated). This bit is the trigger to stop operation of the lower 8-bit timer for TTm1 and TTm3 when channel 1 or 3 is in the 8-bit timer mode.

6. 19.3.12 Serial output register m (SOm) (Page 677)

Incorrect:

19.3.12 Serial output register m (SOm)

The SOm register is a buffer register for serial output of each channel.

(Omitted)

Reset signal generation clears the SOm register to 0F0FH.

Caution For 32-, 36-, 48-, and 64-pin products, reset signal generation sets the SOm register to 0303H.

Figure 19 - 19 Format of Serial output register m (SOm)

Address: F0128H, F0129H After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO 03	CKO 02	CKO 01	CKO 00	0	0	0	0	SO 03	SO 02	SO 01	SO 00

Address: F0168H, F0169H After reset: **0F0FH** R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	**CKO 13**	**CKO 12**	CKO 11	CKO 10	0	0	0	0	**SO 13**	**SO 12**	SO 11	SO 10

CKO mn	Serial clock output of channel n
0	Serial clock output value is “0”.
1	Serial clock output value is “1”.

SO mn	Serial data output of channel n
0	Serial data output value is “0”.
1	Serial data output value is “1”.

Caution Be sure to clear bits 15 to 12 and 7 to 4 of the SO0 register to “0”.
Be sure to clear bits **15 to 12 and 7 to 4** of the SO1 register to “0”.

Correct:

19.3.12 Serial output register m (SOm)

The SOm register is a buffer register for serial output of each channel.

(Omitted)

Reset signal generation clears the SOm register to 0F0FH.

Figure 19 - 19 Format of Serial output register m (SOm)

Address: F0128H, F0129H After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO 03	CKO 02	CKO 01	CKO 00	0	0	0	0	SO 03	SO 02	SO 01	SO 00

Address: F0168H, F0169H After reset: 0303H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	0	0	CKO 11	CKO 10	0	0	0	0	0	0	SO 11	SO 10

CKO mn	Serial clock output of channel n
0	Serial clock output value is “0”.
1	Serial clock output value is “1”.

SO mn	Serial data output of channel n
0	Serial data output value is “0”.
1	Serial data output value is “1”.

Caution Be sure to clear bits 15 to 12 and 7 to 4 of the SO0 register to “0”.
Be sure to clear bits 15 to 10 and 7 to 2 of the SO1 register to “0”.