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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RL*-A0108A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Correction for Incorrect Description Notice RL78/G1C Descriptions in the User's Manual: Hardware Rev. 1.21 Changed | | Information Category | Technical Notification | | |
| Applicable Product | RL78/G1C Group | Lot No.<br>All lots | Reference Document | RL78/G1C User's Manual: Hardware Rev. 1.21<br>R01UH0348EJ0121 (Dec. 2020) | | |

This document describes misstatements found in the RL78/G1C User's Manual: Hardware Rev. 1.21 (R01UH0348EJ0121).

Corrections

| Applicable Item | Applicable Page | Contents |
|---|---|---|
| 7.3.4 Real-time clock control register 1 (RTCC1) | Page 274 | Incorrect descriptions revised |
| Figure 7-21. Procedure for Reading Real-time Clock | Page 287 | Incorrect descriptions revised |
| Figure 7-22. Procedure for Writing Real-time Clock | Page 288 | Incorrect descriptions revised |
| 30.3.2 Supply current characteristics | Page 918 to Page 921 | Incorrect descriptions revised |
| 31.3.2 Supply current characteristics | Page 978 to Page 981 | Incorrect descriptions revised |

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

| No. | Corrections and Applicable Items | | | Pages in this document for corrections |
|---|---|---|---|---|
| | Document No. | English | R01UH0348EJ0121 | |
| 1 | 7.3.4 Real-time clock control register 1 (RTCC1) | | Page 274 | Page 3 |
| 2 | Figure 7-21. Procedure for Reading Real-time Clock | | Page 287 | Page 4 |
| 3 | Figure 7-22. Procedure for Writing Real-time Clock | | Page 288 | Page 4 |
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| 5 | 31.3.2 Supply current characteristics | | Page 978 to Page 981 | Page 9 to Page 12 |

**Incorrect: Bold with underline**; Correct: Gray hatched

## Revision History

RL78/G1C Correction for incorrect description notice

| Document Number | Issue Date | Description |
|---|---|---|
| TN-RL*-A0108A/E | Jan. 19, 2023 | First edition issued<br>Corrections No.1 to No.5 revised (this document) |

## 1. 7.3.4 Real-time clock control register 1 (RTCC1) (Page 274)

Incorrect:

**Figure 7-5. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)**

| RIFG | Constant-period interrupt status flag |
|---|---|
| 0 | Constant-period interrupt is not generated. |
| 1 | Constant-period interrupt is generated. |
| This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”.<br>This flag is cleared when “0” is written to it. Writing “1” to it is invalid. | |

| RWST | Wait status flag of real-time clock |
|---|---|
| 0 | Counter is operating. |
| 1 | Mode to read or write counter value |
| This status flag indicates whether the setting of the RWAIT bit is valid.<br>Before reading or writing the counter value, confirm that the value of this flag is 1. | |

| RWAIT | Wait control of real-time clock |
|---|---|
| 0 | Sets counter operation. |
| 1 | Stops SEC to YEAR counters. Mode to read or write counter value |
| This bit controls the operation of the counter.<br>Be sure to write “1” to it to read or write the counter value.<br>As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0.<br>When RWAIT = 1, it takes up to one cycle of $f_{RTC}$ until the counter value can be read or written (RWST = 1).Notes 1, 2 When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.<br>However, when it wrote a value to second count register, it will not keep the overflow event. | |

Correct:

**Figure 7-5. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)**

| RIFG | Constant-period interrupt status flag |
|---|---|
| 0 | Constant-period interrupt is not generated. |
| 1 | Constant-period interrupt is generated. |
| This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”.<br>This flag is cleared when “0” is written to it. Writing “1” to it is invalid. | |

| RWST | Wait status flag of real-time clock |
|---|---|
| 0 | Counter is operating. |
| 1 | Mode to read or write counter value |
| This status flag indicates whether the setting of the RWAIT bit is valid.<br>Before reading or writing the counter value, confirm that the value of this flag is 1. | |

| RWAIT | Wait control of real-time clock |
|---|---|
| 0 | Sets counter operation. |
| 1 | Stops SEC to YEAR counters. Mode to read or write counter value |
| This bit controls the operation of the counter.<br>Be sure to write “1” to it to read or write the counter value.<br>As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second).<br>Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.<br>When RWAIT = 1, it takes up to one cycle of $f_{RTC}$ until the counter value can be read or written (RWST = 1).Notes 1, 2 When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.<br>However, when it wrote a value to second count register, it will not keep the overflow event. | |

## 2. Figure 7-21. Procedure for Reading Real-time Clock (Page 287)

Incorrect:

**Note** Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

**Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.**

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence.

All the registers do not have to read and only some registers may be read.

Correct:

**Note** Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

**Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

## 3. Figure 7-22. Procedure for Writing Real-time Clock (Page 288)

Incorrect:

**Note** Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

**Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.**

**2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.**

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence.

All the registers do not have to be set and only some registers may be written.

Correct:

**Note** Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

**Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

**2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.**

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence. All the registers do not have to be set and only some registers may be written.

## 4. 30.3.2 Supply current characteristics (Page 918 to Page 921)

Incorrect:

**30.3.2 Supply current characteristics**

**($T_A$ = −40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (High-speed main) mode Note 6 | $f_{HOCO}$ = 48 MHz<br>$f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 1.7 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.7 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.5 | mA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4<br>$T_A$ = +70°C | Normal operation | Square wave input | | 4.2 | 6.3 | μA |
| | | | | | | Resonator connection | | 4.3 | 6.4 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4<br>$T_A$ = +85°C | Normal operation | Square wave input | | 4.8 | 7.7 | μA |
| | | | | | | Resonator connection | | 4.9 | 7.8 | μA |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

**5.** When Operating frequency setting of option byte = 48 MHz. When $f_{HOCO}$ is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

Correct:

**30.3.2 Supply current characteristics**

**($T_A$ = −40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (High-speed main) mode Note 6 | $f_{HOCO}$ = 48 MHz<br>$f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 1.7 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.7 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.5 | mA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4<br>$T_A$ = +70°C | Normal operation | Square wave input | | 4.2 | 6.3 | μA |
| | | | | | | Resonator connection | | 4.3 | 6.4 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4<br>$T_A$ = +85°C | Normal operation | Square wave input | | 4.8 | 7.7 | μA |
| | | | | | | Resonator connection | | 4.9 | 7.8 | μA |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The following points apply in the HS (high-speed main) mode.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, USB 2.0 host/function module, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**5.** When Operating frequency setting of option byte = 48 MHz. When $f_{HOCO}$ is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (Max. 48 MHz)
**2.** $f_{IH}$: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2,4, or 8 (Max. 24 MHz)
**3.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**4.** $fP_{LL}$: PLL oscillation frequency
**5.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**6.** $f_{CLK}$: CPU/peripheral hardware clock frequency
**7.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**Remarks 1.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (Max. 48 MHz)
**2.** $f_{IH}$: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2,4, or 8 (Max. 24 MHz)
**3.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**4.** $fP_{LL}$: PLL oscillation frequency
**5.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**6.** $f_{CLK}$: CPU/peripheral hardware clock frequency
**7.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

($T_A$ = −40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 9 | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.67 | 1.25 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.67 | 1.25 | mA |
| | | | | $f_{HOCO}$ = 24 MHz Note 7, $f_{IH}$ = 12 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.50 | 0.86 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.50 | 0.86 | mA |
| | | | | $f_{HOCO}$ = 12 MHz Note 7, $f_{IH}$ = 6 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.41 | 0.67 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.41 | 0.67 | mA |
| | | | | $f_{HOCO}$ = 6 MHz Note 7, $f_{IH}$ = 3 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 0.58 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 0.58 | mA |
| | | | HS (High-speed main) mode Note 9 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | HS (High-speed main) mode (PLL operation) Note 9 | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 24 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.91 | 1.52 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.91 | 1.52 | mA |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 12 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.85 | 1.28 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.85 | 1.28 | mA |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 6 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.82 | 1.15 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.82 | 1.15 | mA |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = −40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | μA |
| | | | $T_A$ = +50°C | | | | 0.26 | 1.10 | μA |
| | | | $T_A$ = +70°C | | | | 0.29 | 1.90 | μA |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | μA |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, USB 2.0 host/function module, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

($T_A$ = −40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 8 | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.67 | 1.25 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.67 | 1.25 | mA |
| | | | | $f_{HOCO}$ = 24 MHz Note 6, $f_{IH}$ = 12 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.50 | 0.86 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.50 | 0.86 | mA |
| | | | | $f_{HOCO}$ = 12 MHz Note 6, $f_{IH}$ = 6 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.41 | 0.67 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.41 | 0.67 | mA |
| | | | | $f_{HOCO}$ = 6 MHz Note 6, $f_{IH}$ = 3 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 0.58 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 0.58 | mA |
| | | | HS (High-speed main) mode Note 8 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | HS (High-speed main) mode (PLL operation) Note 8 | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 24 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.91 | 1.52 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.91 | 1.52 | mA |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 12 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.85 | 1.28 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.85 | 1.28 | mA |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 6 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.82 | 1.15 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.82 | 1.15 | mA |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = −40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | μA |
| | | | $T_A$ = +50°C | | | | 0.26 | 1.10 | μA |
| | | | $T_A$ = +70°C | | | | 0.29 | 1.90 | μA |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | μA |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The following points apply in the HS (high-speed main) mode.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, USB 2.0 host/function module, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
7. When Operating frequency setting of option byte = 48 MHz. When $f_{HOCO}$ is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).
8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
9. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (Max. 48 MHz)

2. $f_{IH}$: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2,4, or 8 (Max. 24 MHz)
3. $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
4. $fP_{LL}$: PLL oscillation frequency
5. $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
6. $f_{CLK}$: CPU/peripheral hardware clock frequency
7. Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator and subsystem clock are stopped.
4. When high-speed system clock and subsystem clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
6. When Operating frequency setting of option byte = 48 MHz. When $f_{HOCO}$ is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).
7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
8. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (Max. 48 MHz)

2. $f_{IH}$: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2,4, or 8 (Max. 24 MHz)
3. $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
4. $fP_{LL}$: PLL oscillation frequency
5. $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
6. $f_{CLK}$: CPU/peripheral hardware clock frequency
7. Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

## 5. 31.3.2 Supply current characteristics (Page 978 to Page 981)

Incorrect:

**31.3.2 Supply current characteristics**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (High-speed main) mode Note 6 | $f_{HOCO}$ = 48 MHz<br>$f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 1.7 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.7 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.8 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.8 | mA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4<br>$T_A$ = +85°C | Normal operation | Square wave input | | 4.8 | 7.7 | μA |
| | | | | | | Resonator connection | | 4.9 | 7.8 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4<br>$T_A$ = +105°C | Normal operation | Square wave input | | 6.9 | 19.7 | μA |
| | | | | | | Resonator connection | | 7. 0 | 19.8 | μA |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

**5.** When Operating frequency setting of option byte = 48 MHz. When $f_{HOCO}$ is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

Correct:

**31.3.2 Supply current characteristics**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (High-speed main) mode Note 6 | $f_{HOCO}$ = 48 MHz<br>$f_{IH}$ = 24 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 1.7 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 1.7 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.8 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.8 | mA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4<br>$T_A$ = +85°C | Normal operation | Square wave input | | 4.8 | 7.7 | μA |
| | | | | | | Resonator connection | | 4.9 | 7.8 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4<br>$T_A$ = +105°C | Normal operation | Square wave input | | 6.9 | 19.7 | μA |
| | | | | | | Resonator connection | | 7. 0 | 19.8 | μA |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The following points apply in the HS (high-speed main) mode.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, USB 2.0 host/function module, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

**5.** When Operating frequency setting of option byte = 48 MHz. When $f_{HOCO}$ is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).

**6.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (Max. 48 MHz)
**2.** $f_{IH}$: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2,4, or 8 (Max. 24 MHz)
**3.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**4.** $fP_{LL}$: PLL oscillation frequency
**5.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**6.** $f_{CLK}$: CPU/peripheral hardware clock frequency
**7.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**Remarks 1.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (Max. 48 MHz)
**2.** $f_{IH}$: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2,4, or 8 (Max. 24 MHz)
**3.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
**4.** $fP_{LL}$: PLL oscillation frequency
**5.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
**6.** $f_{CLK}$: CPU/peripheral hardware clock frequency
**7.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

($T_A$ = −40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 9 | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.67 | 2.25 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.67 | 2.25 | mA |
| | | | | $f_{HOCO}$ = 24 MHz Note 7, $f_{IH}$ = 12 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.50 | 1.55 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.50 | 1.55 | mA |
| | | | | $f_{HOCO}$ = 12 MHz Note 7, $f_{IH}$ = 6 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.41 | 1.21 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.41 | 1.21 | mA |
| | | | | $f_{HOCO}$ = 6 MHz Note 7, $f_{IH}$ = 3 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 1.05 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 1.05 | mA |
| | | | HS (High-speed main) mode Note 9 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.90 | mA |
| | | | | | Resonator connection | | 0.45 | 2.00 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.90 | mA |
| | | | | | Resonator connection | | 0.45 | 2.00 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 1.02 | mA |
| | | | | | Resonator connection | | 0.26 | 1.10 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 1.02 | mA |
| | | | | | Resonator connection | | 0.26 | 1.10 | mA |
| | | | HS (High-speed main) mode (PLL operation) Note 9 | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 24 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.91 | 2.74 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.91 | 2.74 | mA |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 12 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.85 | 2.31 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.85 | 2.31 | mA |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 6 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.82 | 2.07 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.82 | 2.07 | mA |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = −40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | μA |
| | | | $T_A$ = +50°C | | | | 0.26 | 1.10 | μA |
| | | | $T_A$ = +70°C | | | | 0.29 | 1.90 | μA |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | μA |
| | | | $T_A$ = +105°C | | | | 2.94 | 15.30 | μA |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, USB 2.0 host/function module, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

($T_A$ = −40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V) (2/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (High-speed main) mode Note 8 | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.67 | 2.25 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.67 | 2.25 | mA |
| | | | | $f_{HOCO}$ = 24 MHz Note 6, $f_{IH}$ = 12 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.50 | 1.55 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.50 | 1.55 | mA |
| | | | | $f_{HOCO}$ = 12 MHz Note 6, $f_{IH}$ = 6 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.41 | 1.21 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.41 | 1.21 | mA |
| | | | | $f_{HOCO}$ = 6 MHz Note 6, $f_{IH}$ = 3 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 1.05 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 1.05 | mA |
| | | | HS (High-speed main) mode Note 8 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.90 | mA |
| | | | | | Resonator connection | | 0.45 | 2.00 | mA |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.90 | mA |
| | | | | | Resonator connection | | 0.45 | 2.00 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 1.02 | mA |
| | | | | | Resonator connection | | 0.26 | 1.10 | mA |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 1.02 | mA |
| | | | | | Resonator connection | | 0.26 | 1.10 | mA |
| | | | HS (High-speed main) mode (PLL operation) Note 8 | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 24 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.91 | 2.74 | mA |
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| | | | | | $V_{DD}$ = 3.0 V | | 0.85 | 2.31 | mA |
| | | | | $f_{PLL}$ = 48 MHz, $f_{CLK}$ = 6 MHz Note 3 | $V_{DD}$ = 5.0 V | | 0.82 | 2.07 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.82 | 2.07 | mA |
| | $I_{DD3}$ | STOP mode Note 7 | $T_A$ = −40°C | | | | 0.18 | 0.50 | μA |
| | | | $T_A$ = +25°C | | | | 0.23 | 0.50 | μA |
| | | | $T_A$ = +50°C | | | | 0.26 | 1.10 | μA |
| | | | $T_A$ = +70°C | | | | 0.29 | 1.90 | μA |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | μA |
| | | | $T_A$ = +105°C | | | | 2.94 | 15.30 | μA |

**Notes 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The following points apply in the HS (high-speed main) mode.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, USB 2.0 host/function module, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
7. When Operating frequency setting of option byte = 48 MHz. When $f_{HOCO}$ is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).
8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
9. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remarks 1.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (Max. 48 MHz)

2. $f_{IH}$: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2,4, or 8 (Max. 24 MHz)
3. $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
4. $fP_{LL}$: PLL oscillation frequency
5. $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
6. $f_{CLK}$: CPU/peripheral hardware clock frequency
7. Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator and subsystem clock are stopped.
4. When high-speed system clock and subsystem clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
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7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
8. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 24 MHz

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**Remarks 1.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (Max. 48 MHz)

2. $f_{IH}$: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2,4, or 8 (Max. 24 MHz)
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5. $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)
6. $f_{CLK}$: CPU/peripheral hardware clock frequency
7. Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C