Date: Dec. 3, 2014

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A041A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G14 Descriptions in the Hardware User's Manual Rev. 3.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G14 R5F104xxx	Lot No. All lots	Reference Document	RL78/G14 User's Manual: Hardware Rev.3.10 R01UH0186EJ0310 (Sep. 2014)		

This document describes misstatements found in the RL78/G14 User's Manual: Hardware Rev.3.10 (R01UH0186EJ0310).

Corrections

Applicable Item	Applicable Page	Contents
1.2 Ordering Information Deletion of R5F104JK and R5F104JL from 52-pin	Page 8	Content change
1.3.7 52-pin products deletion of note2.	Page 19	Content change
1.6 Outline of Functions Deletion of 52-pin information	Pages 48 to 50	Content change
2.1.15 52-pin (Code Flash Memory 96 KB to 512 KB) Deletion of ROM 384KB and 512KB information	Page 84	Content change
Deletion of R5F104JK and R5F104JL information	Pages 131, 132, 136, 137, 138, 143, 148, 193, 958, 981, 1086, 1134 and 1304	Content change
6.3.3 Timer mode register mn Figure 6 - 12 the count clock selection	Page 303	Incorrect descriptions revised
17.3.12 Serial output register m (SOm) Figure 17 - 19 Reset value of serial output register m (SOm)	Page 708	Incorrect descriptions revised
19.5.3 DTC Pending Instruction	Page 982	Incorrect descriptions revised
21.4.4 Interrupt servicing during division instruction	Page 1021	Specifications added
21.4.5 Interrupt request hold	Page 1022	Incorrect descriptions revised
33.2 Operation List	Page 1153	Specifications added

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No. English	R01UH0186EJ0310	
1	1.2 Ordering Information Deletion of R5F104JK and R5F104JL from 52-pin		**Page 8**	**p.3**
2	1.3.7 52-pin products deletion of note2.		**Page 19**	**p.4**
3	1.6 Outline of Functions Deletion of 52-pin information		**Pages 48-50**	**p.5-7**
4	2.1.15 52-pin (Code Flash Memory 96 KB to 512 KB) Deletion of ROM 384KB and 512KB information		**Page 84**	**p.8**
5	Deletion of R5F104JK and R5F104JL information		**Pages 131, 132, 136, 137, 138, 143, 148, 193, 958, 981, 1086, 1134 and 1304**	**p.9-14**
6	6.3.3 Timer mode register mn Figure 6 - 12 the count clock selection		**Page 303**	**p.15**
7	17.3.12 Serial output register m (SOm) Figure 17 - 19 Reset value of serial output register m (SOm)		**Page 708**	**p.16**
8	19.5.3 DTC Pending Instruction		**Page 981**	**p.17**
9	21.4.4 Interrupt servicing during division instruction		**Page 1021**	**p.18**
10	21.4.5 Interrupt request hold		**Page 1022**	**p.19**
11	33.2 Operation List		**Page 1153**	**p.20**

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G14 User's Manual: Hardware Rev.3.10 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A041A/E	Dec. 3, 2014	First edition issued No.1 to 11 in corrections (This notice)

1. 1.2 Ordering Information Deletion of R5F104JK and R5F104JL from 52-pin (page 8)

Incorrect:

Pin count	Package	Fields of Application Note 1	Ordering Part Number
(Omitted)			
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	A	R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEAFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHAFA#V0, R5F104JJAFA#V0 R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEAFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHAFA#X0, R5F104JJAFA#X0 **R5F104JKAFA#30Note2, R5F104JLAFA#30Note2 R5F104JKAFA#50Note2, R5F104JLAFA#50Note2**
		D	R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJDFA#V0 R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJDFA#X0
		G	R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0 R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0 **R5F104JKGFA#30Note2, R5F104JLGFA#30Note2 R5F104JKGFA#50Note2, R5F104JLGFA#50Note2**

(Omitted)

Correct:

Pin count	Package	Fields of Application Note 1	Ordering Part Number
(Omitted)			
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	A	R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEAFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHAFA#V0, R5F104JJAFA#V0 R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEAFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHAFA#X0, R5F104JJAFA#X0
		D	R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJDFA#V0 R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJDFA#X0
		G	R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0 R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0

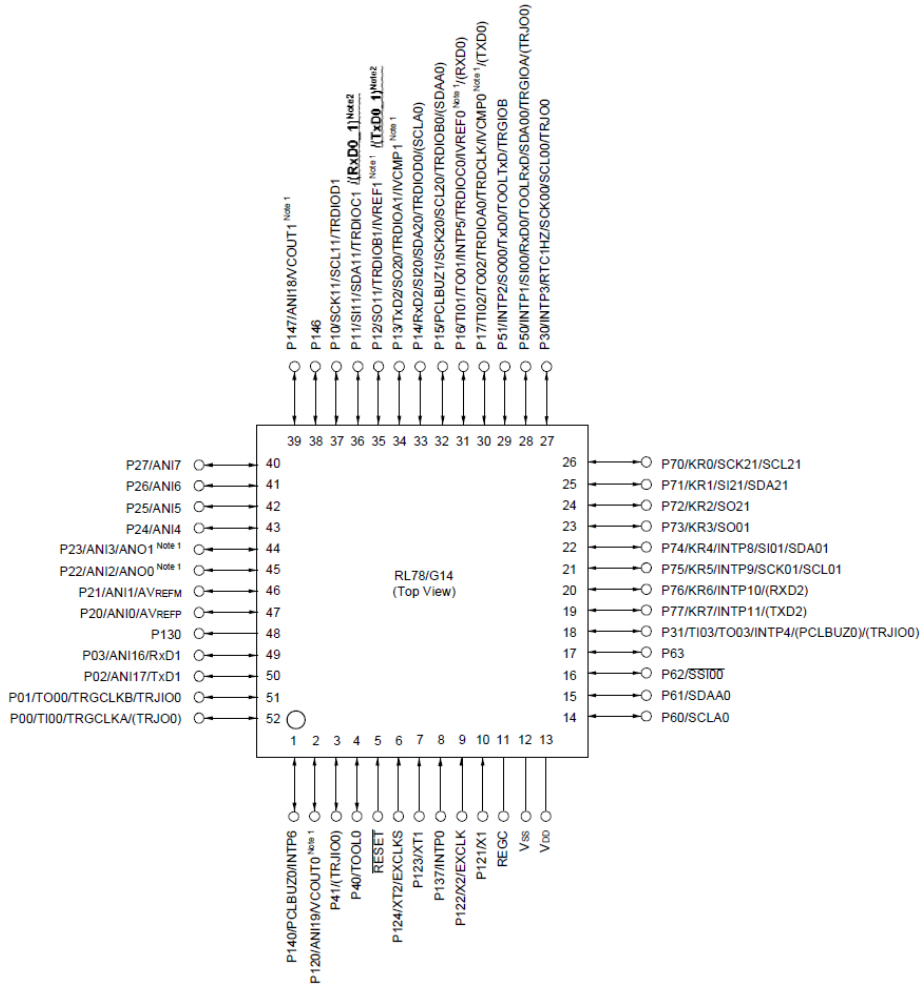
(Omitted)

2. 1.3.7 52-pin products deletion of note2. (page 19)

Incorrect:

1.3.7 52-pin products

• 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



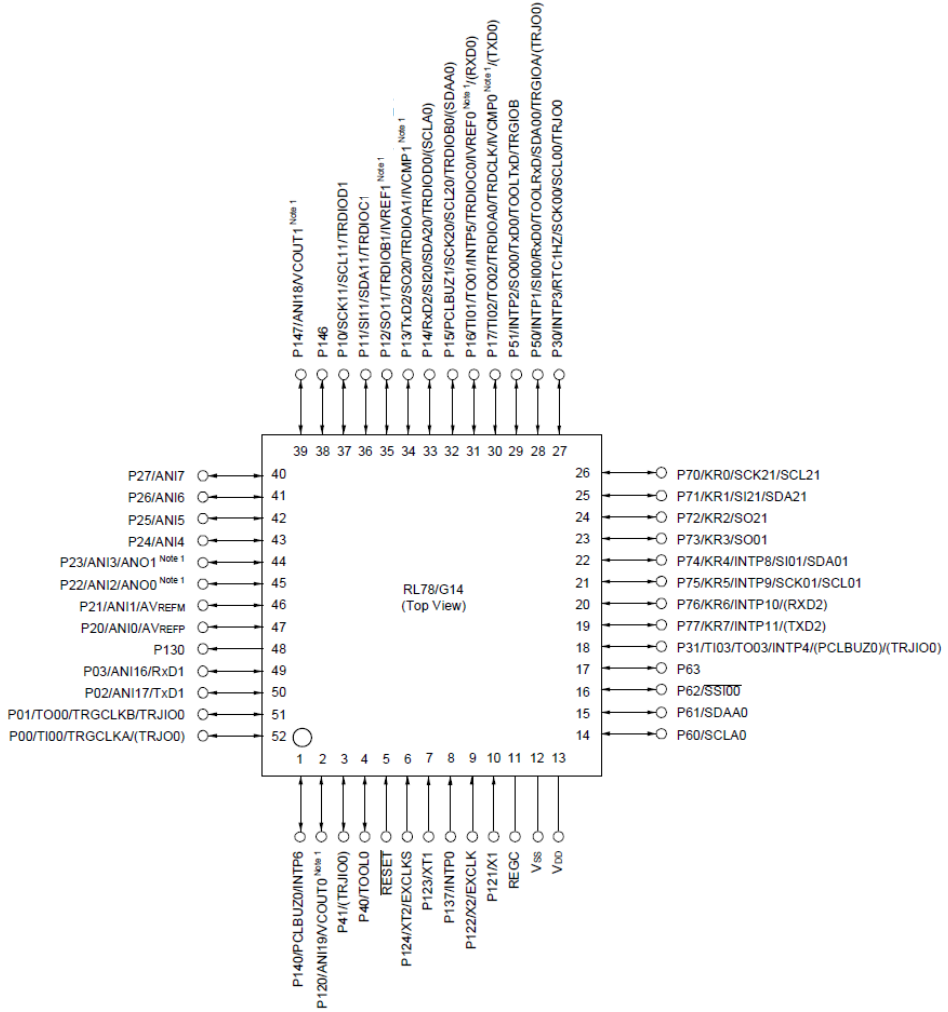
Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Correct:

1.3.7 52-pin products

• 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

3. 1.6 Outline of Functions
Deletion of 52-pin information (Pages 48 to 50)

Incorrect:

[48-pin, **52-pin,** 64-pin products (code flash memory 384 KB to **512 KB**)]
Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1(PIOR0, 1) are set to 00H.

(1/2)

Item		48-pin R5F104Gx (x = K, L)	**52-pin R5F104Jx (x = K, L)**	64-pin R5F104Lx (x = K, L)
Code flash memory (KB)		384 to 512	**384 to 512**	384 to 512
Data flash memory (KB)		8	**8**	8
RAM (KB)		32 to 48 Note	**32 to 48 Note**	32 to 48 Note
Address space		1 MB		
(Omitted)				
I/O port	Total	44	**48**	58
	CMOS I/O	34	**38**	48
	CMOS input	5	**5**	5
	CMOS output	1	**1**	1
	N-ch open-drain I/O (6 V tolerance)	4	**4**	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)		
	Watchdog timer	1 channel		
	Real-time clock(RTC)	1 channel		
	12-bit interval timer	1 channel		
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels		
	RTC output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)		

(**Note** is listed on the next page.)

Correct:

[48-pin, 64-pin products (code flash memory 384 KB to 256 KB)]
Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1(PIOR0, 1) are set to 00H.

(1/2)

Item		48-pin R5F104Gx (x = K, L)	64-pin R5F104Lx (x = K, L)
Code flash memory (KB)		384 to 512	384 to 512
Data flash memory (KB)		8	8
RAM (KB)		32 to 48 Note	32 to 48 Note
Address space		1 MB	
(Omitted)			
I/O port	Total	44	58
	CMOS I/O	34	48
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock(RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels	
	RTC output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	

(**Note** is listed on the next page.)

Incorrect:

Note The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xL (x = G, J, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).

Correct:

Note The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).

Incorrect:

(2/2)

Item		48-pin R5F104Gx (x = K, L)	52-pin R5F104Jx (x = K, L)	64-pin R5F104Lx (x = K, L)
Clock output/buzzer output		2	2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: fMAIN = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: fSUB = 32.768 kHz operation)		
8/10-bit resolution A/D converter		10 channels	12 channels	12 channels
D/A converter		2 channels		
Comparator		2 channels		
Serial interface		[48-pin, 52-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I2C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I2C: 2 channels [64-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I2C: 2 channels		
	I^2C bus	1 channel	1 channel	1 channel
Data transfer controller (DTC)		32 sources		33 sources
Event link controller (ELC)		Event input: 22 Event trigger output: 9		
Vectored interrupt sources	Internal	24	24	24
	External	10	12	13
Key interrupt		6	8	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access		
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V		
Voltage detector		1.63 V to 4.06 V (14 stages)		
On-chip debug function		Provided		
Power supply voltage		V_{DD} = 1.6 to 5.5 V		
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)		

(Omitted)

Correct:

(2/2)

Item		48-pin R5F104Gx (x = K, L)	64-pin R5F104Lx (x = K, L)
Clock output/buzzer output		2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: fMAIN = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: fSUB = 32.768 kHz operation)	
8/10-bit resolution A/D converter		10 channels	12 channels
D/A converter		2 channels	
Comparator		2 channels	
Serial interface		[48-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I2C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I2C: 2 channels [64-pin products] • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I2C: 2 channels	
	I^2C bus	1 channel	1 channel
Data transfer controller (DTC)		32 sources	33 sources
Event link controller (ELC)		Event input: 22 Event trigger output: 9	
Vectored interrupt sources	Internal	24	24
	External	10	13
Key interrupt		6	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V	
Voltage detector		1.63 V to 4.06 V (14 stages)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.6 to 5.5 V	
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T_A = -40 to +105°C (G: Industrial applications)	

(Omitted)

4. 2.1.15 52-pin (Code Flash Memory 96 KB to 512 KB) Deletion of ROM 384KB and 512KB information (Page 84)

Incorrect:

2.1.15 52-pin (Code Flash Memory 96 KB to **512 KB**)

(1/2)

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-1-8	I/O	Input port	SCK11/SCL11/TRDIOD1	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. (Omitted)
P11	7-1-8			SI11/SDA11/TRDIOC1/**(RxD0_1)**Note3	
P12	7-6-6			SO11/TRDIOB1/IVREF1/(INTP5)/**(TxD0_1)**Note3	
(Omitted)					

Note 1. Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
Note 2. Each pin can be specified as either digital or analog by setting the A/D port configuration register (ADPC).
Note 3. Mounted on the 384 KB or more code flash memory products.

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0, 1(PIOR0, 1).

Correct:

2.1.15 52-pin (Code Flash Memory 96 KB to 256 KB)

(1/2)

	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-1-8	I/O	Input port	SCK11/SCL11/TRDIOD1	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. (Omitted)
P11	7-1-8			SI11/SDA11/TRDIOC1	
P12	7-6-6			SO11/TRDIOB1/IVREF1/(INTP5)	
(Omitted)					

Note 1. Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
Note 2. Each pin can be specified as either digital or analog by setting the A/D port configuration register (ADPC).

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0, 1(PIOR0, 1).

5. Deletion of R5F104JK and R5F104JL information)
(the corresponding page is indicated below.)

3.1 Memory Space (Page 131)

Incorrect:

Figure 3 - 9 Memory Map **(R5F104xK (x = G, J, L, M, P))**

3.1 Memory Space (Page 132)

Incorrect:

Figure 3 - 10 Memory Map **(R5F104xL (x = G, J, L, M, P))**

Remark of Correspondence Between Address Values and Block Numbers in Flash Memory (Page 136)

Incorrect:

Table 3 - 3 Correspondence Between Address Values and Block Numbers in Flash Memory (3/4)

(Omitted)

Remark **R5F104xK (x = G, J, L, M, P)**: Block numbers 00H to 17FH

Remark of Correspondence Between Address Values and Block Numbers in Flash Memory (Page 137)

Incorrect:

Table 3 - 4 Correspondence Between Address Values and Block Numbers in Flash Memory (4/4)

(Omitted)

Remark **R5F104xL (x = G, J, L, M, P)**: Block numbers 00H to 1FFH

3.1 Memory Space (Page 131)

Correct:

Figure 3 - 9 Memory Map (R5F104xK (x = G, L, M, P))

3.1 Memory Space (Page 132)

Correct:

Figure 3 - 10 Memory Map (R5F104xL (x = G, L, M, P))

Remark of Correspondence Between Address Values and Block Numbers in Flash Memory (Page 136)

Correct:

Table 3 - 3 Correspondence Between Address Values and Block Numbers in Flash Memory (3/4)

(Omitted)

Remark R5F104xK (x = G, L, M, P): Block numbers 00H to 17FH

Remark of Correspondence Between Address Values and Block Numbers in Flash Memory (Page 137)

Correct:

Table 3 - 4 Correspondence Between Address Values and Block Numbers in Flash Memory (4/4)

(Omitted)

Remark R5F104xL (x = G, L, M, P): Block numbers 00H to 1FFH

3.1.1 Internal program memory space (page 138)

Incorrect:

Table 3 - 5 Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
R5F104xA (x = A to C, E to G)	Flash memory	16384 × 8bits(00000H to 03FFFH)
R5F104xC (x = A to C, E to G, J, L)		32768 × 8bits(00000H to 07FFFH)
R5F104xD (x = A to C, E to G, J, L)		49152 × 8bits(00000H to 0BFFFH)
R5F104xE (x = A to C, E to G, J, L)		65536 × 8bits(00000H to 0FFFFH)
R5F104xF (x = A to C, E to G, J, L, M, P)		98304 × 8bits(00000H to 17FFFH)
R5F104xG (x = A to C, E to G, J, L, M, P)		131072 × 8bits(00000H to 1FFFFH)
R5F104xH (x = E to G, J, L, M, P)		196608 × 8bits(00000H to 2FFFFH)
R5F104xJ (x = F, G ,J , L, M, P)		262144 × 8bits(00000H to 3FFFFH)
R5F104xK (x = G, J, L, M, P)		393216 × 8bits(00000H to 5FFFFH)
R5F104xL (x = G, J, L, M, P)		524288 × 8bits(00000H to 7FFFFH)

(Omitted)

3.1.3 Internal data memory space (page 143)

Incorrect:

Table 3 - 8 Internal RAM Capacity

Part Number	Internal RAM
R5F104xA (x = A to C, E to G)	2560 × 8bits(FF500H to FFEFFH)
R5F104xC (x = A to C, E to G, J, L)	4096 × 8bits(FEF00H to FFEFFH)
R5F104xD (x = A to C, E to G, J, L)	5632 × 8bits(FE900H to FFEFFH)
R5F104xE (x = A to C, E to G, J, L)	
R5F104xF (x = A to C, E to G, J, L, M, P)	12288 × 8bits(FCF00H to FFEFFH)
R5F104xG (x = A to C, E to G, J, L, M, P)	16384 × 8bits(FBF00H to FFEFFH)
R5F104xH (x = E to G, J, L, M, P)	20480 × 8bits(FAF00H to FFEFFH)
R5F104xJ (x = F, G ,J , L, M, P)	24576 × 8bits(F9F00H to FFEFFH)
R5F104xK (x = G, J, L, M, P)	32768 × 8bits(F7F00H to FFEFFH)
R5F104xL (x = G, J, L, M, P)	49152 × 8bits(F3F00H to FFEFFH)

(Omitted)

3.1.1 Internal program memory space (page 138)

Correct:

Table 3 - 5 Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
R5F104xA (x = A to C, E to G)	Flash memory	16384 × 8bits(00000H to 03FFFH)
R5F104xC (x = A to C, E to G, J, L)		32768 × 8bits(00000H to 07FFFH)
R5F104xD (x = A to C, E to G, J, L)		49152 × 8bits(00000H to 0BFFFH)
R5F104xE (x = A to C, E to G, J, L)		65536 × 8bits(00000H to 0FFFFH)
R5F104xF (x = A to C, E to G, J, L, M, P)		98304 × 8bits(00000H to 17FFFH)
R5F104xG (x = A to C, E to G, J, L, M, P)		131072 × 8bits(00000H to 1FFFFH)
R5F104xH (x = E to G, J, L, M, P)		196608 × 8bits(00000H to 2FFFFH)
R5F104xJ (x = F, G ,J , L, M, P)		262144 × 8bits(00000H to 3FFFFH)
R5F104xK (x = G, L, M, P)		393216 × 8bits(00000H to 5FFFFH)
R5F104xL (x = G, L, M, P)		524288 × 8bits(00000H to 7FFFFH)

(Omitted)

3.1.3 Internal data memory space (page 143)

Correct:

Table 3 - 8 Internal RAM Capacity

Part Number	Internal RAM
R5F104xA (x = A to C, E to G)	2560 × 8bits(FF500H to FFEFFH)
R5F104xC (x = A to C, E to G, J, L)	4096 × 8bits(FEF00H to FFEFFH)
R5F104xD (x = A to C, E to G, J, L)	5632 × 8bits(FE900H to FFEFFH)
R5F104xE (x = A to C, E to G, J, L)	
R5F104xF (x = A to C, E to G, J, L, M, P)	12288 × 8bits(FCF00H to FFEFFH)
R5F104xG (x = A to C, E to G, J, L, M, P)	16384 × 8bits(FBF00H to FFEFFH)
R5F104xH (x = E to G, J, L, M, P)	20480 × 8bits(FAF00H to FFEFFH)
R5F104xJ (x = F, G ,J , L, M, P)	24576 × 8bits(F9F00H to FFEFFH)
R5F104xK (x = G, L, M, P)	32768 × 8bits(F7F00H to FFEFFH)
R5F104xL (x = G, L, M, P)	49152 × 8bits(F3F00H to FFEFFH)

(Omitted)

3.2.1 Control registers (page 148)

Incorrect:

(Omitted)

Caution 4. The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
R5F104xL (x = G, J, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).

Caution 5. The internal RAM area in the following products cannot be used as stack memory when using the on-chip debugging trace function.

R5F104xJ (x = A to C, E to G, J, L): FA300H to FA6FFH
R5F104xL (x = G, J, L, M, P): F4300H to F46FFH

4.3 Registers Controlling Port Function (page 193)

Incorrect:

(Omitted)

Note 1. 30-pin and 32-pin products only.
Note 2. R5F104xF (x = A to C, E to G, J, L, M, P), R5F104xG (x = A to C, E to G, J, L, M, P), R5F104xH (x = E to G, J, L, M,P), R5F104xJ (x = F, G, J, L, M, P), **R5F104xK (x = G, J, L, M, P), R5F104xL (x = G, J, L, M, P)** only.

3.2.1 Control registers (page 148)

Correct:

(Omitted)

Caution 4. The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).

Caution 5. The internal RAM area in the following products cannot be used as stack memory when using the on-chip debugging trace function.

R5F104xJ (x = A to C, E to G, J, L): FA300H to FA6FFH
R5F104xL (x = G, L, M, P): F4300H to F46FFH

4.3 Registers Controlling Port Function (page 193)

Correct:

(Omitted)

Note 1. 30-pin and 32-pin products only.
Note 2. R5F104xF (x = A to C, E to G, J, L, M, P), R5F104xG (x = A to C, E to G, J, L, M, P), R5F104xH (x = E to G, J, L, M,P), R5F104xJ (x = F, G, J, L, M, P), R5F104xK (x = G, L, M, P), R5F104xL (x = G, L, M, P) only.

19.3.1 Allocation of DTC Control Data Area and DTC Vector Table Area (Page 958)

Incorrect:

(Omitted)

Caution 3. The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the self-programming and data-flash functions.

R5F104xD (x = A to C, E to G, J, L):	FE900H to FED09H
R5F104xE (x = A to C, E to G, J, L):	FE900H to FED09H
R5F104xJ (x = A to C, E to G, J, L):	F9F00H to FA309H
R5F104xL (x = G, J, L, M, P):	F3F00H to F4309H

Caution 4. The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the on-chip debugging trace function.

R5F104xJ (x = A to C, E to G, J, L):	FA300H to FA6FFH
R5F104xL (x = G, J, L, M, P):	F4300H to F46FFH

19.3.1 Allocation of DTC Control Data Area and DTC Vector Table Area (Page 958)

Correct:

(Omitted)

Caution 3. The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the self-programming and data-flash functions.

R5F104xD (x = A to C, E to G, J, L):	FE900H to FED09H
R5F104xE (x = A to C, E to G, J, L):	FE900H to FED09H
R5F104xJ (x = A to C, E to G, J, L):	F9F00H to FA309H
R5F104xL (x = G, L, M, P):	F3F00H to F4309H

Caution 4. The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the on-chip debugging trace function.

R5F104xJ (x = A to C, E to G, J, L):	FA300H to FA6FFH
R5F104xL (x = G, L, M, P):	F4300H to F46FFH

19.5.2 Allocation of DTC Control Data Area and DTC Vector Table Area (Page 981)

Incorrect:

(Omitted)

- The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the self-programming and data-flash functions.

R5F104xD (x = A to C, E to G, J, L):	FE900H to FED09H
R5F104xE (x = A to C, E to G, J, L):	FE900H to FED09H
R5F104xJ (x = A to C, E to G, J, L):	F9F00H to FA309H
R5F104xL (x = G, J, L, M, P):	F3F00H to F4309H

- The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the on-chip debugging trace function.

R5F104xJ (x = A to C, E to G, J, L):	FA300H to FA6FFH
R5F104xL (x = G, J, L, M, P):	F4300H to F46FFH

- Initialize the DTRLD register to 00H even in normal mode when parity error resets are enabled (RPERDIS = 0) using the RAM parity error detection function.

19.5.2 Allocation of DTC Control Data Area and DTC Vector Table Area (Page 981)

Correct:

(Omitted)

- The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the self-programming and data-flash functions.

R5F104xD (x = A to C, E to G, J, L):	FE900H to FED09H
R5F104xE (x = A to C, E to G, J, L):	FE900H to FED09H
R5F104xJ (x = A to C, E to G, J, L):	F9F00H to FA309H
R5F104xL (x = G, L, M, P):	F3F00H to F4309H

- The internal RAM area in the following products cannot be used as the DTC control data area or DTC vector table area when using the on-chip debugging trace function.

R5F104xJ (x = A to C, E to G, J, L):	FA300H to FA6FFH
R5F104xL (x = G, L, M, P):	F4300H to F46FFH

- Initialize the DTRLD register to 00H even in normal mode when parity error resets are enabled (RPERDIS = 0) using the RAM parity error detection function.

27.3.6 Invalid memory access detection function (Page 1086)

Incorrect:

(Omitted)

Note The code flash memory, RAM, and lowest detection address of each product are as follows.

Products	Code Flash Memory (00000H to xxxxxH)	RAM (zzzzzH to FFEFFH)	Lowest Detection Address (yyyyyH) when Reading/Fetching (Executing) Instructions
R5F104xA(x=A to C, E to G)	16384 × 8 bits (00000H to 03FFFH)	2560 × 8 bit (FF500H to FFEFFH)	10000H
R5F104xC(x=A to C,E to G,J,L)	32768 × 8 bits (00000H to 07FFFH)	4096 × 8 bit (FEF00H to FFEFFH)	10000H
R5F104xD(x=A to C,E to G,J,L)	49152 × 8 bits (00000H to 0BFFFH)	5632 × 8 bit (FE900H to FFEFFH)	10000H
R5F104xE(x=A to C,E to G,J,L)	65536 × 8 bits (00000H to 0FFFFH)	5632 × 8 bit (FE900H to FFEFFH)	10000H
R5F104xF (x=A to C,E to G,J,L,M,P)	98304 × 8 bits (00000H to 17FFFH)	12288 × 8 bit (FCF00H to FFEFFH)	20000H
R5F104xG (x=A to C,E to G,J,L,M,P)	131072 × 8 bits (00000H to 1FFFFH)	16384 × 8 bit (FBF00H to FFEFFH)	20000H
R5F104xH(x=E to G,J,L,M,P)	196608 × 8 bits (00000H to 2FFFFH)	20480 × 8 bit (FAF00H to FFEFFH)	30000H
R5F104xJ(x=F,G,J,L,M,P)	262144 × 8 bits (00000H to 3FFFFH)	24576 × 8 bit (F9F00H to FFEFFH)	40000H
R5F104xK(x=G,J,L,M,P)	393216 × 8 bits (00000H to 5FFFFH)	32768 × 8 bit (F7F00H to FFEFFH)	60000H
R5F104xL(x=G,J,L,M,P)	524688 × 8 bits (00000H to 7FFFFH)	49152 × 8 bit (F3F00H to FFEFFH)	80000H

27.3.6 Invalid memory access detection function (Page 1086)

Correct:

(Omitted)

Note The code flash memory, RAM, and lowest detection address of each product are as follows.

Products	Code Flash Memory (00000H to xxxxxH)	RAM (zzzzzH to FFEFFH)	Lowest Detection Address (yyyyyH) when Reading/Fetching (Executing) Instructions
R5F104xA(x=A to C, E to G)	16384 × 8 bits (00000H to 03FFFH)	2560 × 8 bits (FF500H to FFEFFH)	10000H
R5F104xC(x=A to C,E to G,J,L)	32768 × 8 bits (00000H to 07FFFH)	4096 × 8 bits (FEF00H to FFEFFH)	10000H
R5F104xD(x=A to C,E to G,J,L)	49152 × 8 bits (00000H to 0BFFFH)	5632 × 8 bits (FE900H to FFEFFH)	10000H
R5F104xE(x=A to C,E to G,J,L)	65536 × 8 bits (00000H to 0FFFFH)	5632 × 8 bits (FE900H to FFEFFH)	10000H
R5F104xF (x=A to C,E to G,J,L,M,P)	98304 × 8 bits (00000H to 17FFFH)	12288 × 8 bits (FCF00H to FFEFFH)	20000H
R5F104xG (x=A to C,E to G,J,L,M,P)	131072 × 8 bits (00000H to 1FFFFH)	16384 × 8 bits (FBF00H to FFEFFH)	20000H
R5F104xH(x=E to G,J,L,M,P)	196608 × 8 bits (00000H to 2FFFFH)	20480 × 8 bits (FAF00H to FFEFFH)	30000H
R5F104xJ(x=F,G,J,L,M,P)	262144 × 8 bits (00000H to 3FFFFH)	24576 × 8 bits (F9F00H to FFEFFH)	40000H
R5F104xK(x=G,L,M,P)	393216 × 8 bits (00000H to 5FFFFH)	32768 × 8 bits (F7F00H to FFEFFH)	60000H
R5F104xL(x=G,L,M,P)	524688 × 8 bits (00000H to 7FFFFH)	49152 × 8 bits (F3F00H to FFEFFH)	80000H

31.3 Securing of User Resources (Page 1134)

Incorrect:

(Omitted)

Note 1. Address differs depending on products as follows.

Products (code flash memory capacity)	Address of Note 1.
R5F104xA (x = A to C, E to G)	03FFFH
R5F104xC (x = A to C, E to G, J, L)	07FFFH
R5F104xD (x = A to C, E to G, J, L)	0BFFFH
R5F104xE (x = A to C, E to G, J, L)	0FFFFH
R5F104xF (x = A to C, E to G, J, L, M, P)	17FFFH
R5F104xG (x = A to C, E to G, J, L, M, P)	1FFFFH
R5F104xH (x = E to G, J, L, M, P)	2FFFFH
R5F104xJ (x = F, G ,J , L, M, P)	3FFFFH
R5F104xK (x = G, J, L, M, P)	5FFFFH
R5F104xL (x = G, J, L, M, P)	7FFFFH

(Omitted)

36.7 52-pin products (Page 1304)

Incorrect:

R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA,
R5F104JHAFA, R5F104JJAFA
R5F104JCDFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA,
R5F104JHDFA, R5F104JJDFA
R5F104JCGFA, R5F104JDGFA, R5F104JEGFA, R5F104JFGFA, R5F104JGGFA,
R5F104JHGFA, R5F104JJGFA
R5F104GKGNA, R5F104GLGNA
R5F104JKGFA, R5F104JLGFA

(Omitted)

31.3 Securing of User Resources (Page 1134)

Correct:

(Omitted)

Note 1. Address differs depending on products as follows.

Products (code flash memory capacity)	Address of Note 1.
R5F104xA (x = A to C, E to G)	03FFFH
R5F104xC (x = A to C, E to G, J, L)	07FFFH
R5F104xD (x = A to C, E to G, J, L)	0BFFFH
R5F104xE (x = A to C, E to G, J, L)	0FFFFH
R5F104xF (x = A to C, E to G, J, L, M, P)	17FFFH
R5F104xG (x = A to C, E to G, J, L, M, P)	1FFFFH
R5F104xH (x = E to G, J, L, M, P)	2FFFFH
R5F104xJ (x = F, G ,J , L, M, P)	3FFFFH
R5F104xK (x = G, L, M, P)	5FFFFH
R5F104xL (x = G, L, M, P)	7FFFFH

(Omitted)

36.7 52-pin products (Page 1304)

Correct:

R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA,
R5F104JHAFA, R5F104JJAFA
R5F104JCDFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA,
R5F104JHDFA, R5F104JJDFA
R5F104JCGFA, R5F104JDGFA, R5F104JEGFA, R5F104JFGFA, R5F104JGGFA,
R5F104JHGFA, R5F104JJGFA

(Omitted)

6. 6.3.3 Timer mode register mn (TMRmn) Figure 6 - 12 the count clock selection (Page 303)

Incorrect:

Figure 6 - 12 Format of Timer mode register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) to F0196H, F0197H (TMR03), After reset: 0000H R/W
F01D0H, F01D1H (TMR10) to F01D6H, F01D7H (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n=2)	CKS mn1	CKS mn0	0	CCS mn	MAS TERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

(Omitted)

CCS mn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin
Count clock (f_{TCLK}) is used for the counter, output controller, and interrupt controller.	

(Omitted)

Correct:

Figure 6 - 12 Format of Timer mode register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) to F0196H, F0197H (TMR03), After reset: 0000H R/W
F01D0H, F01D1H (TMR10) to F01D6H, F01D7H (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n=2)	CKS mn1	CKS mn0	0	CCS mn	MAS TERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

(Omitted)

CCS mn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin When using unit 0: In channel 0, Valid edge of input signal selected by TIS0 In channel 1, Valid edge of input signal selected by TIS0 In channel 3, Valid edge of input signal selected by ISC
Count clock (f_{TCLK}) is used for the counter, output controller, and interrupt controller.	

(Omitted)

7. 17.3.12 Serial output register m (SOm) Figure 17 - 19 Reset value of serial output register m (SOm) (Page 708)

Incorrect:

Figure 17 - 19 Format of Serial output register m (SOm)

Address: F0128H, F0129H After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO 03	CKO 02	CKO 01	CKO 00	0	0	0	0	SO 03	SO 02	SO 01	SO 00

Address: F0168H, F0169H After reset: 0F0FH Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	CKO 13	CKO 12	CKO 11	CKO 10	0	0	0	0	SO 13	SO 12	SO 11	SO 10

(Omitted)

Note The register value becomes **3030H** after a reset for the 30 to 64-pin products.

(Omitted)

Correct:

Figure 17 - 19 Format of Serial output register m (SOm)

Address: F0128H, F0129H After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO 03	CKO 02	CKO 01	CKO 00	0	0	0	0	SO 03	SO 02	SO 01	SO 00

Address: F0168H, F0169H After reset: 0F0FH Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	CKO 13	CKO 12	CKO 11	CKO 10	0	0	0	0	SO 13	SO 12	SO 11	SO 10

(Omitted)

Note The register value becomes 0303H after a reset for the 30 to 64-pin products.

(Omitted)

8. 19.5.3 DTC Pending Instruction (Page 982)

Incorrect:

(Omitted)

Even if a DTC transfer request is generated, DTC transfer is held pending immediately after the following instructions. Also, the DTC is not activated between PREFIX instruction code and the instruction immediately after that code.

- Call/return instruction
- Unconditional branch instruction
- Conditional branch instruction
- Read access instruction for code flash memory
- Bit manipulation instructions for IFxx, MKxx, PRxx, and PSW, and an 8-bit manipulation instruction that has the ES register as operand
- Instruction for accessing the data flash memory

Caution 1. When a DTC transfer request is acknowledged, all interrupt requests are held pending until DTC transfer is completed.
Caution 2. While the DTC is held pending by the DTC pending instruction, all interrupt requests are held pending.

Correct:

(Omitted)

Even if a DTC transfer request is generated, DTC transfer is held pending immediately after the following instructions. Also, the DTC is not activated between PREFIX instruction code and the instruction immediately after that code.

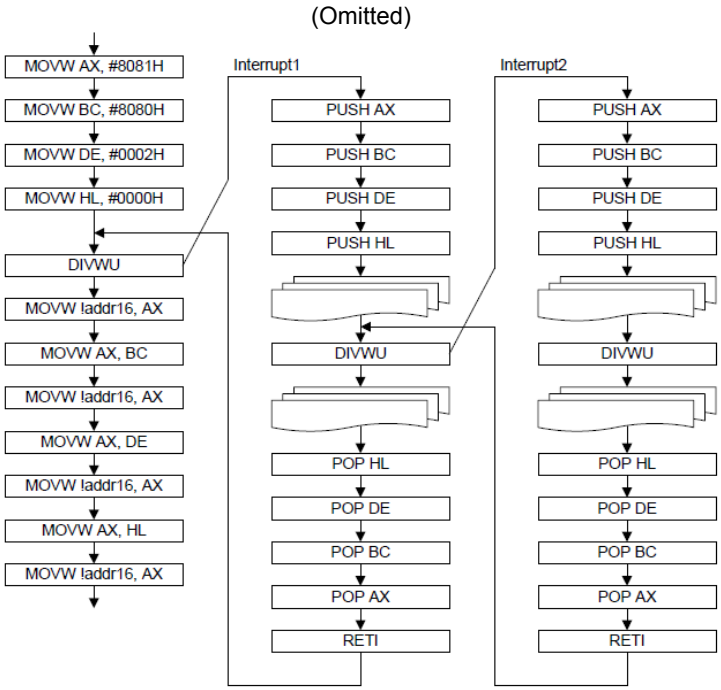
- Call/return instruction
- Unconditional branch instruction
- Conditional branch instruction
- Read access instruction for code flash memory
- Bit manipulation instructions for IFxx, MKxx, PRxx, and PSW, and an 8-bit manipulation instruction that has the ES register as operand
- Instruction for accessing the data flash memory
- Instruction of Multiply, Divide, Multiply & Accumulate (excluding MULU)

Caution 1. When a DTC transfer request is acknowledged, all interrupt requests are held pending until DTC transfer is completed.
Caution 2. While the DTC is held pending by the DTC pending instruction, all interrupt requests are held pending.

9. 21.4.4 Interrupt servicing during division instruction (Page 1021)

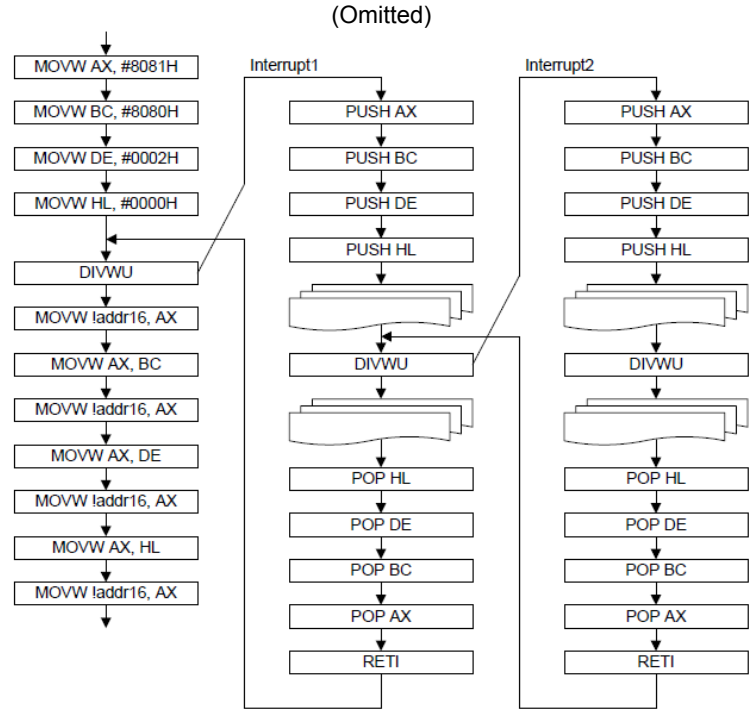
Incorrect:

The RL78/G14 handles interrupts during the DIVHU/DIVWU instruction in order to enhance the interrupt response when a division instruction is executed.



Correct:

The RL78/G14 handles interrupts during the DIVHU/DIVWU instruction in order to enhance the interrupt response when a division instruction is executed.



Caution Disable interrupts when executing the DIVHU or DIVWU instruction in an interrupt servicing routine.

Alternatively, unless they are executed in the RAM area, note that execution of a DIVHU or DIVWU instruction is possible even with interrupts enabled as long as a NOP instruction is added immediately after the DIVHU or DIVWU instruction in the assembly language source code. The following compilers automatically add a NOP instruction immediately after any DIVHU or DIVWU instruction output during the build process.

- V. 1.71 and later versions of the CA78K0R (Renesas Electronics compiler), for both C and assembly language source code
- Service pack 1.40.6 and later versions of the EWRL78 (IAR compiler), for C language source code
- GNURL78 (KPIT compiler), for C language source code

10. 21.4.5 Interrupt request hold (Page 1022)

Incorrect:

There are instructions where, even if an interrupt request is issued while the instructions are being executed, interrupt request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV PSW, A
- MOV1 PSW. bit, CY
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- POP PSW
- BTCLR PSW. bit, $addr20
- EI
- DI
- SKC
- SKNC
- SKZ
- SKNZ
- SKH
- SKNH
- Write instructions for the IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and PR12H registers

Correct:

There are instructions where, even if an interrupt request is issued while the instructions are being executed, interrupt request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV PSW, A
- MOV1 PSW. bit, CY
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- POP PSW
- BTCLR PSW. bit, $addr20
- EI
- DI
- SKC
- SKNC
- SKZ
- SKNZ
- SKH
- SKNH
- MULHU
- MULH
- MACHU
- MACH
- Write instructions for the IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and PR12H registers

11. 33.2 Operation List (Page 1153)

Incorrect:

Table 33 - 16 Operation List (12/18)

(Omitted)

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Remark 1. Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.
Remark 2. MACR indicates the multiplication and accumulation register (MACRH, MACRL).

Correct:

Table 33 - 16 Operation List (12/18)

(Omitted)

Note 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.
Note 2. Number of CPU clocks (f_{CLK}) when the code flash memory is accessed, or when the data flash memory is accessed by an 8-bit instruction.

Remark 1. Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.
Remark 2. MACR indicates the multiplication and accumulation register (MACRH, MACRL).

Caution Disable interrupts when executing the DIVHU or DIVWU instruction in an interrupt servicing routine.
Alternatively, unless they are executed in the RAM area, note that execution of a DIVHU or DIVWU instruction is possible even with interrupts enabled as long as a NOP instruction is added immediately after the DIVHU or DIVWU instruction in the assembly language source code. The following compilers automatically add a NOP instruction immediately after any DIVHU or DIVWU instruction output during the build process.

- V. 1.71 and later versions of the CA78K0R (Renesas Electronics compiler), for both C and assembly language source code
- Service pack 1.40.6 and later versions of the EWRL78 (IAR compiler), for C language source code
- GNURL78 (KPIT compiler), for C language source code