Date: July. 2, 2014

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A030A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G14 Descriptions in the Hardware User's Manual Rev. 2.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G14 R5F104xxx	Lot No. All lots	Reference Document	RL78/G14 User's Manual: Hardware Rev.2.00 R01UH0186EJ0200 (Nov. 2013)		

This document describes misstatements found in the RL78/G14 User's Manual: Hardware Rev.2.00 (R01UH0186EJ0200).

Corrections

Applicable Item	Applicable Page	Contents
2.4 Pin Block Diagrams (Figure2-5, Figure2-7 and addition)	Pages 94 and 96	Incorrect descriptions revised
17.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 17-74. and Figure 17-76.)	Pages 749 and 751	Incorrect descriptions revised
17.7.3 SNOOZE mode function	Page 809	Incorrect descriptions revised
17.7.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 17-123., Figure 17-124. and Figure 17-126.)	Pages 811, 812 and 814	Incorrect descriptions revised
19.1 Alteration of Note of DTC function	Page 938	Incorrect descriptions revised
34.5.1 Serial array unit (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)	Page 1191	Incorrect descriptions revised
34.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 1209	Content change
35.5.1 Serial array unit (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)	Page 1252	Incorrect descriptions revised
35.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 1267	Content change

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0186EJ0200	
1	**Figure 29-6 Format of Option Byte (000C2H/010C2H)**		**Pages 1087**	**Page 3**
2	**2.4 Pin Block Diagrams (Figure2-5, Figure2-7 and addition)**		**Pages 94 and 96**	**Pages 4 to 9**
3	**17.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 17-74. and Figure 17-76.)**		**Pages 749 and 751**	**Pages 10 and 11**
4	**17.7.3 SNOOZE mode function**		**Page 809**	**Page 12**
5	**17.7.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 17-123., Figure 17-124. and Figure 17-126.)**		**Pages 811, 812 and 814**	**Pages 13 to 15**
6	**19.1 Alteration of Note of DTC function**		**Page 938**	**Page 16**
7	**34.5.1 Serial array unit (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**		**Page 1191**	**Page 17**
8	**34.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics**		**Page 1209**	**Page 18**
9	**35.5.1 Serial array unit (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**		**Page 1252**	**Page 19**
10	**35.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics**		**Page 1267**	**Page 20**

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G14 User's Manual: Hardware Rev.2.00 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A020A/E	Dec. 19, 2013	First edition issued No.1 in a correction
TN-RL*-A030A/E	Jul. 2, 2014	second edition issued No.2 to 10 in corrections (This notice)

1. Figure 29-6 Format of Option Byte (000C2H/010C2H) (page 1087)

Incorrect:

Figure 29-6 Format of Option Byte (000C2H/010C2H)

Address: 000C2H/010C2H Note

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	0	HS (high speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 32 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

Correct:

Figure 29-6 Format of Option Byte (000C2H/010C2H)

Address: 000C2H/010C2H Note

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

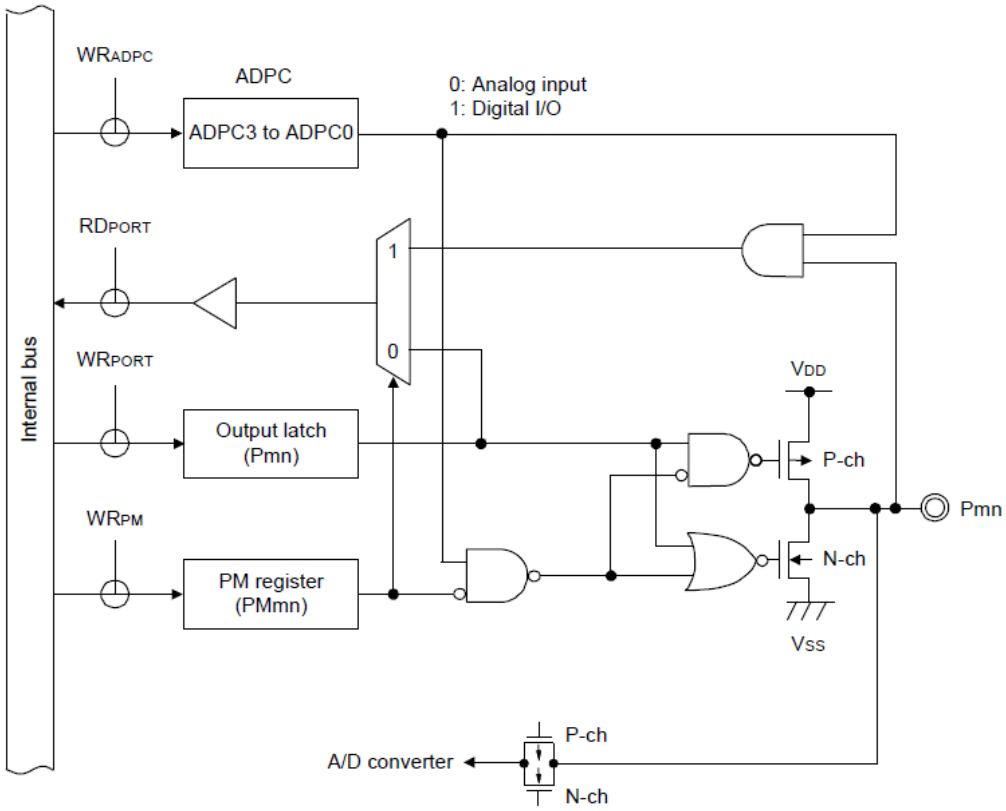
CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 32 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

2. 2.4 Pin Block Diagrams

Incorrect descriptions revised of Pin Block Diagrams (Figure2-5, Figure2-7 and addition) (Pages 94 and 96)

Incorrect:

Figure 2-5 Pin Block Diagram of Pin Type 4-3-1

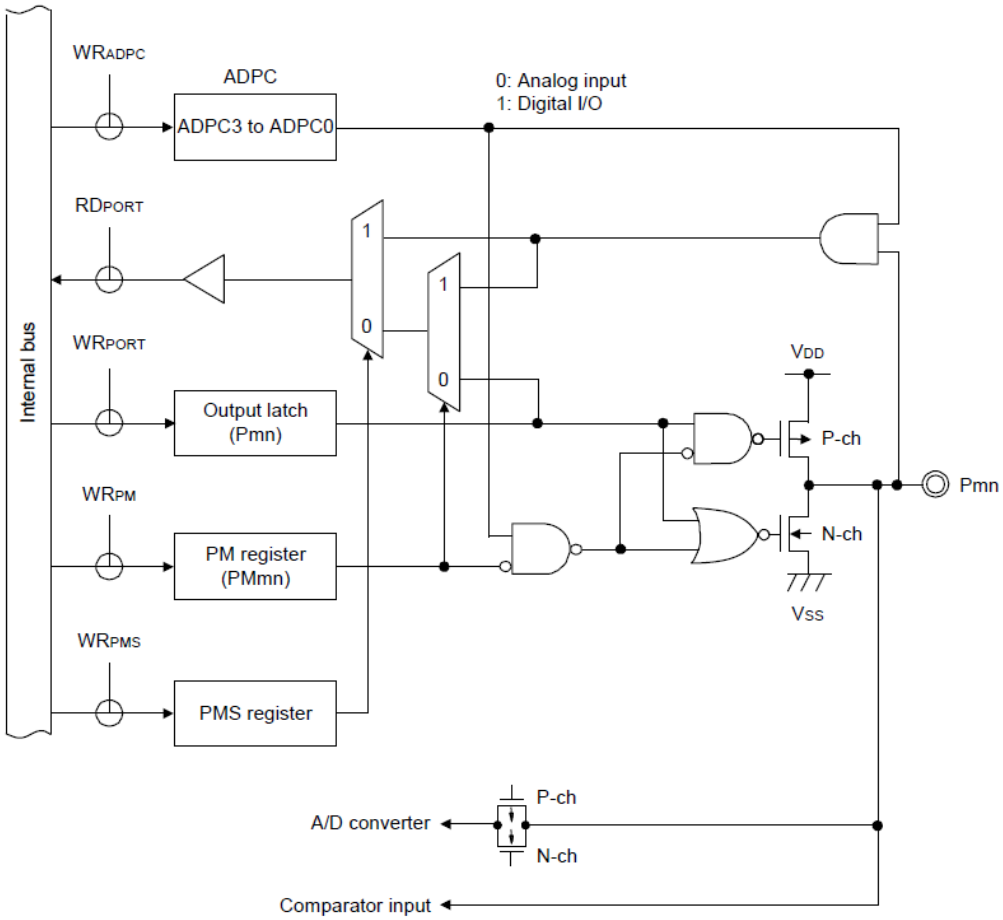


Correct:

Deleted (not exist port)

Incorrect:

Figure 2-7 Pin Block Diagram of Pin Type 4-6-1



Correct:

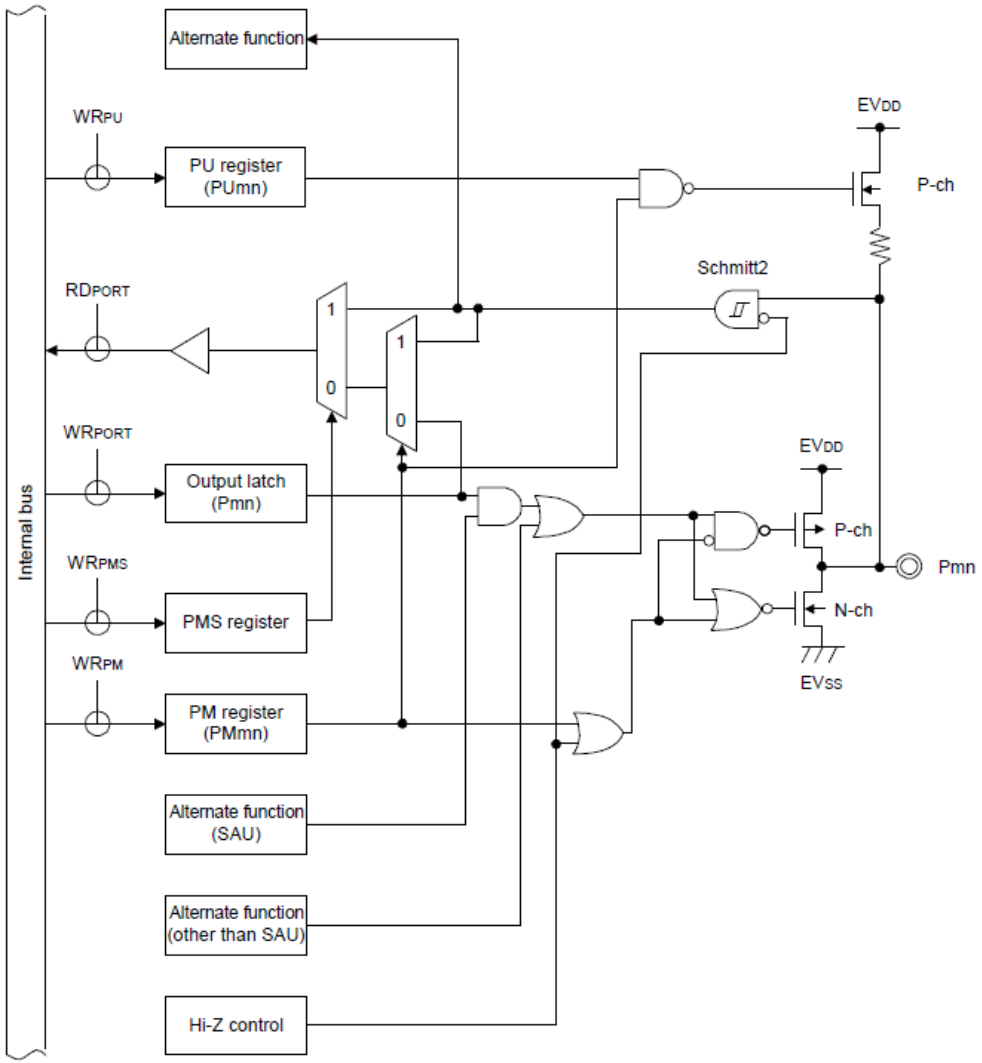
Deleted (not exist port)

Incorrect:

non-existent

Correct:

Pin Block Diagram of Pin Type 7-1-7

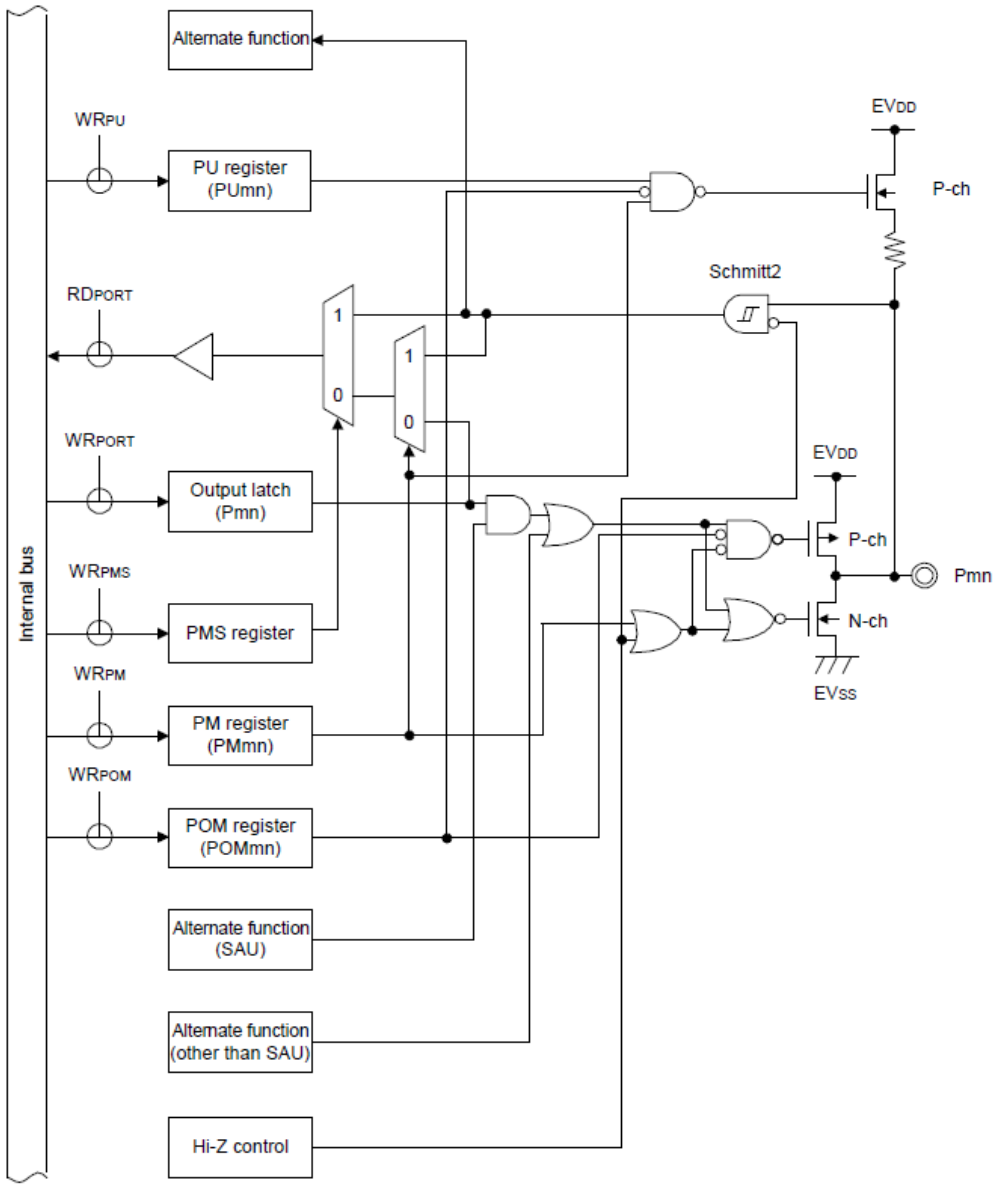


Incorrect:

non-existent

Correct:

Pin Block Diagram of Pin Type 7-1-8

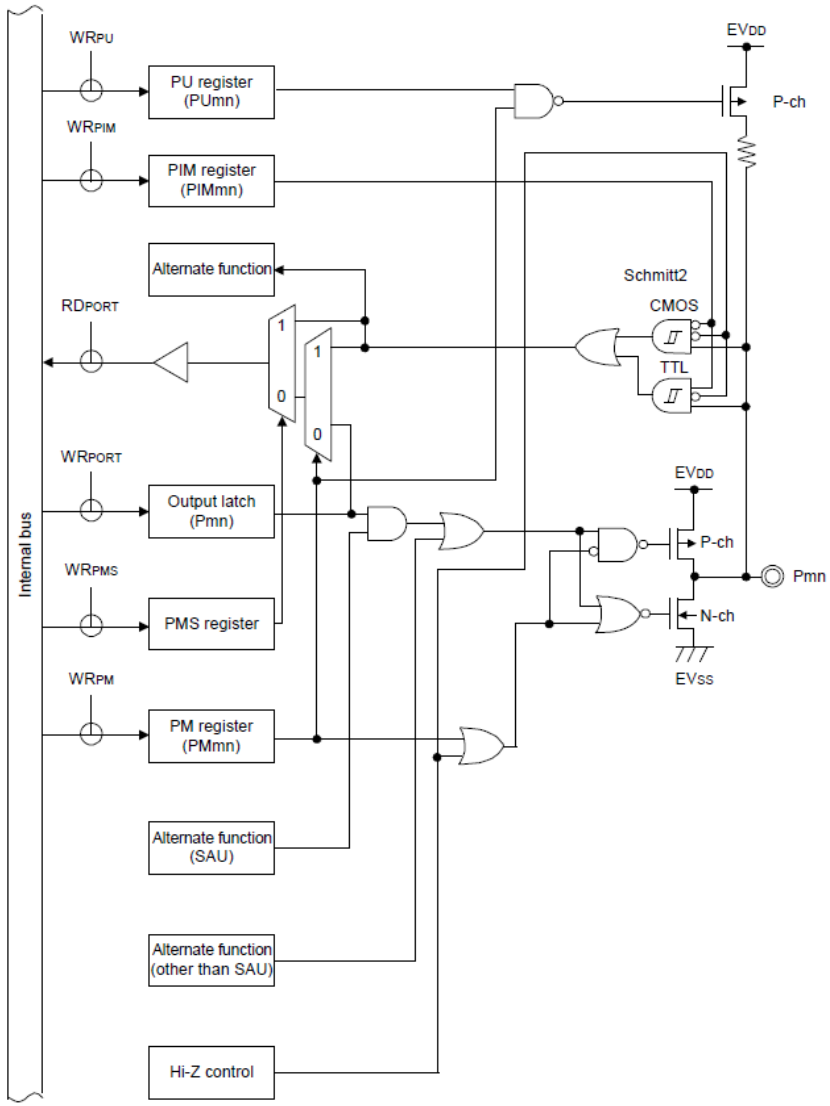


Incorrect:

non-existent

Correct:

Pin Block Diagram of Pin Type 8-1-7

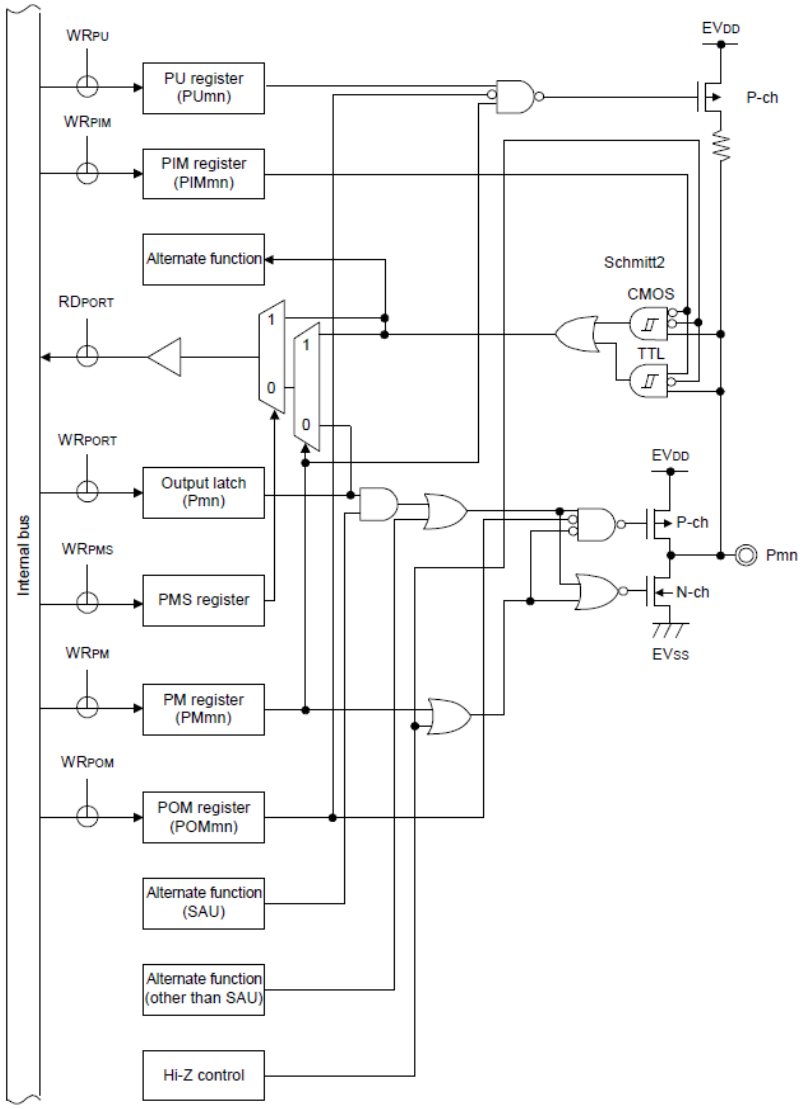


Incorrect:

non-existent

Correct:

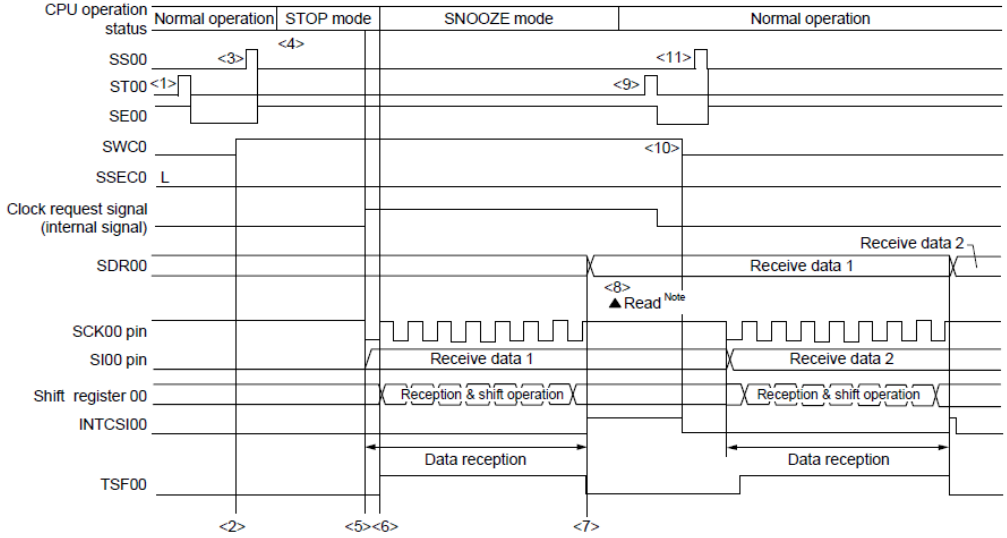
Pin Block Diagram of Pin Type 8-1-8



3. 17.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 17-74. and Figure 17-76.) (Pages 749 and 751)

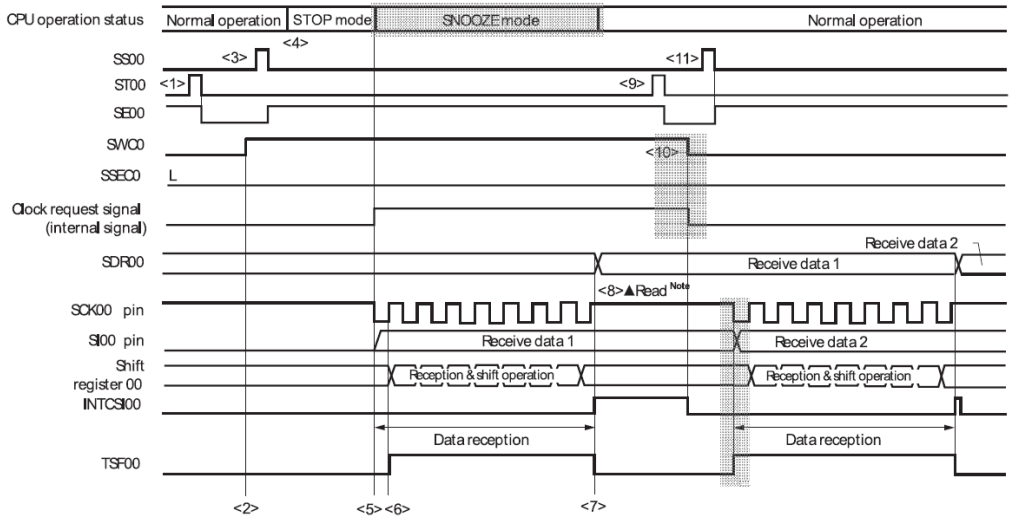
It is correction of "CPU operation status", "Clock request signal (internal signal)" and "TSF00" in this Figure.

Incorrect:
Figure 17-74. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:
Figure 17-74. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)

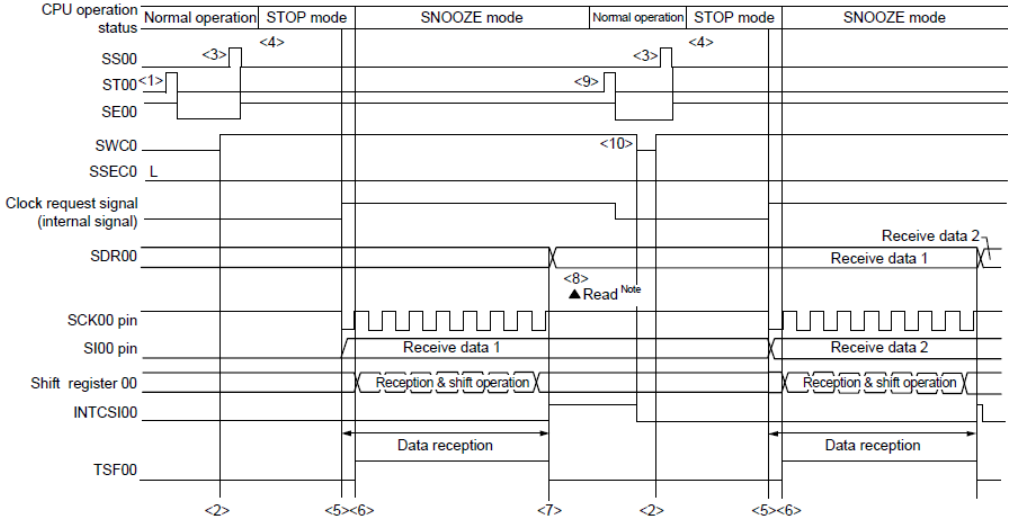


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)” and “INTCSI00” in this Figure.

Incorrect:

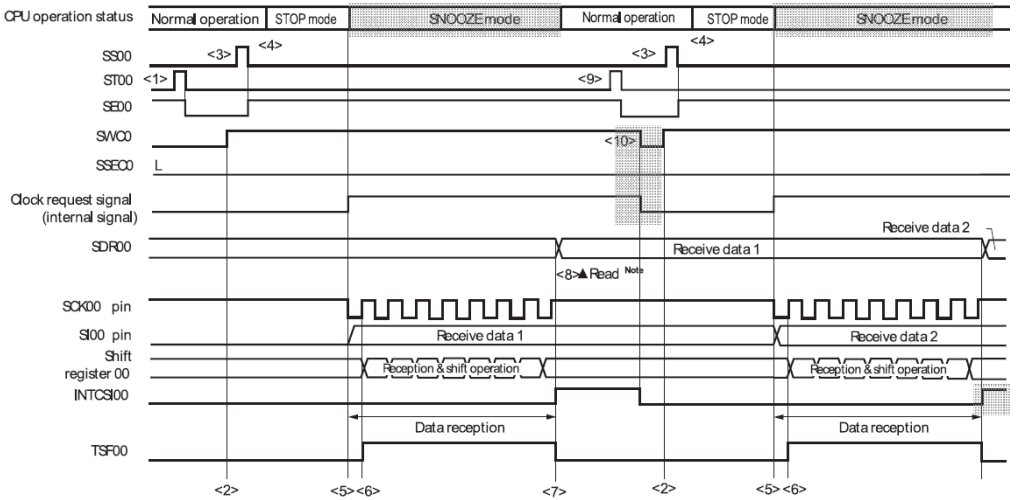
Figure 17-76. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:

Figure 17-76. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

4. 17.7.3 SNOOZE mode function (Page 809)

Incorrect:

17.7.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation. Only the following UARTs can be specified when FRQSEL4 in the option byte (000C2H) = 0 in the SNOOZE mode.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

Cautions 4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Correct:

17.7.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation. Only the following UARTs can be specified when FRQSEL4 in the option byte (000C2H) = 0 in the SNOOZE mode.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

Cautions 4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

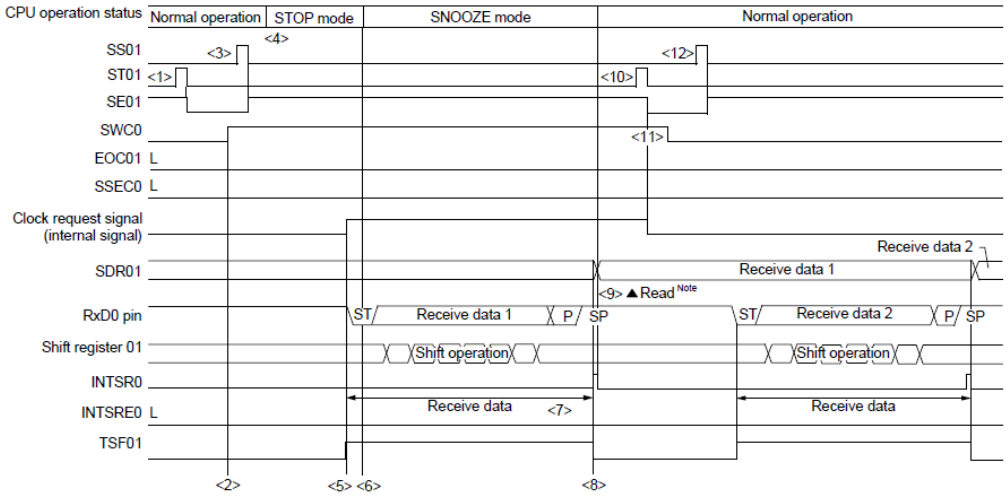
Cautions 5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note, however, that transfer through the UART channel may not start and the CPU may remain in the SNOOZE mode if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may not be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

5. 17.7.3 SNOOZE mode function
Timing Chart of SNOOZE Mode Operation (Figure 17-123., Figure 17-124. and Figure 17-126.) (Pages 811, 812 and 814)

It is correction of "CPU operation status", "Clock request signal (internal signal)", "INTSR0" and "TSF01" in this Figure.

Incorrect:

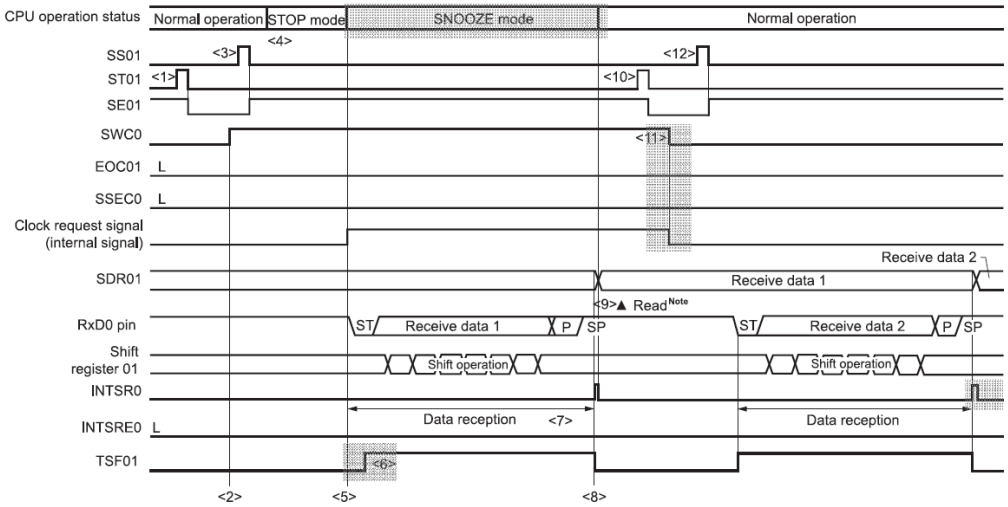
Figure 17-123. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)



(omitted)

Correct:

Figure 17-123. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)

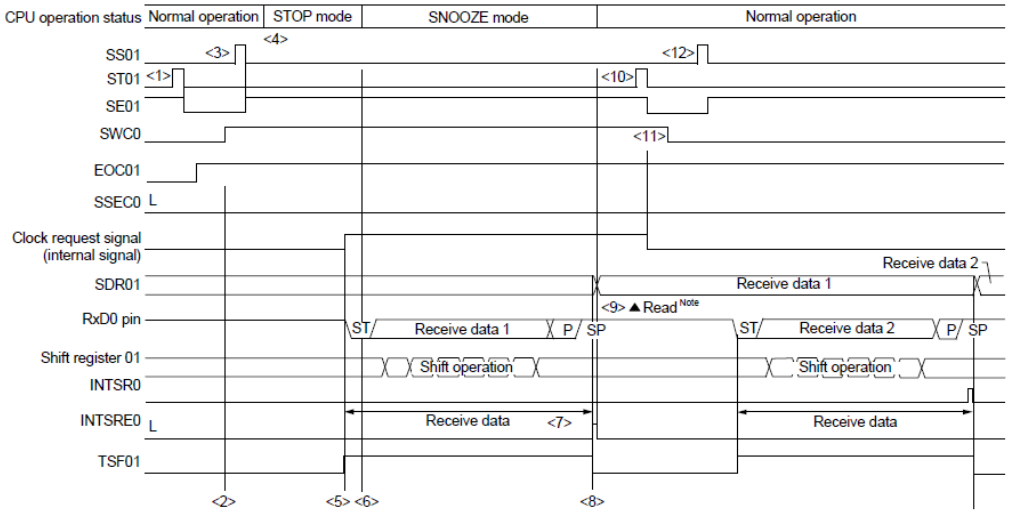


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

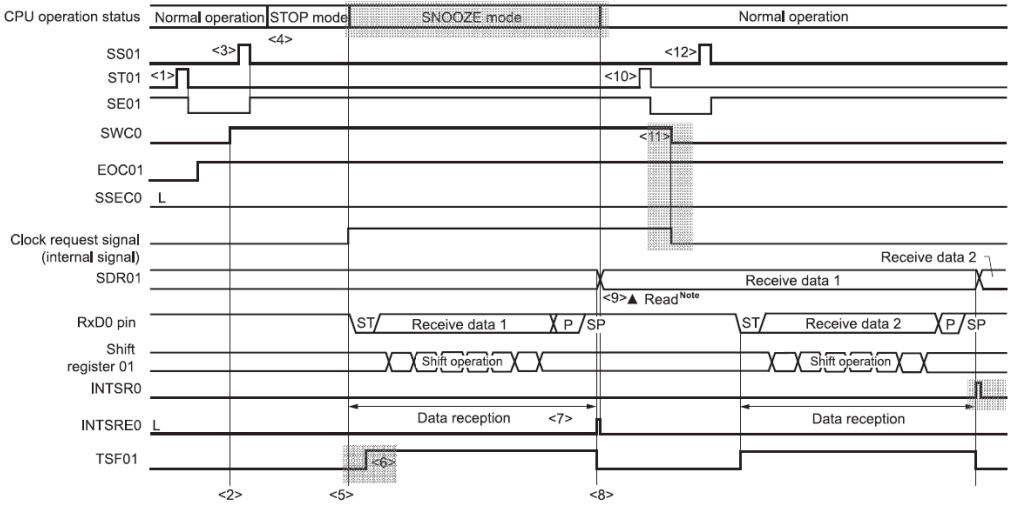
Figure 17-124. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)



(omitted)

Correct:

Figure 17-124. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)

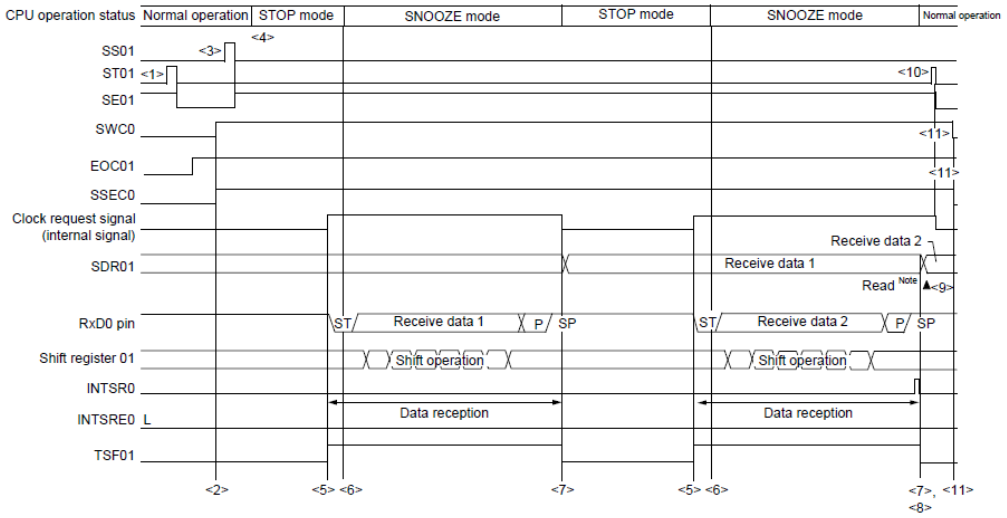


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

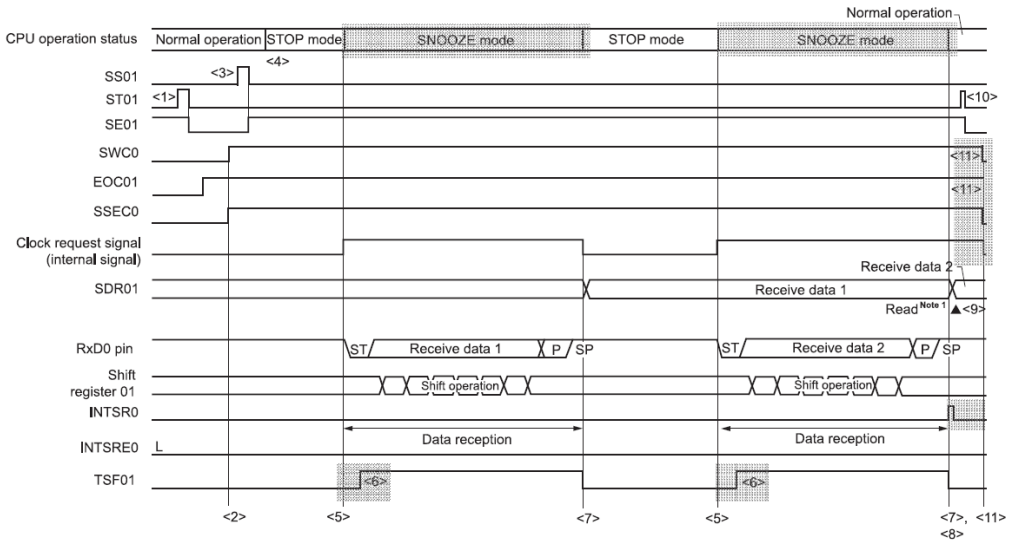
Figure 17-126. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

Correct:

Figure 17-126. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

6. 19.1 Alteration of Note of DTC function (Page 938)

Incorrect:

Table 19-1. DTC Specifications

(omitted)

Note **In the SNOOZE mode,** these areas cannot be set as the sources for DTC transfer since the flash memory is stopped.

Remark i = 0 to 4, j = 0 to 23

Correct:

Table 19-1. DTC Specifications

(omitted)

Note In the HALT mode and SNOOZE mode, these areas cannot be set as the sources for DTC transfer since the flash memory is stopped.

Remark i = 0 to 4, j = 0 to 23

7. 34.5.1 Serial array unit (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input) (Page 1191)

Incorrect:

34.5.1 Serial array unit

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
(omitted)									
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.7 V ≤ EV_{DD0} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD0} ≤ 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
(omitted)									

(omitted)

Correct:

34.5.1 Serial array unit

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
(omitted)									
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
(omitted)									

(omitted)

8. 34.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1209)

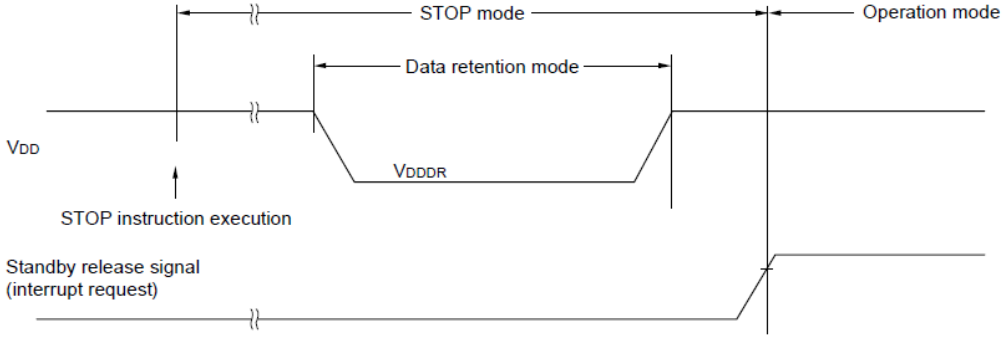
Old:

34.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



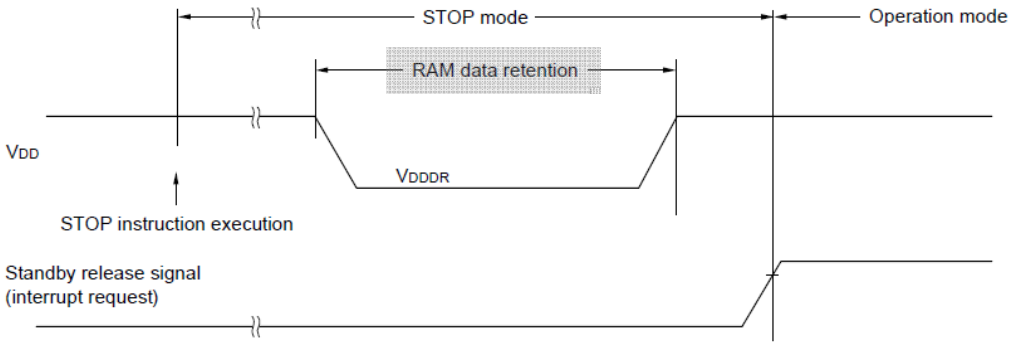
New:

34.7 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



9. 35.5.1 Serial array unit (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input) (Page 1252)

Incorrect:

35.5.1 Serial array unit

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
(omitted)					
SIp setup time (to SCKp↑) Note 2	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 40		ns
		~~2.7 V ≤ EV_{DD0} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V~~	1/f_{MCK} + 40		ns
		~~2.4 V ≤ EV_{DD0} ≤ 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V~~	1/f_{MCK} + 60		ns
(omitted)					

(omitted)

Correct:

35.5.1 Serial array unit

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
(omitted)					
SIp setup time (to SCKp↑) Note 2	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 40		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	1/f_{MCK} + 60		ns
(omitted)					

(omitted)

10. 35.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1267)

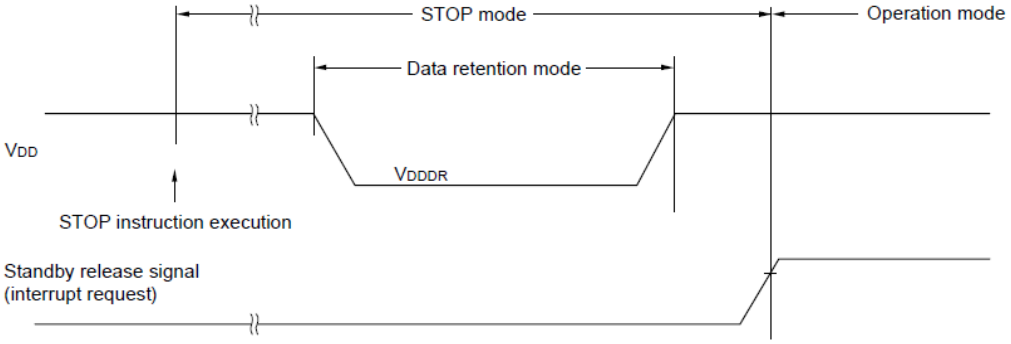
Old:

35.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = −40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



New:

35.7 RAM Data Retention Characteristics

(T_A = −40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.