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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0138A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G12 Descriptions in the User's Manual: Hardware Rev. 2.40 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G12 Group	Lot No. All lots	Reference Document	RL78/G12 User's Manual: Hardware Rev. 2.40 R01UH0200EJ0240 (Mar. 2024)		

This document describes misstatements found in the RL78/G12 User's Manual: Hardware Rev. 2.40 (R01UH0200EJ0240).

Corrections

Applicable Item	Applicable Page	Contents
4.5.3 Register setting examples for using the port and alternate functions	Page 105, Page 107, Page 110, Page 112	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0200EJ 0240	
1	4.5.3 Register setting examples for using the port and alternate functions		Page 105, Page 107, Page 110, Page 112	Page 3 ~ Page 6

Incorrect: Bold with underline; Correct: Gray hatched

Revision History No,

RL78/G12 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0138A/E	Nov. 20, 2024	First edition issued Corrections No.1 revised (this document)

1. 4.5.3 Register setting examples for using the port and alternate functions (page 105, page 107, page 110, page 112)

Incorrect:

(page 105)

(omitted)

Table 4-7. Setting Examples of Registers and Output Latches When Using Alternate Function (20-, 24-Pin Products) (1/5)

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU	Other than SAU
P00[Note 1]	P00	Input	–	–	–	1	×	–	–
		Output	–	–	–	0	0/1	–	–
	KR6	Input	–	–	–	1	×	–	–
	(SI01)	Input	–	–	–	1	×	–	–
P10	P10	Input	–	×	0	1	×	×	×
		Output	–	0	0	0	0/1	SCK00/ SCL00 = 1	PCLBZ0 = 0
		N-ch open drain output	–	1	0	0	0/1		
	ANI16	Input	–	×	1	1	×	×	×
	PCLBZ0	Output	–	0	0	0	0	SCK00/SCL00 = 1	×
	SCK00	Input	–	×	0	1	×	×	PCLBZ0 = 0
		Output	–	0/1	0	0	1	×	PCLBZ0 = 0
	SCL00[Note 2]	Output	–	0/1	0	0	1	×	PCLBZ0 = 0

Notes 1. Provided only in 24-pin products.

2. Provided only in the R5F102 products.

Correct:

(page 105)

(omitted)

Table 4-7. Setting Examples of Registers and Output Latches When Using Alternate Function (20-, 24-Pin Products) (1/5)

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU	Other than SAU
P00[Note 1]	P00	Input	–	–	–	1	×	–	–
		Output	–	–	–	0	0/1	–	–
	KR6	Input	–	–	–	1	×	–	–
	(SI01)	Input	–	–	–	1	×	–	–
P10	P10	Input	–	×	0	1	×	×	×
		Output	–	0	0	0	0/1	SCK00/ SCL00 = 1	PCLBUZ0 = 0
		N-ch open drain output	–	1	0	0	0/1		
	ANI16	Input	–	×	1	1	×	×	×
	PCLBUZ0	Output	–	0	0	0	0	SCK00/SCL00 = 1	×
	SCK00	Input	–	×	0	1	×	×	×
		Output	–	0/1	0	0	1	×	PCLBUZ0 = 0
	SCL00[Note 2]	Output	–	0/1	0	0	1	×	PCLBUZ0 = 0

Notes 1. Provided only in 24-pin products.

2. Provided only in the R5F102 products.

Incorrect:

(page 107)

Table 4-7. Setting Examples of Registers and Output Latches When Using Alternate Function
(20-, 24-Pin Products (4/5))

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU	Other than SAU
P40	P40	Input	–	–	–	1	×	–	–
		Output	–	–	–	0	0/1	–	–
	KR0	Input	–	–	–	1	×	–	–
P41	P41	Input	–	×	0	1	×	×	×
		Output	–	0	0	0	0/1	SO01/SDA01 = 1	TO02 = 0
		N-ch open drain output	–	1	0	0	0/1		
	ANI22	Input	–	×	1	1	×	×	
	SO01Note 2	Output	PIOR3 = 0Note 1	0/1	0	0	1	×	TO02 = 0
	SDA01Note 2	I/O	PIOR3 = 0Note 1	1	0	0	1	×	TO02 = 0
	TI02	Input	PIOR2 = 0	×	0	1	×	×	×
	TO02	Output	–	0	0	0	0	SO01/SDA01 = 1	×
	INTP1	Input	–	×	0	1	×	×	×
P42	P42	Input	–	–	0	1	×	×	×
		Output	–	–	0	0	0/1	SCK01/SCL01 = 1	TO03 = 0
	ANI21	Input	–	–	1	1	×	×	×
	SCK01Note 2	Input	PIOR3 = 0Note 1	–	0	1	×	×	×
		Output	PIOR3 = 0Note 1	–	0	0	1	×	TO03 = 0
	SCL01Note 2	Output	PIOR3 = 0Note 1	–	0	0	1	×	TO03 = 0
	TI03	Input	PIOR2 = 0	–	0	1	×	×	×
	TO03	Output	–	–	0	0	0	SCK01/SCL01 = 1	×
P60	P60	Input	–	–	–	1	×	×	×
		N-ch open drain output (6-V tolerance)	–	–	–	0	0/1	SCLA0/(TxD0) = 1	×
	KR4	Input	–	–	–	1	×	×	×
	SCLA0	I/O	–	–	–	0	0	×	×
	(TxD0)	Output	PIOR1 = 1	–	–	0	1	×	×
P61	P61	Input	–	–	–	1	×	×	×
		N-ch open drain output (6-V tolerance)	–	–	–	0	0/1	SDAA0 = 1	×
	KR5	Input	–	–	–	1	×	×	×
	SDAA0	I/O	–	–	–	0	0	×	×
	(RxD0)	Input	PIOR1 = 1	–	–	1	×	×	×

Notes 1. Provided only in 24-pin products.

2. Provided only in the R5F102 products.

Correct:

(page 107)

Table 4-7. Setting Examples of Registers and Output Latches When Using Alternate Function
(20-, 24-Pin Products (4/5))

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU	Other than SAU
P40	P40	Input	–	–	–	1	×	–	–
		Output	–	–	–	0	0/1	–	–
	KR0	Input	–	–	–	1	×	–	–
P41	P41	Input	–	×	0	1	×	×	×
		Output	–	0	0	0	0/1	SO01/SDA01 = 1	TO02 = 0
		N-ch open drain output	–	1	0	0	0/1		
	ANI22	Input	–	×	1	1	×	×	×
	SO01Note 2	Output	PIOR3 = 0Note 1	0/1	0	0	1	×	TO02 = 0
	SDA01Note 2	I/O	PIOR3 = 0Note 1	1	0	0	1	×	TO02 = 0
	TI02	Input	PIOR2 = 0	×	0	1	×	×	×
	TO02	Output	–	0	0	0	0	SO01/SDA01 = 1	×
	INTP1	Input	–	×	0	1	×	×	×
P42	P42	Input	–	–	0	1	×	×	×
		Output	–	–	0	0	0/1	SCK01/SCL01 = 1	TO03 = 0
	ANI21	Input	–	–	1	1	×	×	×
	SCK01Note 2	Input	PIOR3 = 0Note 1	–	0	1	×	×	×
		Output	PIOR3 = 0Note 1	–	0	0	1	×	TO03 = 0
	SCL01Note 2	Output	PIOR3 = 0Note 1	–	0	0	1	×	TO03 = 0
	TI03	Input	PIOR2 = 0	–	0	1	×	×	×
	TO03	Output	–	–	0	0	0	SCK01/SCL01 = 1	×
P60	P60	Input	–	–	–	1	×	×	×
		N-ch open drain output (6-V tolerance)	–	–	–	0	0/1	(TxD0) = 1	SCLA0 = 0
	KR4	Input	–	–	–	1	×	×	×
	SCLA0	I/O	–	–	–	0	0	×	×
	(TxD0)	Output	PIOR1 = 1	–	–	0	1	×	×
P61	P61	Input	–	–	–	1	×	–	×
		N-ch open drain output (6-V tolerance)	–	–	–	0	0/1	–	SDAA0 = 0
	KR5	Input	–	–	–	1	×	–	×
	SDAA0	I/O	–	–	–	0	0	–	×
	(RxD0)	Input	PIOR1 = 1	–	–	1	×	–	×

Notes 1. Provided only in 24-pin products.

2. Provided only in the R5F102 products.

Incorrect:

(page 110)

Table 4-8. Setting Examples of Registers and Output Latches When Using Alternate Function (30-Pin Products) (2/6)

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU	Other than SAU
P14	P14	Input	–	×	–	1	×		
		Output	–	0	–	0	0/1	SDA20 = 1	(SCLA0)/(TO03) = 0
		N-ch open drain output	–	1	–	0	0/1		
	RxD2Note	Input	PIOR1 = 0	×	–	1	×	×	×
	SI20Note	Input	PIOR1 = 0	×	–	1	×	×	×
	SDA20Note	I/O	PIOR1 = 0	1	–	0	1	×	(SCLA0)/(TO03) = 0
	(SCLA0)	I/O	PIOR2 = 1	1	–	0	0	SDA20 = 1	(TO03) = 0
	(TI03)	Input	PIOR0 = 1	×	–	1	×	×	×
						0	0	SDA20 = 1	(SCLA0) = 0
P17	P15	Input	–	×	–	1	×	×	×
		Output	–	0	–	0	0/1	(TxD0) = 1	TO02 = 0
		N-ch open drain output	–	1	–	0	0/1		
	TI02	Input	PIOR0 = 0	×	–	1	×	×	×
	TO02	Output	PIOR0 = 0	0	–	0	0	(TxD0) = 1	×
	(TxD0)	Output	PIOR1 = 1	0/1	–	0	1	×	TO02 = 0

Note Provided only in the R5F102 products.

Correct:

(page 110)

Table 4-8. Setting Examples of Registers and Output Latches When Using Alternate Function (30-Pin Products) (2/6)

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU	Other than SAU
P14	P14	Input	–	×	–	1	×	×	×
		Output	–	0	–	0	0/1	SDA20 = 1	(SCLA0)/(TO03) = 0
		N-ch open drain output	–	1	–	0	0/1		
	RxD2Note	Input	PIOR1 = 0	×	–	1	×	×	×
	SI20Note	Input	PIOR1 = 0	×	–	1	×	×	×
	SDA20Note	I/O	PIOR1 = 0	1	–	0	1	×	(SCLA0)/(TO03) = 0
	(SCLA0)	I/O	PIOR2 = 1	1	–	0	0	SDA20 = 1	(TO03) = 0
	(TI03)	Input	PIOR0 = 1	×	–	1	×	×	×
						0	0	SDA20 = 1	(SCLA0) = 0
P17	P15	Input	–	×	–	1	×	×	×
		Output	–	0	–	0	0/1	(TxD0) = 1	TO02 = 0
		N-ch open drain output	–	1	–	0	0/1		
	TI02	Input	PIOR0 = 0	×	–	1	×	×	×
	TO02	Output	PIOR0 = 0	0	–	0	0	(TxD0) = 1	×
	(TxD0)	Output	PIOR1 = 1	0/1	–	0	1	×	TO02 = 0

Note Provided only in the R5F102 products.

Incorrect:

(page 112)

Table 4-8. Setting Examples of Registers and Output Latches When Using Alternate Function (30-Pin Products) (5/6)

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU	Other than SAU
P60	P60	Input	–	–	–	1	×	×	×
		N-ch open drain output (6-V tolerance)	–	–	–	0	0/1	SCLA0 = 1	×
	SCLA0	I/O	PIOR2 = 0	–	–	0	0	×	×
P61	P61	Input	–	–	–	1	×	×	×
		N-ch open drain output (6-V tolerance)	–	–	–	0	0/1	SDAA0 = 1	×
	SDAA0	I/O	PIOR2 = 0	–	–	0	0	×	×
P120	P120	Input	–	–	0	1	×	–	–
		Output	–	–	0	0	0/1	–	–
	ANI19	Analog input	–	–	1	1	×	–	–
P137	P137	Input	–	–	–	–	×	–	–
	INTP0	Input	–	–	–	–	×	–	–
P147	P147	Input	–	–	0	1	×	–	–
		Output	–	–	0	0	0/1	–	–
	ANI18	Analog input	–	–	1	1	×	–	–

(omitted)

Correct:

(page 112)

Table 4-8. Setting Examples of Registers and Output Latches When Using Alternate Function (30-Pin Products) (5/6)

Pin Name	Used Function		PIORx	POMxx	PMCxx	PMxx	Pxx	Alternate Function Output	
	Function Name	I/O						SAU	Other than SAU
P60	P60	Input	–	–	–	1	×	–	×
		N-ch open drain output (6-V tolerance)	–	–	–	0	0/1	–	SCLA0 = 0
	SCLA0	I/O	PIOR2 = 0	–	–	0	0	–	×
P61	P61	Input	–	–	–	1	×	–	×
		N-ch open drain output (6-V tolerance)	–	–	–	0	0/1	–	SDAA0 = 0
	SDAA0	I/O	PIOR2 = 0	–	–	0	0	–	×
P120	P120	Input	–	–	0	1	×	–	–
		Output	–	–	0	0	0/1	–	–
	ANI19	Analog input	–	–	1	1	×	–	–
P137	P137	Input	–	–	–	–	×	–	–
	INTP0	Input	–	–	–	–	×	–	–
P147	P147	Input	–	–	0	1	×	–	–
		Output	–	–	0	0	0/1	–	–
	ANI18	Analog input	–	–	1	1	×	–	–

(omitted)