

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-RL*-A0133B/E	Rev.	2.00
Title	Correction for Incorrect Description Notice RL78/G23 Descriptions in the User's Manual: Hardware Rev. 1.30 Changed		Information Category	Technical Notification	
Applicable Product	RL78/G23 Group	Lot No.	Reference Document	RL78/G23 User's Manual: Hardware Rev. 1.30 R01UH0896EJ0130 (Jan. 2024)	
		All lots			

This document describes misstatements found in the RL78/G23 User's Manual: Hardware Rev. 1.30 (R01UH0896EJ0130).

Corrections

Applicable Item	Applicable Page	Contents
2.2.3.2 Connecting the VBAT pin to the battery for use in backing up	Page 106	Incorrect descriptions revised
2.2.3.3 Using the VBAT pin	Page 107	Incorrect descriptions revised
2.4 Block Diagrams of Pins	Page 125, Page 126, Page 132, Page 135, Page 138 to Page 141, Page 143 to Page 145	Incorrect descriptions revised
4.5.4 Examples of register settings for port and alternate functions	Page 262, Page 281	Incorrect descriptions revised
12.3.8 Analog input channel specification register (ADS)	Page 574	Incorrect descriptions revised
12.6.6 Software trigger wait mode (select mode, one-shot conversion mode)	Page 586	Incorrect descriptions revised
15.3.8 Serial status register mn (SSRmn)	Page 666	Incorrect descriptions revised
15.3.13 Serial output register m (SOM)	Page 671	Incorrect descriptions revised
17.3.4 Baud Rate Generator	Page 943	Incorrect descriptions revised
19.4.3 Repeat mode	Page 1024, Page 1025	Incorrect descriptions revised
37.2.3 Characteristics of the On-chip Oscillators	Page 1401	Incorrect descriptions revised
37.3.1 Pin characteristics	Page 1406	Incorrect descriptions revised
37.3.2 Supply current characteristics	Page 1411, Page 1414, Page 1418, Page 1421, Page 1425, Page 1428	Incorrect descriptions revised
37.6.1 A/D converter characteristics	Page 1475, Page 1476	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0896EJ0130	
1	3.1 Memory Space		Page 147 to Page 153, Page 160	Page 3 to Page 10
2	33.6.1 Self-programming procedure		Page 1315	Page 11
3	33.10.1 Overview of the data flash memory		Page 1366	Page 12
4	34.3 Security Settings for On-chip Debugging		Page 1369	Page 13
5	2.2.3.2 Connecting the VBAT pin to the battery for use in backing up		Page 106	Page 14
6	2.2.3.3 Using the VBAT pin		Page 107	Page 15
7	2.4 Block Diagrams of Pins		Page 125, Page 126, Page 132, Page 135, Page 138 to Page 141, Page 143 to Page 145	Page 16 to Page 25
8	4.5.4 Examples of register settings for port and alternate functions		Page 262, Page 281	Page 26, Page 27
9	12.3.8 Analog input channel specification register (ADS)		Page 574	Page 28
10	12.6.6 Software trigger wait mode (select mode, one-shot conversion mode)		Page 586	Page 29
11	15.3.8 Serial status register mn (SSRmn)		Page 666	Page 30
12	15.3.13 Serial output register m (SOM)		Page 671	Page 31
13	17.3.4 Baud Rate Generator		Page 943	Page 32
14	19.4.3 Repeat mode		Page 1024, Page 1025	Page 33 to Page 35
15	37.2.3 Characteristics of the On-chip Oscillators		Page 1401	Page 36
16	37.3.1 Pin characteristics		Page 1406	Page 37
17	37.3.2 Supply current characteristics		Page 1411, Page 1414, Page 1418, Page 1421, Page 1425, Page 1428	Page 38 to Page 43
18	37.6.1 A/D converter characteristics		Page 1475, Page 1476	Page 44, Page 45

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G23 Correction for incorrect description notice

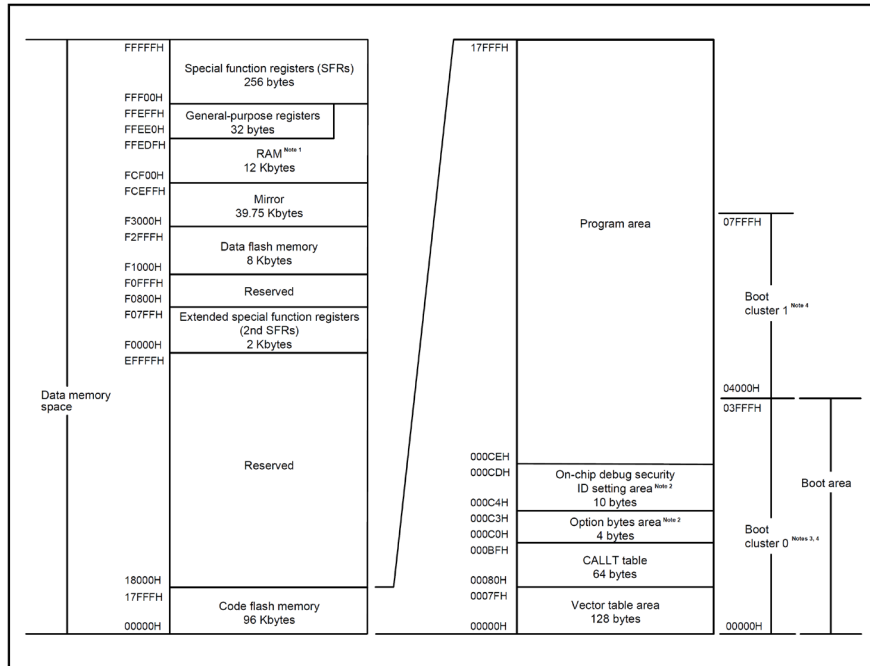
Document Number	Issue Date	Description
TN-RL*-A0133A/E	Apr. 26, 2024	First edition issued Corrections No.1 to No.4 revised
TN-RL*-A0133B/E	May 22, 2025	Corrections No.5 to No.18 revised (this document)

1. 3.1 Memory Space (Page 147 to Page 153, Page 160)

Incorrect:
(Page 147)

Products in the RL78/G23 can access a 1 MB address space. Figure 3 - 1 to Figure 3 - 3 show the memory maps.

Figure 3 - 1 Memory Map (R7F100GxF (x = A, B, C, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. ~~When boot swap is not used:~~ Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

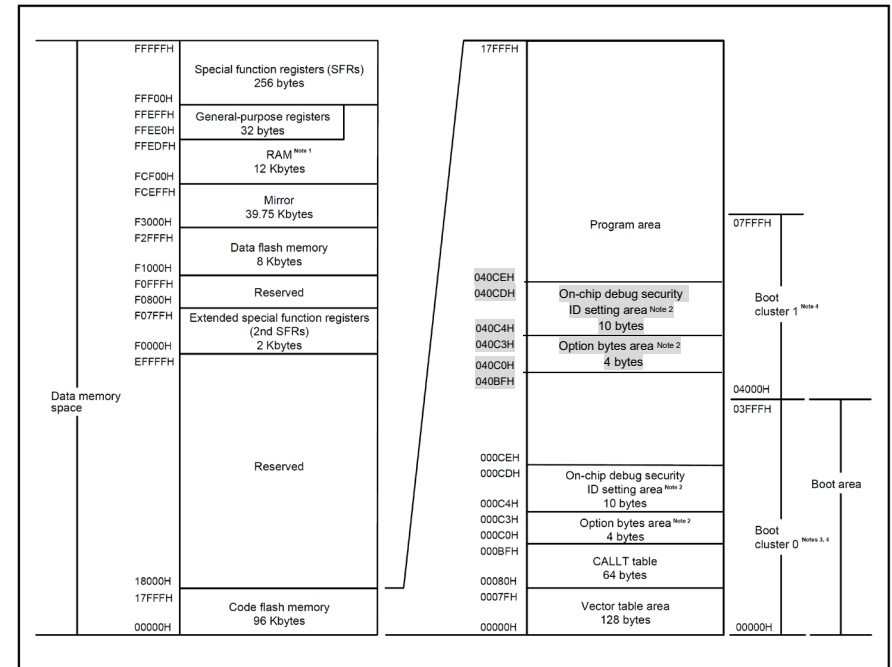
~~When boot swap is used:~~ Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Correct:

Products in the RL78/G23 can access a 1 MB address space. Figure 3 - 1 to Figure 3 - 3 show the memory maps.

Figure 3 - 1 Memory Map (R7F100GxF (x = A, B, C, E, F, G, J, L))



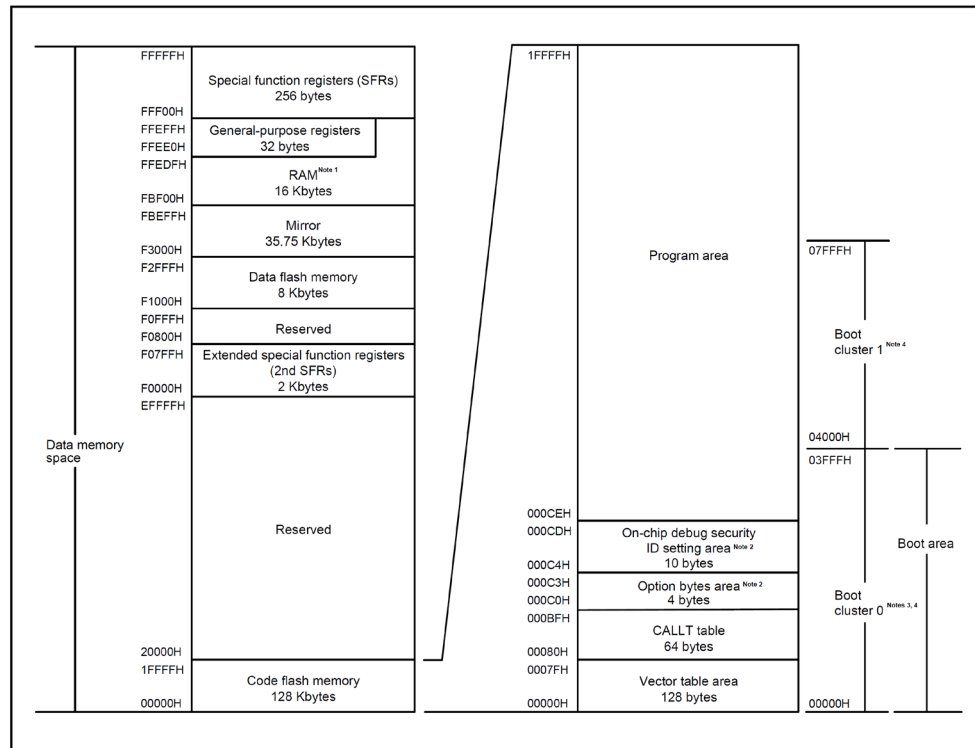
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 2 Memory Map (R7F100GxG (x = A, B, C, E, F, G, J, L, M, P))



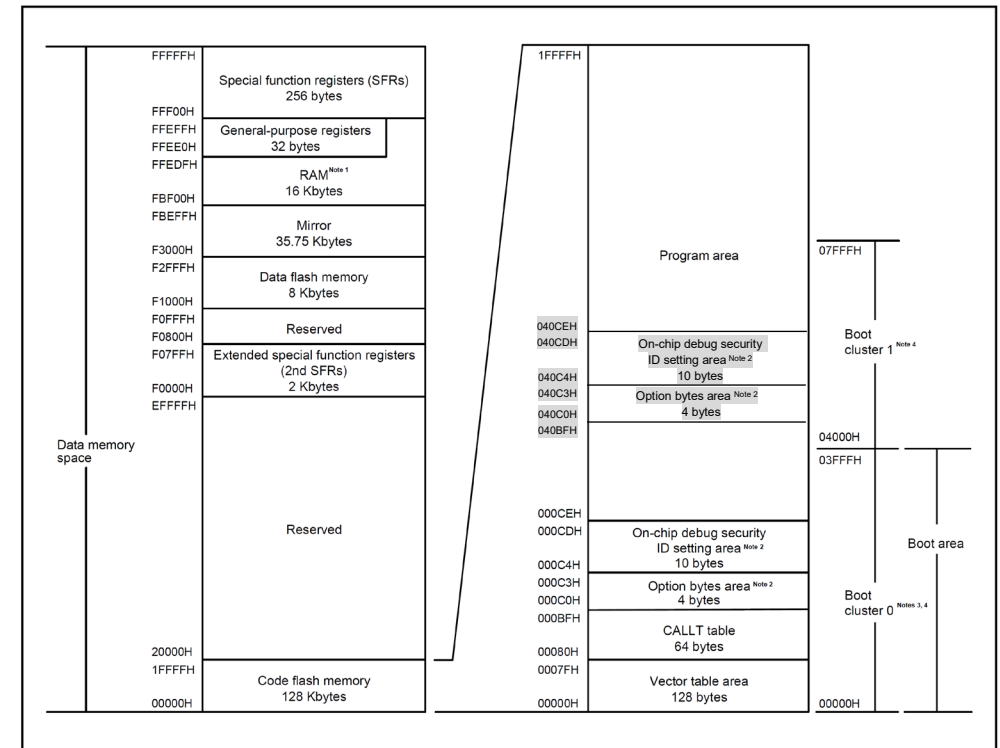
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 2 Memory Map (R7F100GxG (x = A, B, C, E, F, G, J, L, M, P))



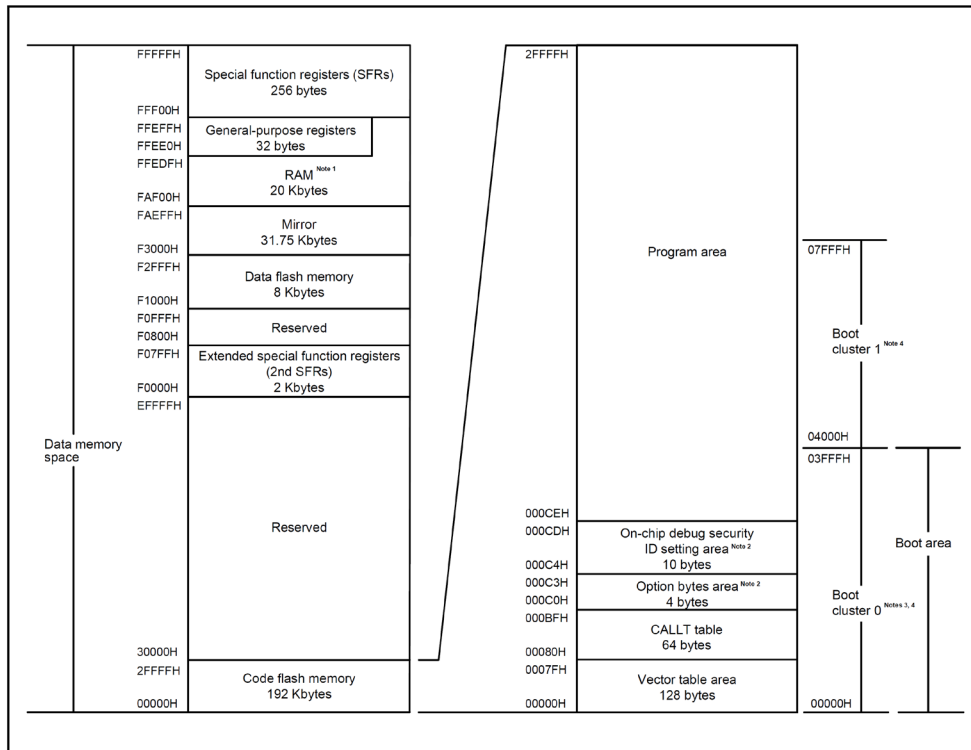
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1,** set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 3 Memory Map (R7F100GxH (x = A, B, C, E, F, G, J, L, M, P))



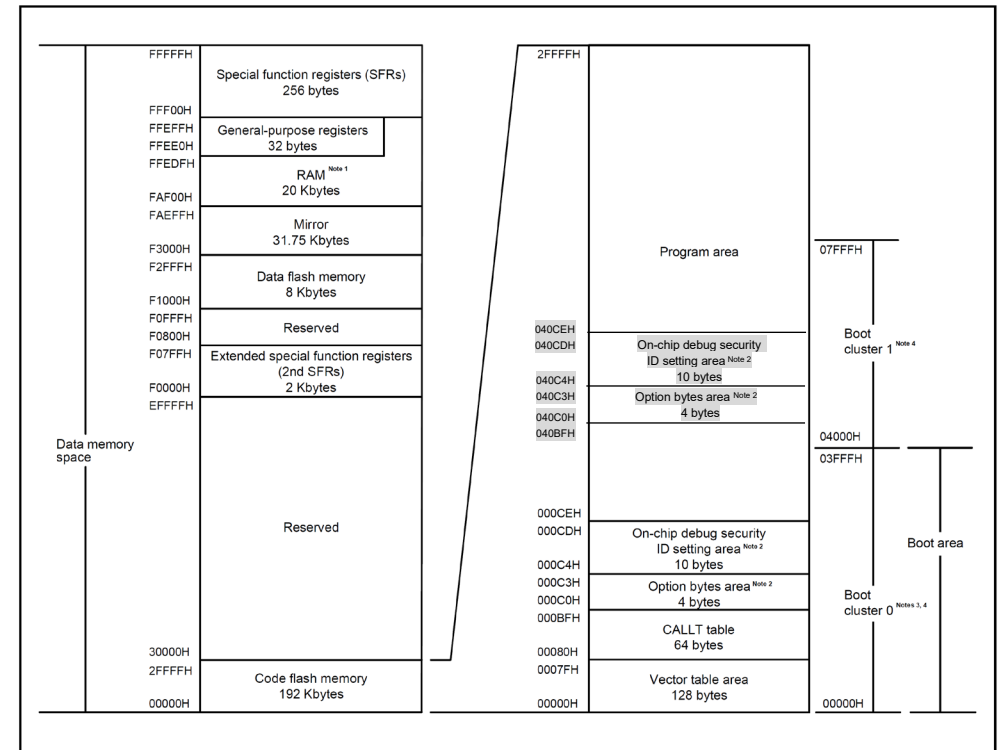
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 3 Memory Map (R7F100GxH (x = A, B, C, E, F, G, J, L, M, P))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

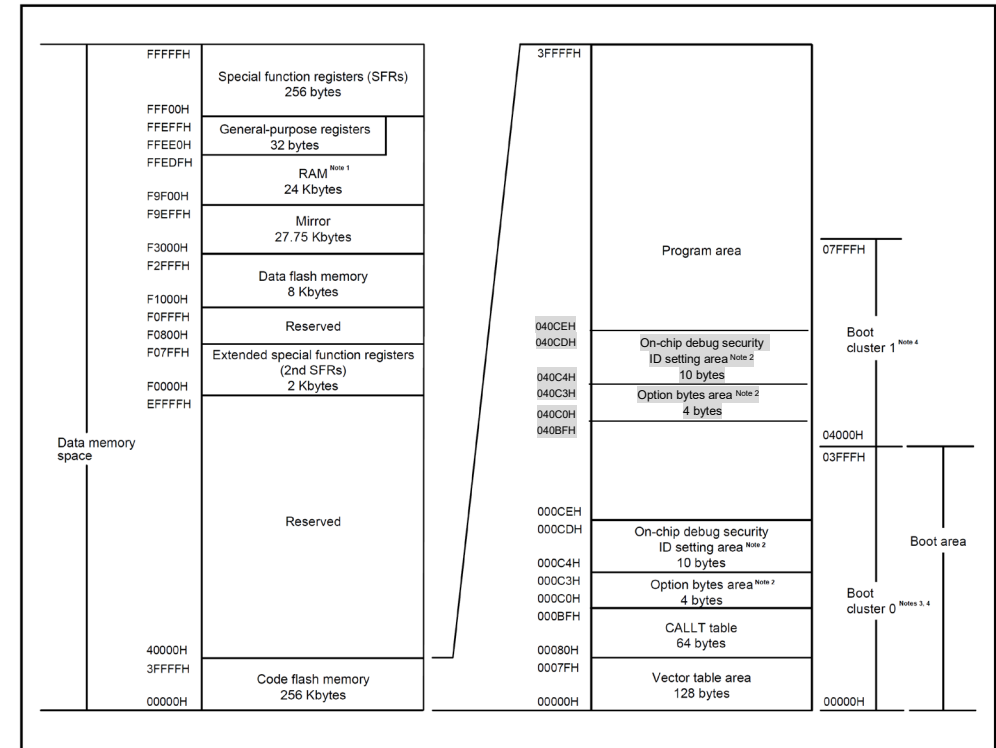
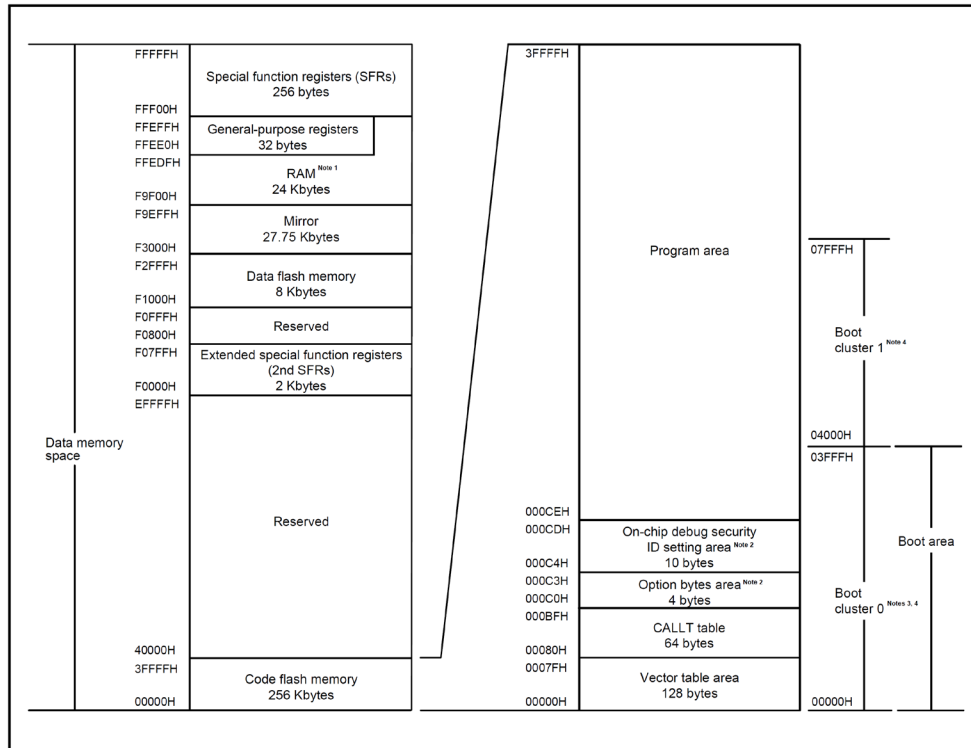
Note 2. **When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1,** set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 4 Memory Map (R7F100GxJ (x = A, B, C, E, F, G, J, L, M, P, S))

Figure 3 - 4 Memory Map (R7F100GxJ (x = A, B, C, E, F, G, J, L, M, P, S))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

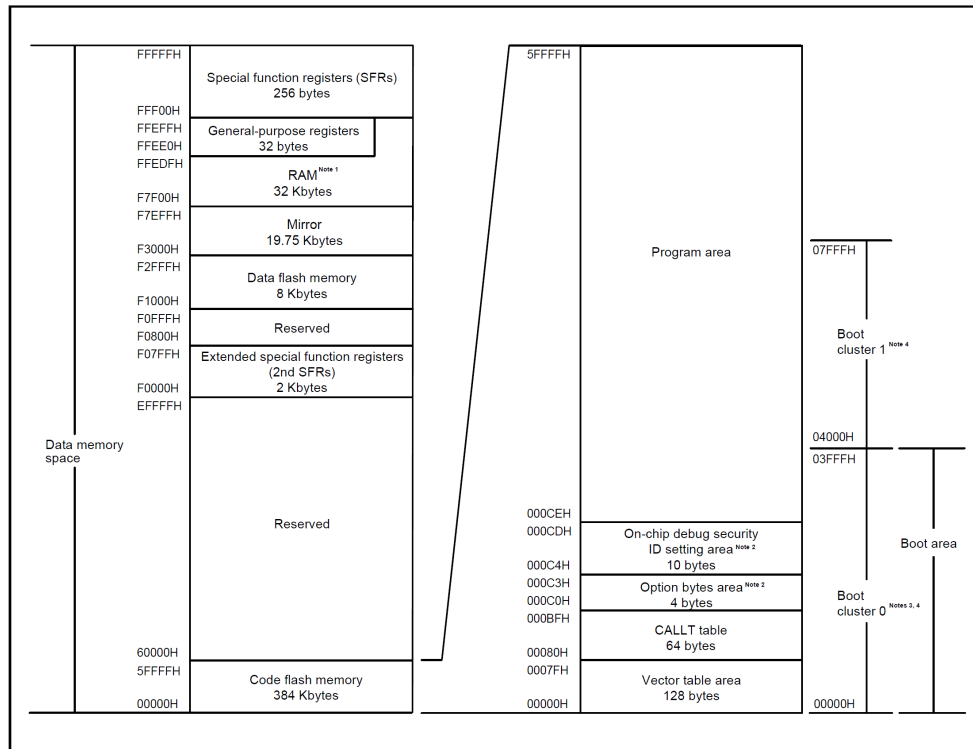
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1,** set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 5 Memory Map (R7F100GxK (x = F, G, J, L, M, P, S))



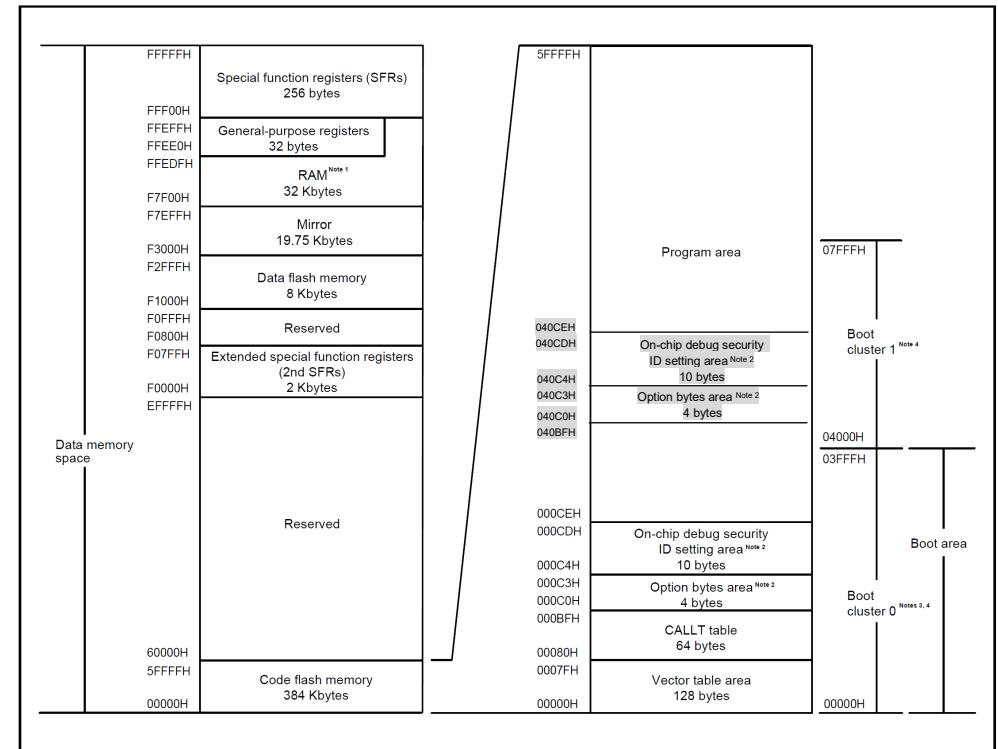
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 5 Memory Map (R7F100GxK (x = F, G, J, L, M, P, S))



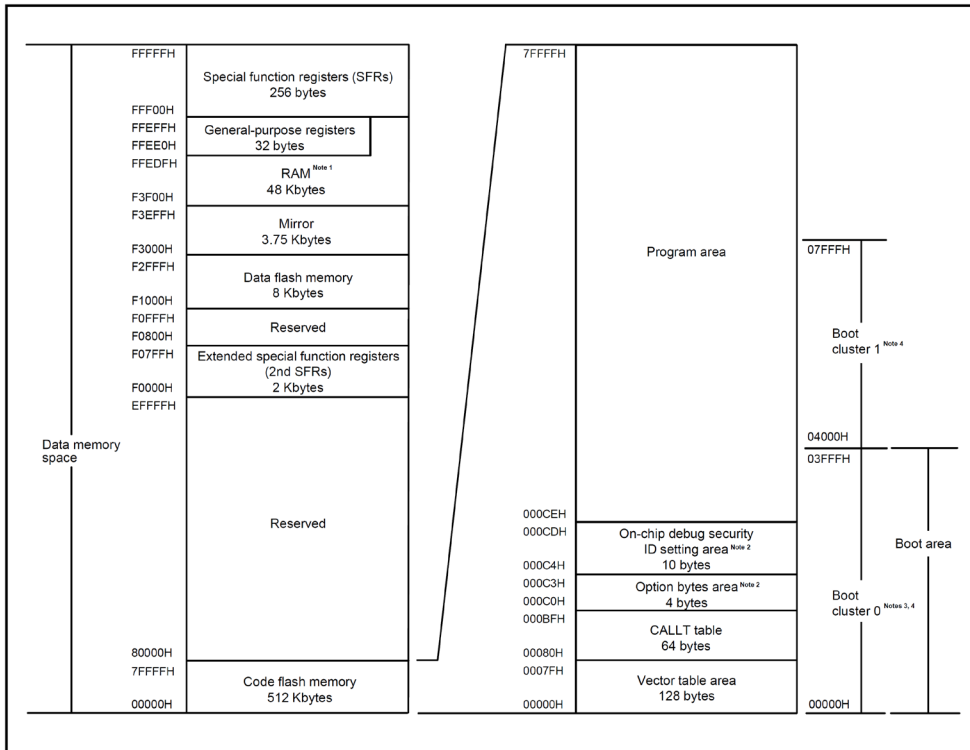
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1,** set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 6 Memory Map (R7F100GxL (x = F, G, J, L, M, P, S))



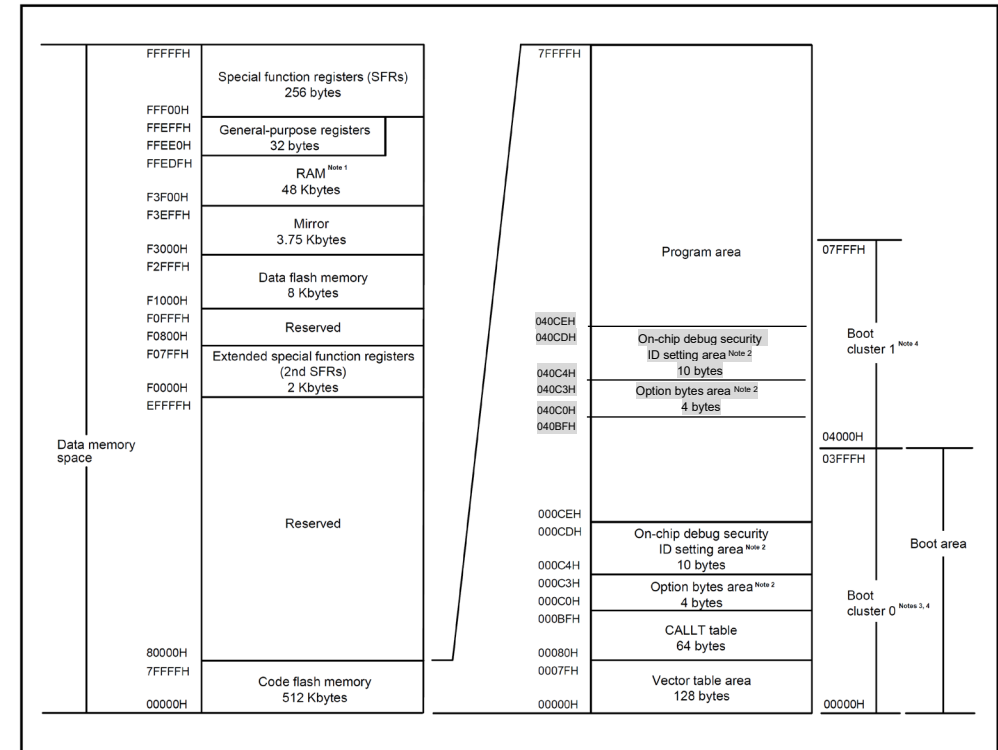
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 6 Memory Map (R7F100GxL (x = F, G, J, L, M, P, S))



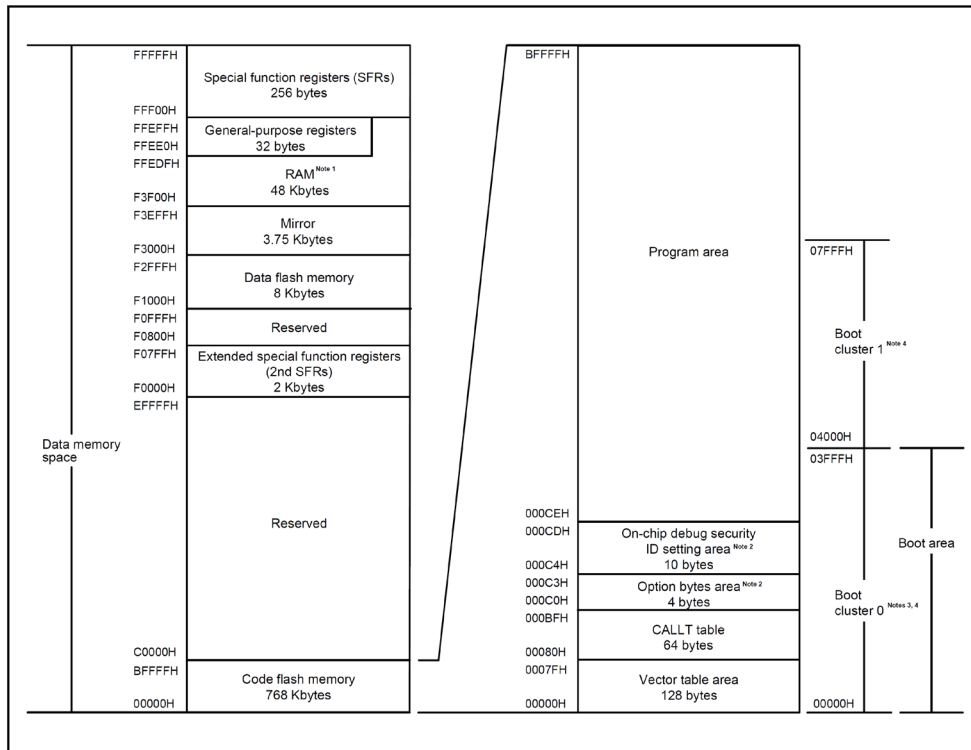
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1,** set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 7 Memory Map (R7F100GxN (x = F, G, J, L, M, P, S))



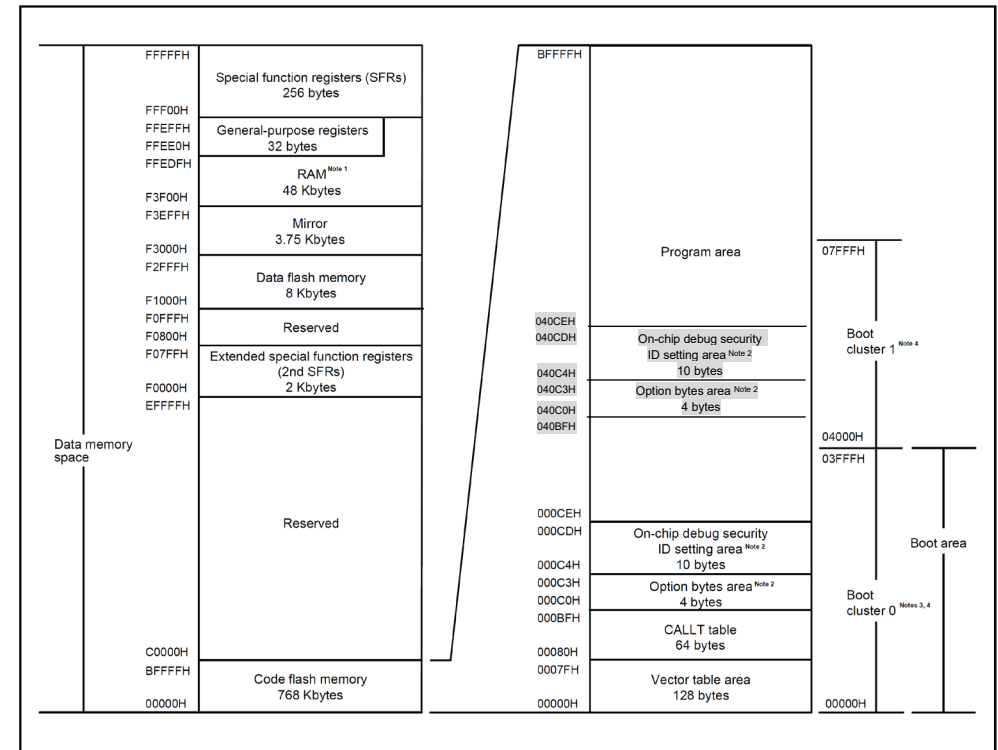
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 7 Memory Map (R7F100GxN (x = F, G, J, L, M, P, S))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1,** set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 160)

(omitted)

3. Option bytes area

A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when **the boot swap is used**. For details, see Section 32 Option Bytes.

4. On-chip debug security ID setting area

A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. **Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when the boot swap is not used and at 000C4H to 000CDH and at 040C4H to 040CDH when the boot swap is used**. For details, see Section 34 On-chip Debugging.

(omitted)

3. Option bytes area

A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when **boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0**. For details, see Section 32 Option Bytes.

4. On-chip debug security ID setting area

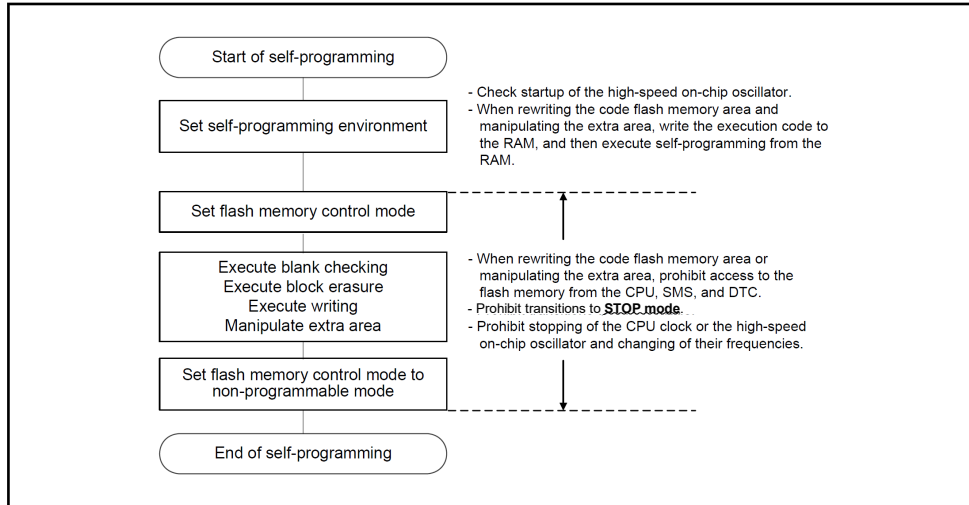
A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. **Set the 10-byte security ID for on-chip debugging at 000C4H to 000CDH when boot swapping is not to be used, that is, the value of the BTFLG bit in the FLSEC register is 1, and at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0**. For details, see Section 34 On-chip Debugging.

2. 33.6.1 Self-programming procedure (Page 1315)

Incorrect:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 33.6.2 Registers to control the flash memory.

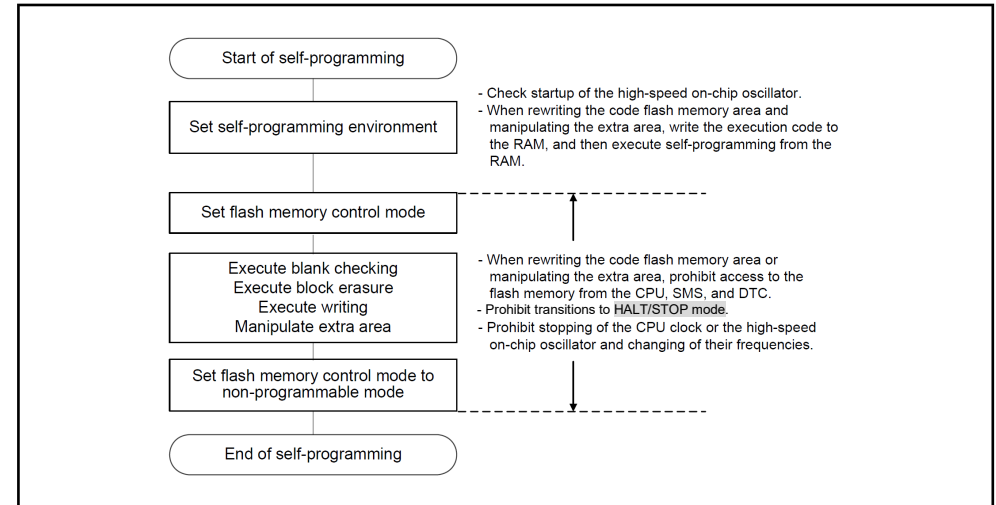
Figure 33 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



Correct:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 33.6.2 Registers to control the flash memory.

Figure 33 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



3. 33.10.1 Overview of the data flash memory (Page 1366)

Incorrect:

An overview of the data flash memory is provided below.

(omitted)

- Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.
- Transition to the **STOP mode** is prohibited while rewriting the data flash memory.

(omitted)

Correct:

An overview of the data flash memory is provided below.

(omitted)

- Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.
- Transition to the **HALT/STOP mode** is prohibited while rewriting the data flash memory.

(omitted)

4. 34.3 Security Settings for On-chip Debugging (Page 1369)

Incorrect:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 33.9 Security Settings in Section 33 Flash Memory).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 32 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.^{Note.1}

Table 34 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID code ^{Note 2}
040C4H to 040CDH	

Note 1. ~~The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.~~

Note 2. The setting FFFFFFFFFFFFFFFFFFH is not allowed.

Correct:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 33.9 Security Settings in Section 33 Flash Memory).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 32 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.^{Note}

Note The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.

Table 34 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID code ^{Note 2,3}
040C4H to 040CDH	

Note 1. The setting FFFFFFFFFFFFFFFFFFH is not allowed.

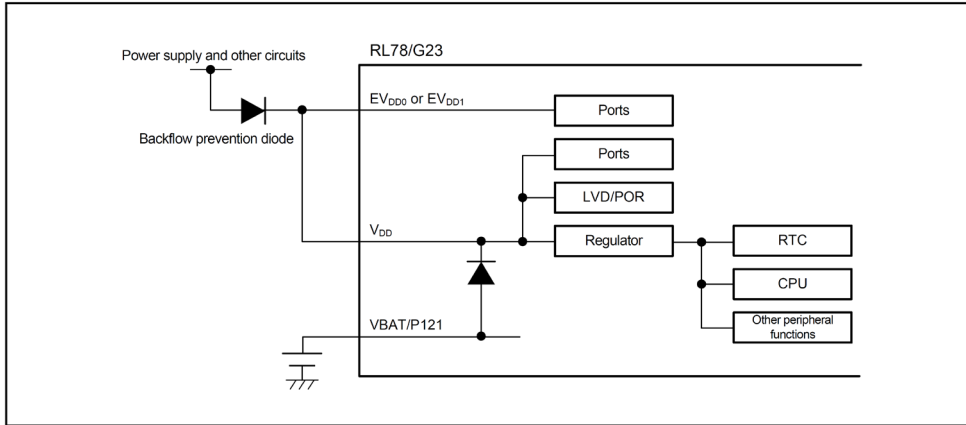
Note 2. Set the 10-byte security ID for on-chip debugging at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0.

5. **2.2.3.2 Connecting the VBAT pin to the battery for use in backing up (Page 106)**

Incorrect:

(omitted)

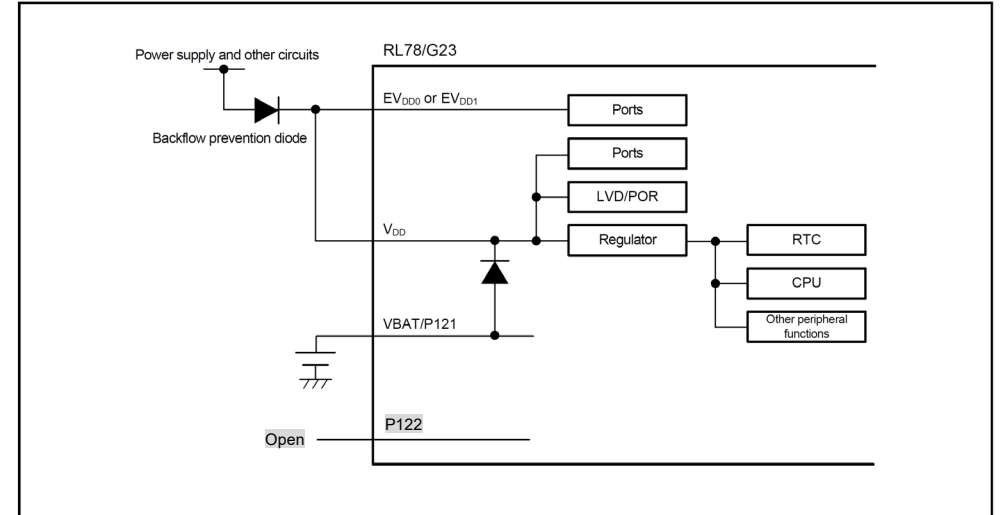
Figure 2 - 1 Example of the Connection of the VBAT Pin



Correct:

(omitted)

Figure 2 - 1 Example of the Connection of the VBAT Pin



6. 2.2.3.3 Using the VBAT pin (Page 107)

Incorrect:

How to make the initial settings for the VBAT pin and an example of the procedure for switching the power supply pin to the VBAT pin are described below. This processing is to be completed before the voltage on the VDD pin falls below that supplied from the VBAT pin. In addition, **Figure 2 - 2** shows the state transitions in switching the power supply pin between the VDD and VBAT pins.

1. Making the initial settings for the VBAT pin

Set the P121 pin to X1 oscillation mode (by setting the EXCLK and OSCSEL bits of the CMC register to 0 and 1, respectively, and the MSTOP bit of the CSC register to **0**) in the initial settings.

(omitted)

Correct:

How to make the initial settings for the VBAT pin and an example of the procedure for switching the power supply pin to the VBAT pin are described below. This processing is to be completed before the voltage on the VDD pin falls below that supplied from the VBAT pin. In addition, **Figure 2 - 2** shows the state transitions in switching the power supply pin between the VDD and VBAT pins.

1. Making the initial settings for the VBAT pin

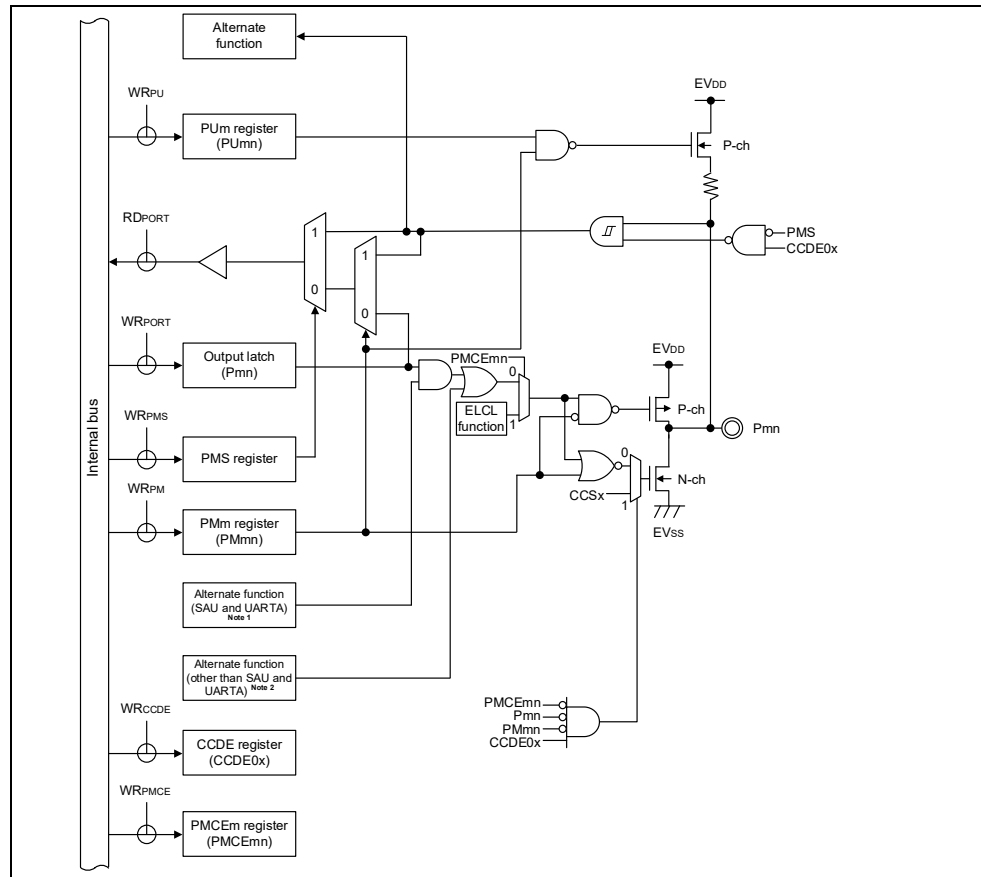
Set the P121 pin to X1 oscillation mode (by setting the EXCLK and OSCSEL bits of the CMC register to 0 and 1, respectively, and the MSTOP bit of the CSC register to **1**) in the initial settings.

(omitted)

7. 2.4 Block Diagrams of Pins (Page 125, Page 126, Page 132, Page 135, Page 138 to Page 141, Page 143 to Page 145)

Incorrect:
(Page 125)

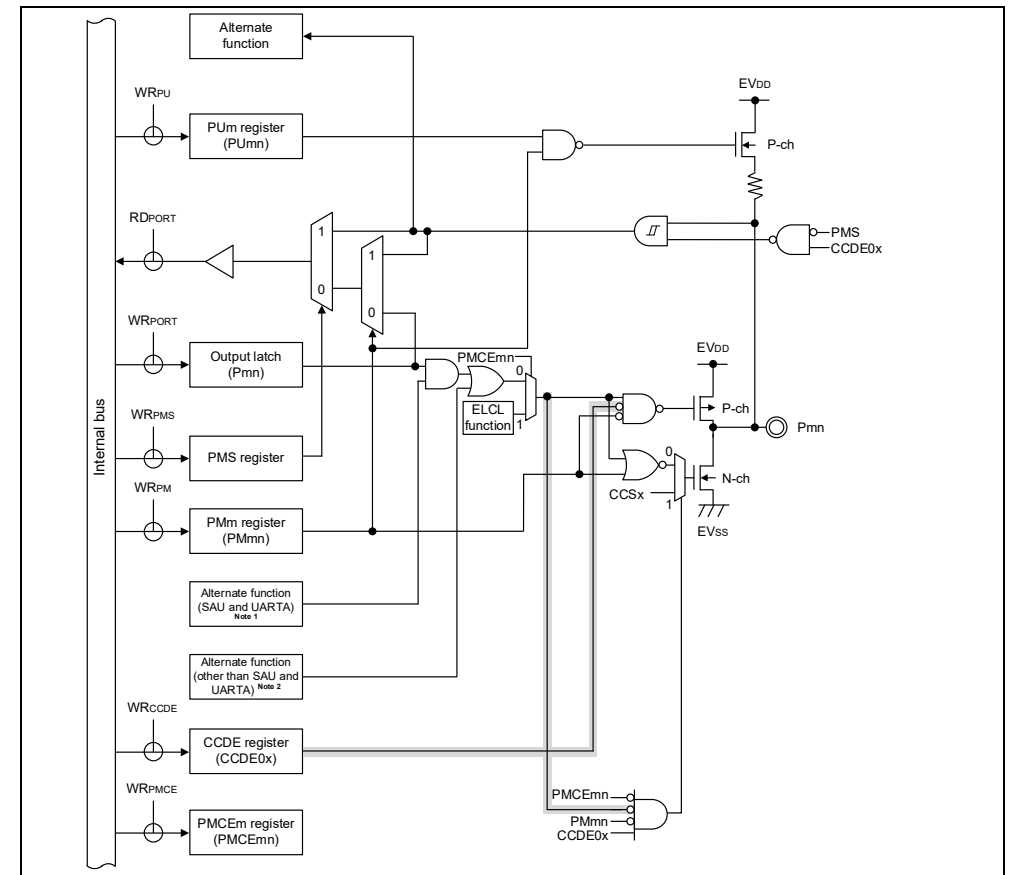
Figure 2 - 21 Pin Block Diagram for Pin Type 7-38-1



(omitted)

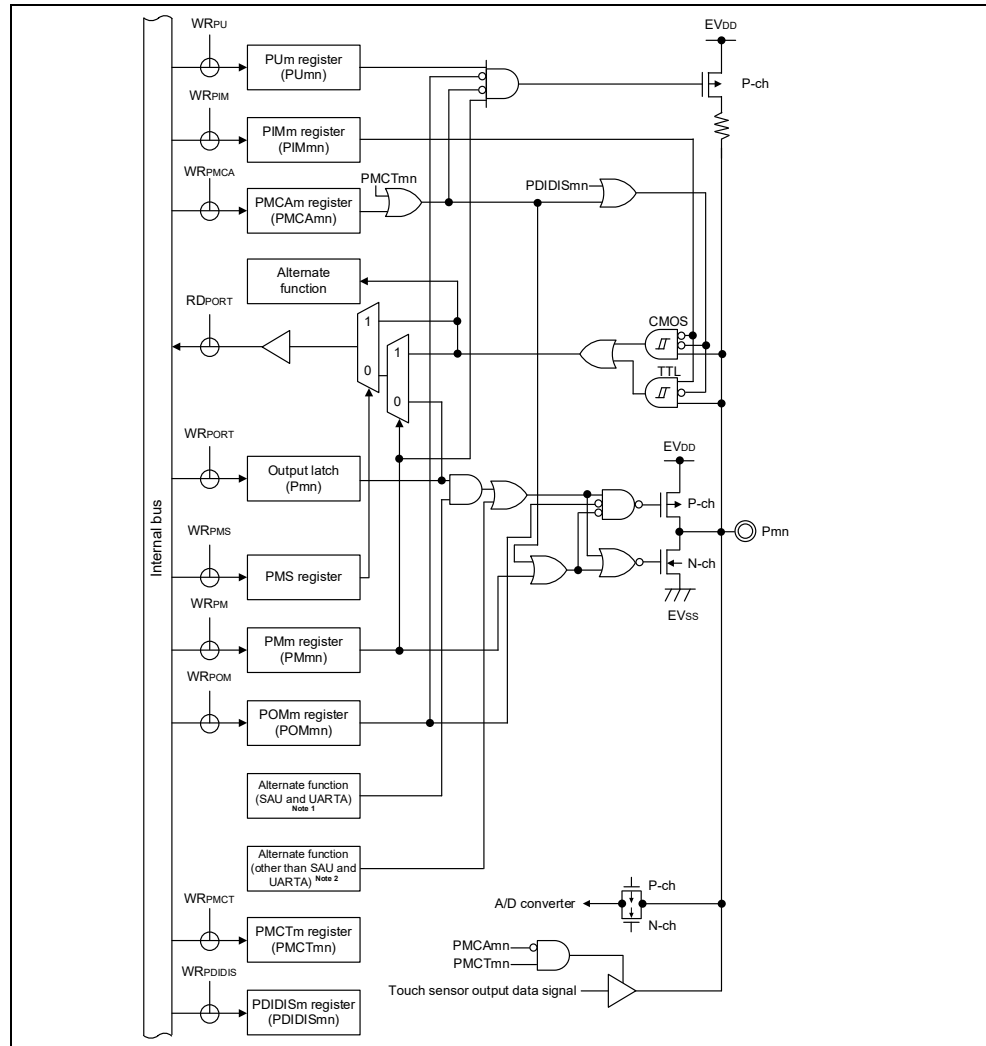
Correct:

Figure 2 - 21 Pin Block Diagram for Pin Type 7-38-1



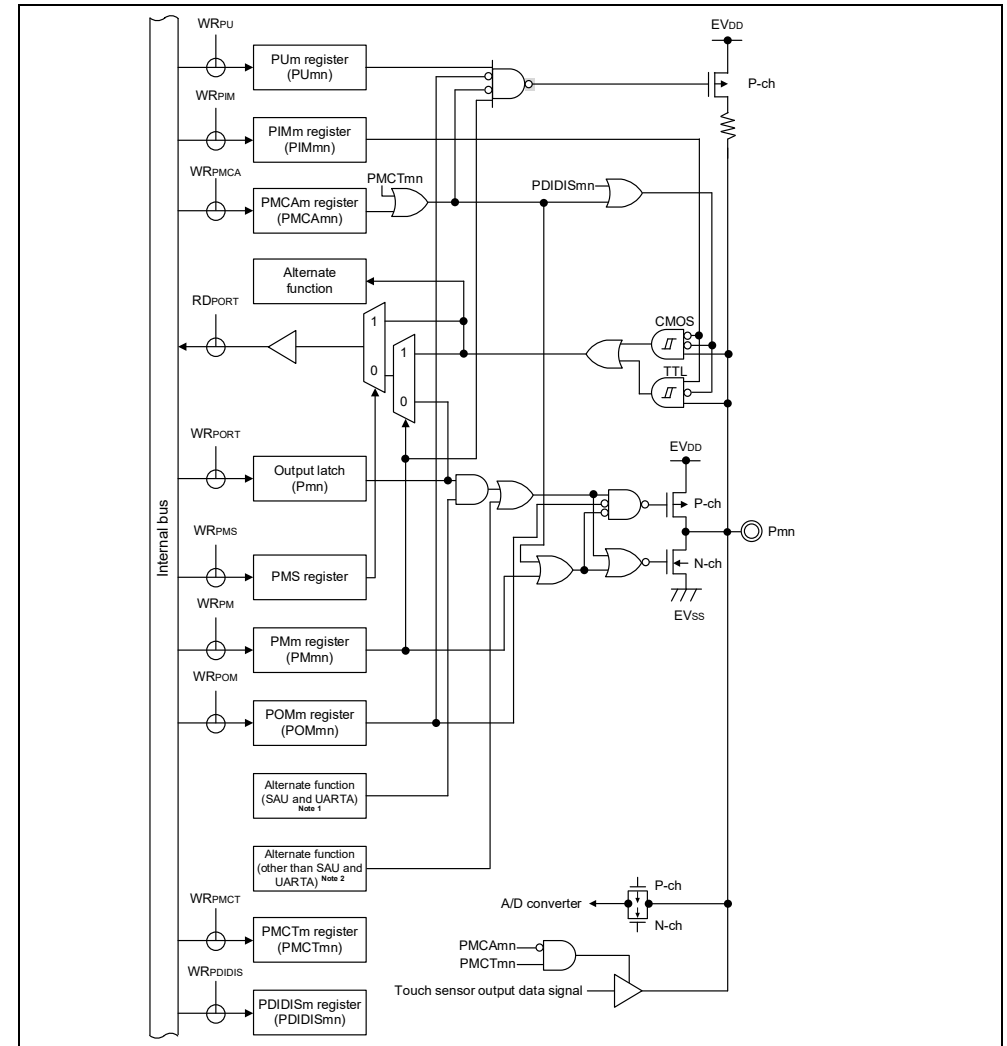
(omitted)

Figure 2 - 30 Pin Block Diagram for Pin Type 8-33-3



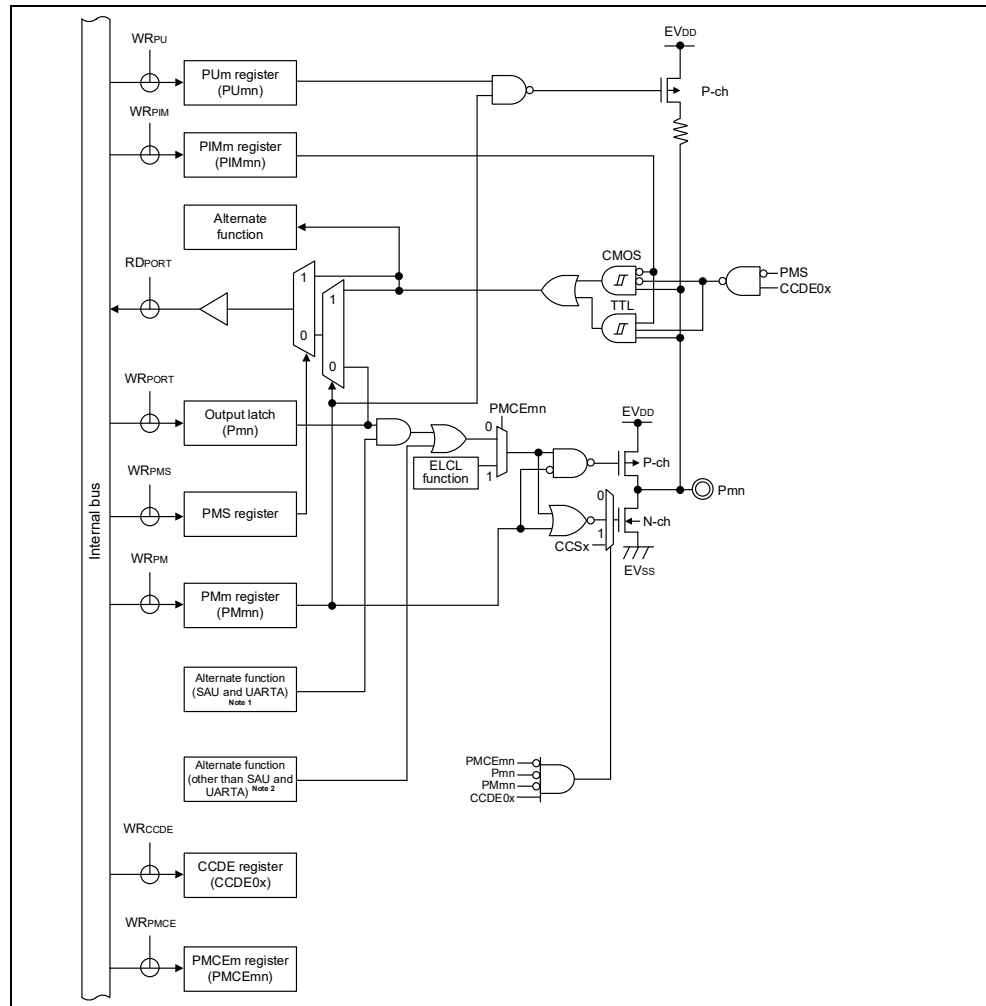
(omitted)

Figure 2 - 30 Pin Block Diagram for Pin Type 8-33-3



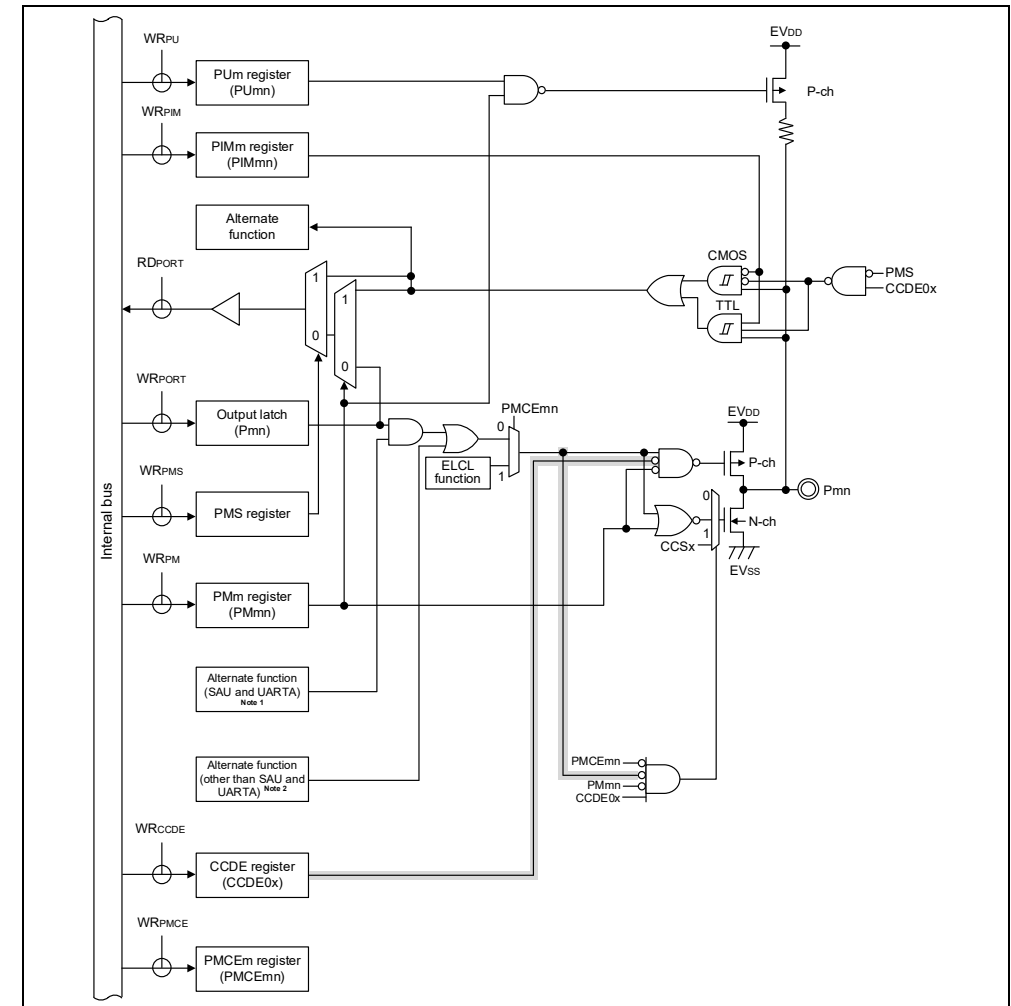
(omitted)

Figure 2 - 31 Pin Block Diagram for Pin Type 8-38-1



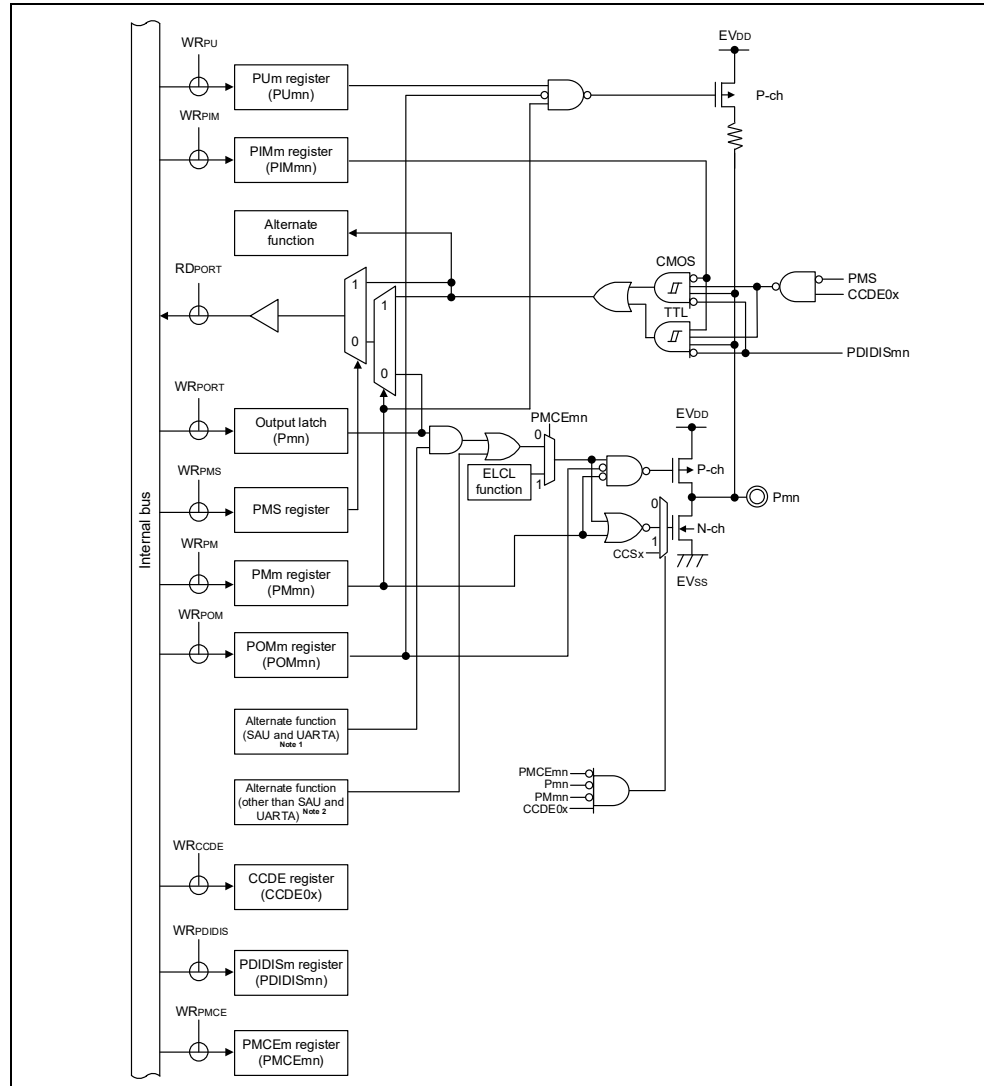
(omitted)

Figure 2 - 31 Pin Block Diagram for Pin Type 8-38-1



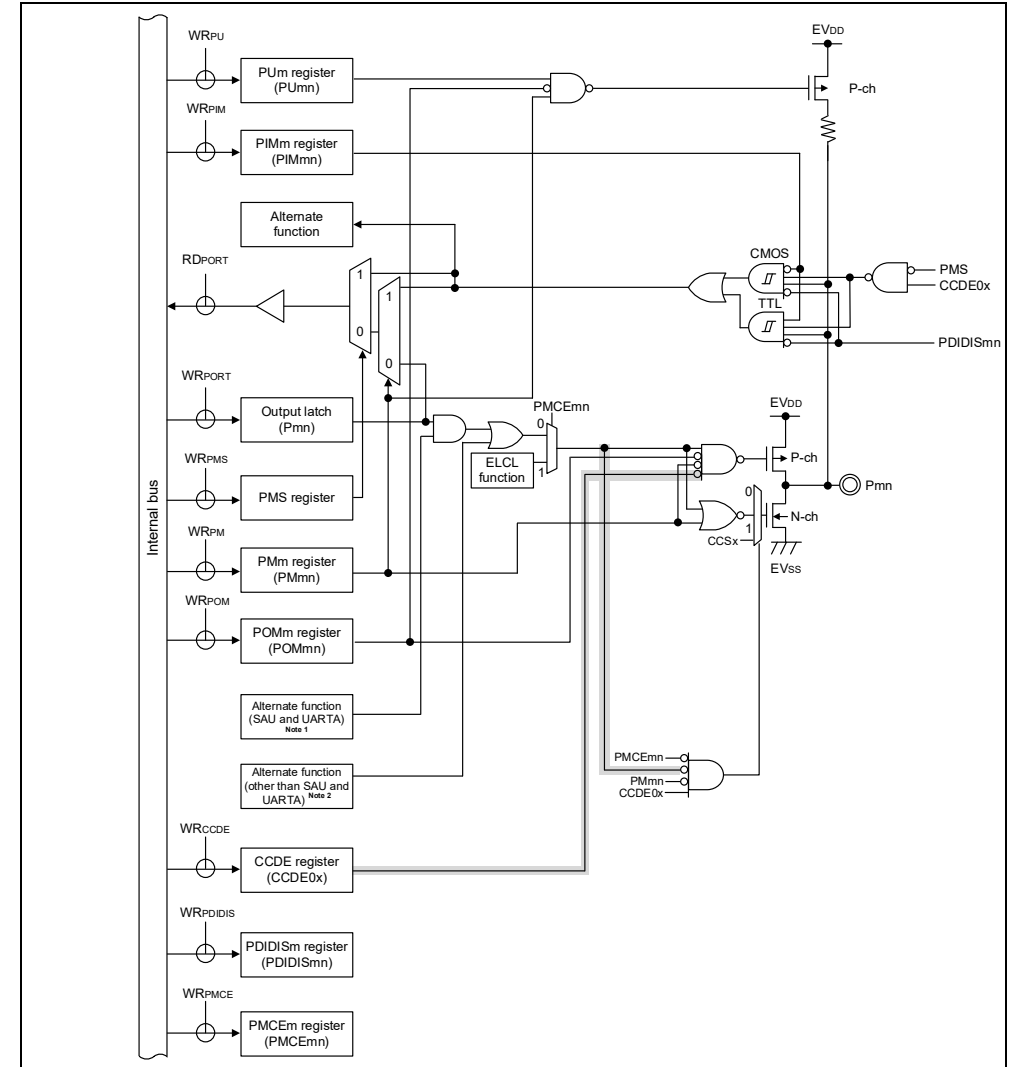
(omitted)

Figure 2 - 32 Pin Block Diagram for Pin Type 8-38-2



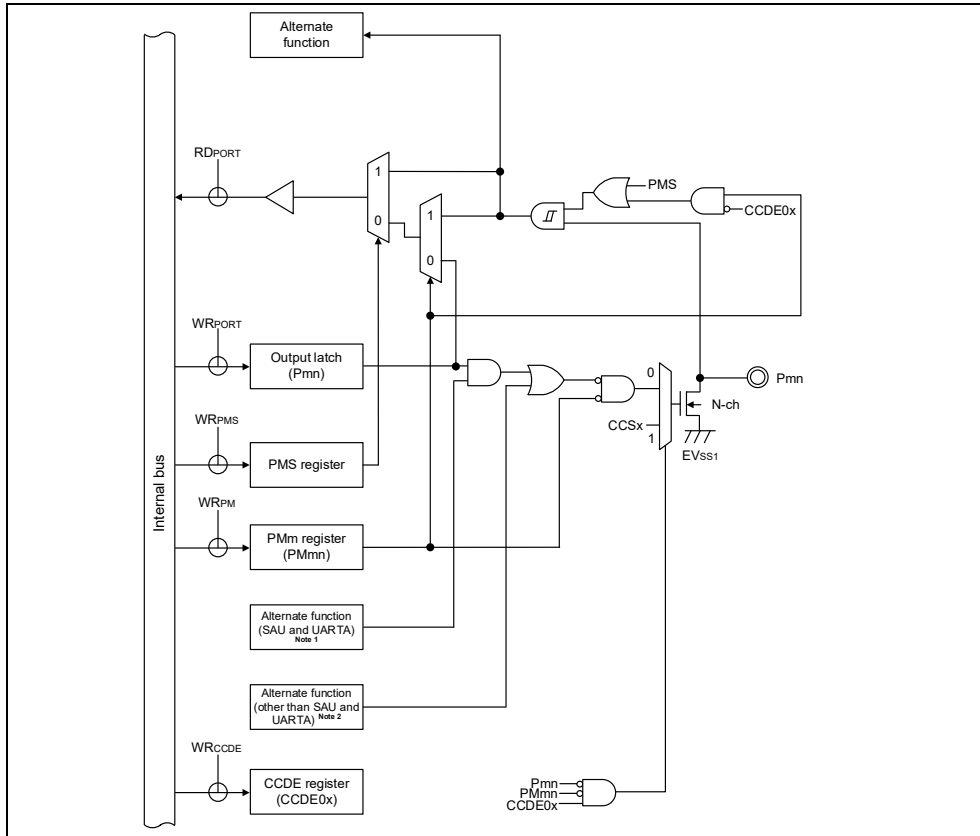
(omitted)

Figure 2 - 32 Pin Block Diagram for Pin Type 8-38-2



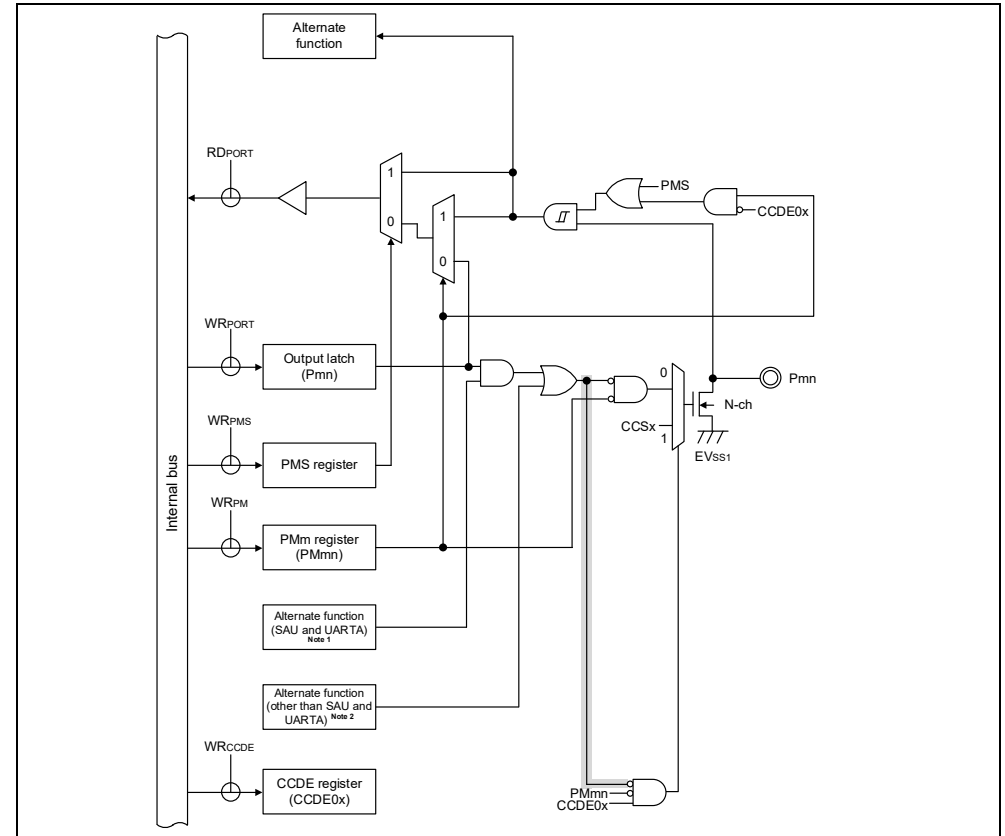
(omitted)

Figure 2 - 33 Pin Block Diagram for Pin Type 12-38-1



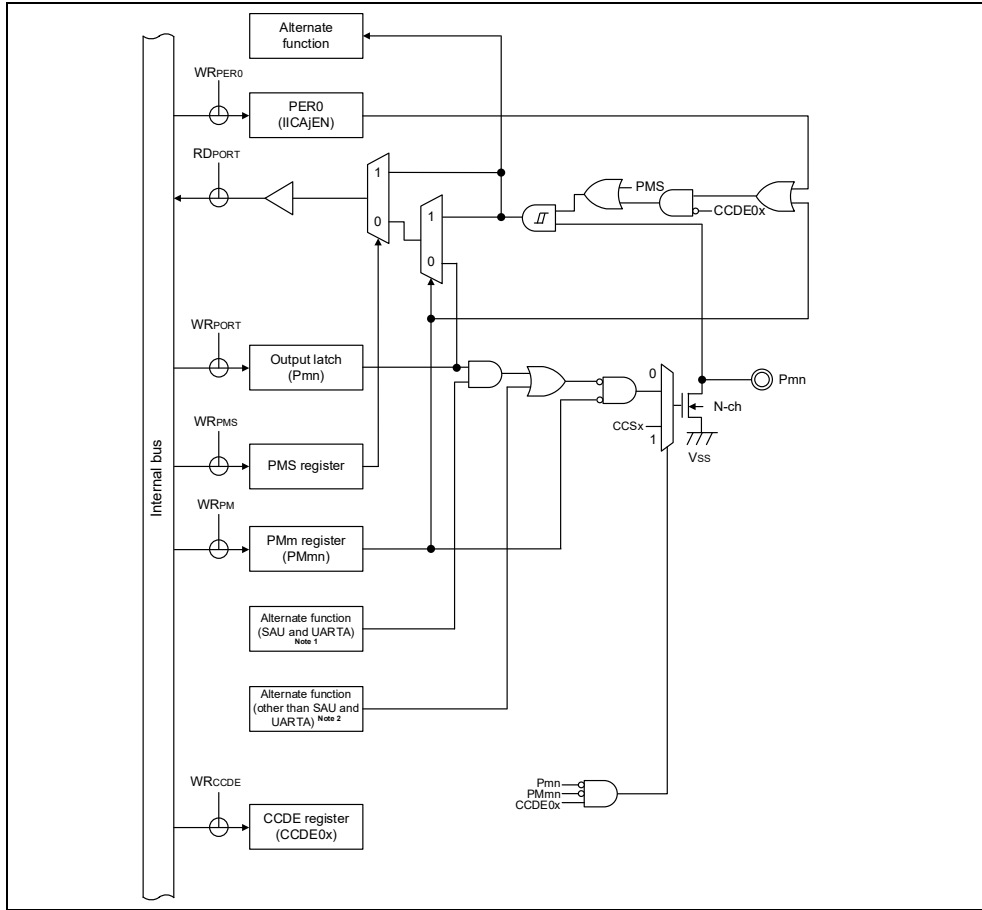
(omitted)

Figure 2 - 33 Pin Block Diagram for Pin Type 12-38-1



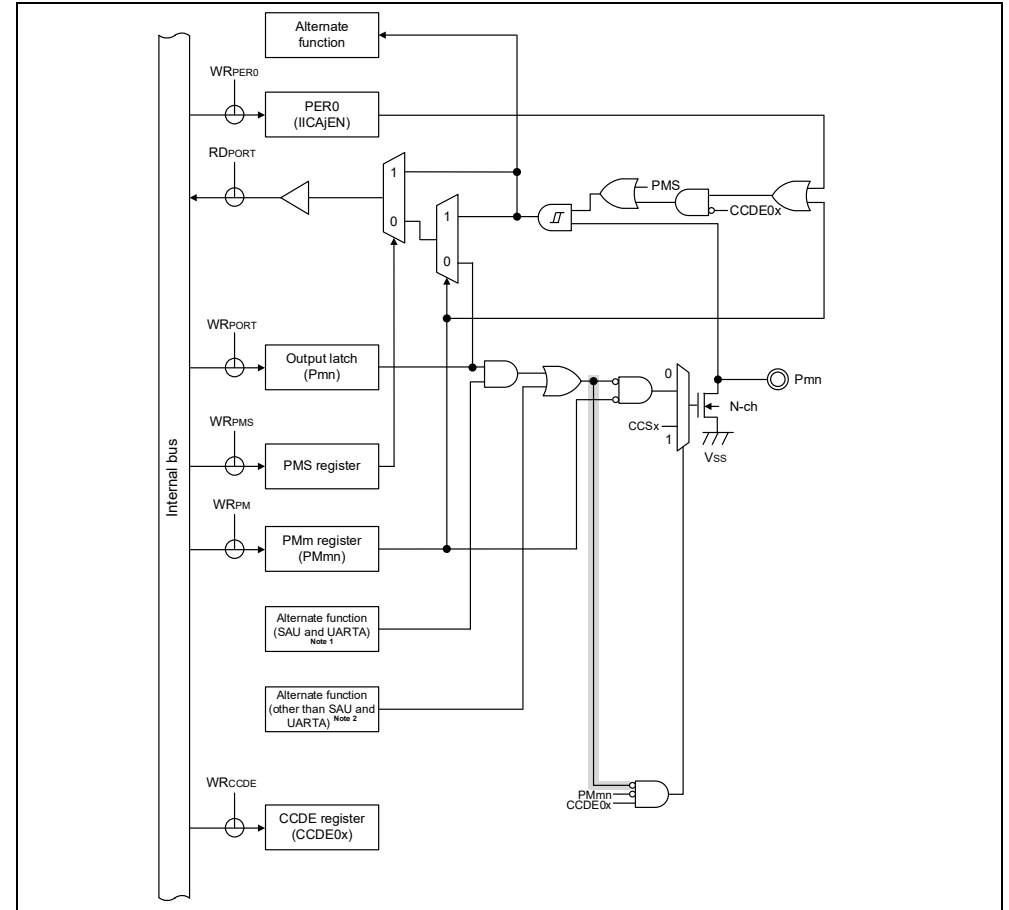
(omitted)

Figure 2 - 34 Pin Block Diagram for Pin Type 12-38-2



(omitted)

Figure 2 - 34 Pin Block Diagram for Pin Type 12-38-2



(omitted)

Figure 2 - 35 Pin Block Diagram for Pin Type 12-38-3

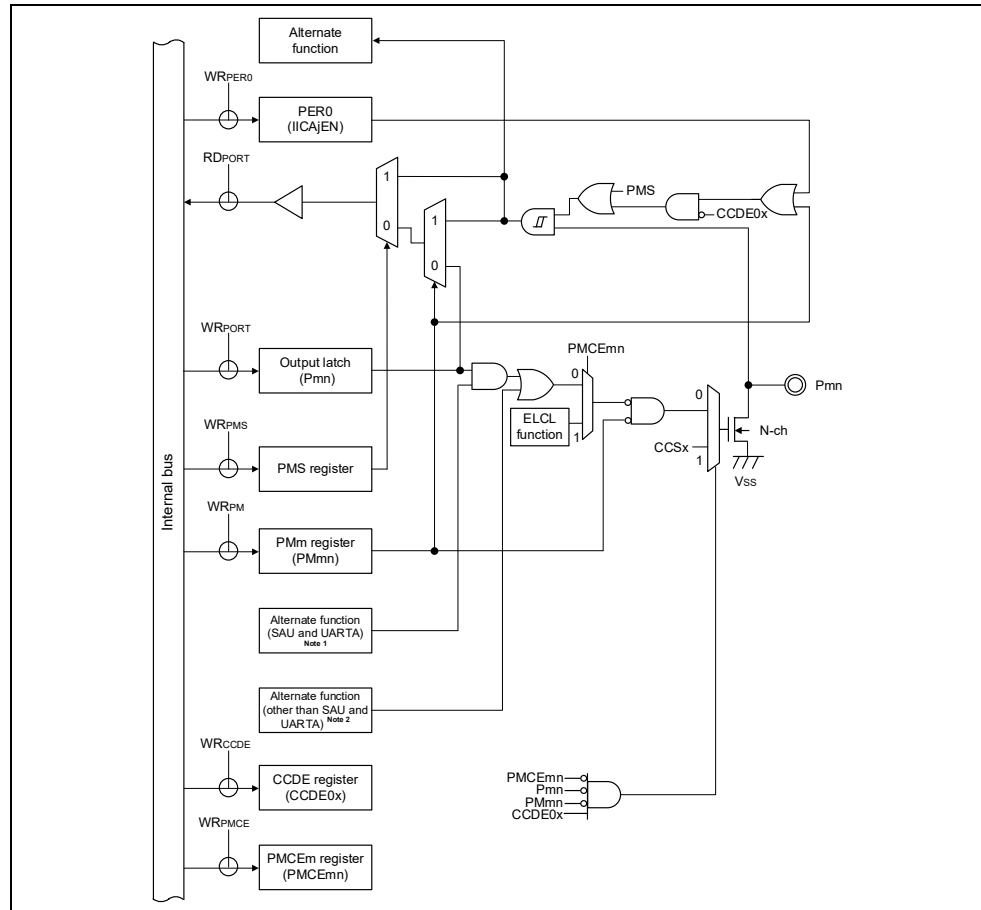
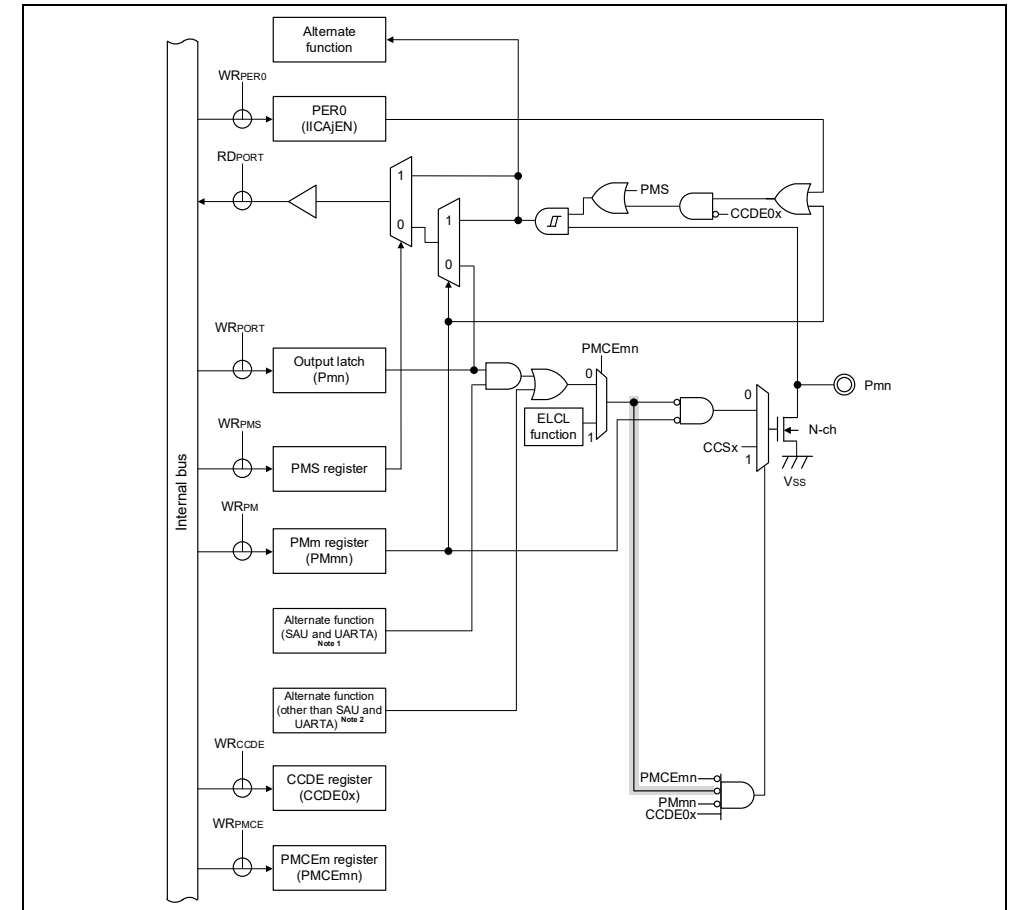


Figure 2 - 35 Pin Block Diagram for Pin Type 12-38-3



**8. 4.5.4 Examples of register settings for port and alternate functions
(Page 262, Page 281)**

Incorrect:
(Page 262)

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-pin to 64-pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (14/16)

Pin Name	Function Used		CMC					PMxx	Pxx	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin													
	Function Name	I/O	EXCLK, OSCSEL, EXCLKS, OSCSELS	XTSEL	EXCLK, OSCSEL, EXCLKS, OSCSELS	XTSEL																								
P121	P121	Input	00 xx / 10 xx / 11 xx	0	1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓													
			xx 00 / xx 10 / xx 11	1Note																										
		Output	00 xx / 10 xx / 11 xx	0														0	0/1											
			xx 00 / xx 10 / xx 11	1Note																										
	EI121	Input	00 xx / 10 xx / 11 xx	0														1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note																										
	VBAT	Input	00 xx / 10 xx / 11 xx	0														0	1	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
	X1	—	01 xx	0														1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
XT1	—	xx 01	1	1	x	✓	✓	✓	—	—	—	—	—	—	—	—														
	EXCLKS	Input	xx 11	0	—	x	—	—	—	✓	✓	✓	✓	✓	✓	✓														

Note This setting is only applicable in the 30- to 36-pin products.

(omitted)

Correct:

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-pin to 64-pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (14/16)

Pin Name	Function Used		CMC					PMxx	Pxx	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin													
	Function Name	I/O	EXCLK, OSCSEL, EXCLKS, OSCSELS	XTSEL	EXCLK, OSCSEL, EXCLKS, OSCSELS	XTSEL																								
P121	P121	Input	00 xx / 10 xx / 11 xx	0	1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓													
			xx 00 / xx 10 / xx 11	1Note																										
		Output	00 xx / 10 xx / 11 xx	0														0	0/1											
			xx 00 / xx 10 / xx 11	1Note																										
	EI121	Input	00 xx / 10 xx / 11 xx	0														1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note																										
	VBAT	Input	01 xx	0														1	x	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
	X1	—	01 xx	0														1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
XT1	—	xx 01	1	1	x	✓	✓	✓	—	—	—	—	—	—	—	—														
	EXCLKS	Input	xx 11	0	—	x	—	—	—	✓	✓	✓	✓	✓	✓	✓														

Note This setting is only applicable in the 30- to 36-pin products.

(omitted)

(Page 281)

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-pin and 100-pin Products with 128-Kbyte Flash Memory) (18/21)

Pin Name	Function Used		CMC				PMxx	Pxx	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin		
	Function Name	I/O	EXCLK, OSCSEL, EXCLKS, OSCSELS	XTSEL																	
P121	P121	Input	00 xx / 10 xx / 11 xx	0	1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
			xx 00 / xx 10 / xx 11	1Note																	
	Output	00 xx / 10 xx / 11 xx	0	0	0/1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		xx 00 / xx 10 / xx 11	1Note																		
	EI121	Input	00 xx / 10 xx / 11 xx	0	1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note																	
VBAT	Input	00 xx / 10 xx / 11 xx	0	0	0	1	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
X1	—	01 xx	0	1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
XT1	—	xx 01	1	1	x	✓	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—	

	EXCLKS	Input	xx 11	0	—	x	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
--	--------	-------	-------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Note This setting is only applicable in the 30- to 36-pin products.

(omitted)

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-pin and 100-pin Products with 128-Kbyte Flash Memory) (18/21)

Pin Name	Function Used		CMC				PMxx	Pxx	30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin		
	Function Name	I/O	EXCLK, OSCSEL, EXCLKS, OSCSELS	XTSEL																	
P121	P121	Input	00 xx / 10 xx / 11 xx	0	1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
			xx 00 / xx 10 / xx 11	1Note																	
	Output	00 xx / 10 xx / 11 xx	0	0	0/1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
		xx 00 / xx 10 / xx 11	1Note																		
	EI121	Input	00 xx / 10 xx / 11 xx	0	1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
			xx 00 / xx 10 / xx 11	1Note																	
VBAT	—	01 xx	0	0	1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
X1	—	01 xx	0	1	x	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
XT1	—	xx 01	1	1	x	✓	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—	

	EXCLKS	Input	xx 11	0	—	x	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
--	--------	-------	-------	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Note This setting is only applicable in the 30- to 36-pin products.

(omitted)

9. 12.3.8 Analog input channel specification register (ADS) (Page 574)

Incorrect:

(omitted)

- Caution 7. When the setting of the ADISS bit is 1, the internal reference voltage cannot be used for the + side reference voltage. After the ADISS bit is set to 1, the initial conversion result cannot be used. For the setting flow, see 12.7.5 Example of using the ADC when selecting the temperature sensor output voltage or internal reference voltage, and software trigger no-wait mode and one-shot conversion mode. For details about the internal reference voltage, see Section 37 Electrical Characteristics.
- Caution 8. Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in 37.3.2 Supply current characteristics will be added.
- Caution 9. When the setting of the ADISS bit is 1, the hardware trigger wait mode and one-shot conversion mode cannot be used at the same time.

Correct:

(omitted)

- Caution 7. When the setting of the ADISS bit is 1, the internal reference voltage cannot be used for the + side reference voltage. After the ADISS bit is set to 1, the initial conversion result cannot be used. For the setting flow, see 12.7.5 Example of using the ADC when selecting the temperature sensor output voltage or internal reference voltage, and software trigger no-wait mode and one-shot conversion mode. For details about the internal reference voltage, see Section 37 Electrical Characteristics.
- Caution 8. Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in 37.3.2 Supply current characteristics will be added.
- Caution 9. When the setting of the ADISS bit is 1, the hardware trigger wait mode and one-shot conversion mode cannot be used at the same time.
- Caution 10. When the setting of the ADISS bit is 1, the software trigger wait mode and one-shot conversion mode cannot be used at the same time.

10. 12.6.6 Software trigger wait mode (select mode, one-shot conversion mode) (Page 586)

Incorrect:

(omitted)

Caution When <5> or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

(omitted)

Caution 1. When <5> or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Caution 2. The setting of ADISS being 1 (the input source is temperature sensor output voltage or internal reference voltage) cannot be used in the software trigger wait mode (one-shot conversion mode).

11. 15.3.8 Serial status register mn (SSRmn) (Page 666)

Incorrect:

(omitted)

Note 1. SSR00 to SSR03, SSR10, and SSR11 are present in all products.
SSR12 and SSR13 are only present in the 80- to 128-pin products.

Note 2. This bit is only present in the SSR01, SSR03, SSR11, and SSR13 registers.

Caution 1. If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVFmn = 1) is detected.

Caution 2. When the simplified SPI (CSI) is handling reception in the SNOOZE mode (SWCm = 1), the OVFmn flag will not change.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Correct:

(omitted)

Note 1. SSR00 to SSR03, SSR10, and SSR11 are present in all products.
SSR12 and SSR13 are only present in the 80- to 128-pin products.

Note 2. This bit is only present in the SSR01, SSR03, SSR11, and SSR13 registers.

Caution 1. If data is written to the SDRmn register when BFFmn = 1, the transmit/receive data stored in the register is discarded and an overrun error (OVFmn = 1) is detected.

Caution 2. When the simplified SPI (CSI) is handling reception in the SNOOZE mode (SWCm = 1), the OVFmn and BFFmn flags will not change.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

12. 15.3.13 Serial output register m (SOm) (Page 671)

Incorrect:

Address: F0168H, F0169H (SO1)
 After reset: 0F0FH^{Note}
 R/W: R/W

Symbol	15	14	13	12	11	10	9	8
SO1	0	0	0	0	CKO13	CKO12	CKO11	CKO10
	7	6	5	4	3	2	1	0
	0	0	0	0	SO13	SO12	SO11	SO10
CKOmn	Serial clock output of channel n							
0	Serial clock output value is 0.							
1	Serial clock output value is 1.							
SOmn	Serial data output of channel n							
0	Serial data output value is 0.							
1	Serial data output value is 1.							

Note In the 30- to 64-pin products, the value of the SO1 register is 0303H following a reset.

Caution Be sure to clear bits 15 to 12 and 7 to 4 of the SO0 register to 0. Be sure to clear bits 15 to 10 and 7 to 2 of the SO1 register for 30- to 64-pin products and bits 15 to 12 and 7 to 4 of the SO1 register for 80- to 128-pin products to 0.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Correct:

Address: F0168H, F0169H (SO1)
 After reset: 0F0FH^{Note}
 R/W: R/W

Symbol	15	14	13	12	11	10	9	8
SO1	0	0	0	0	CKO13	CKO12	CKO11	CKO10
	7	6	5	4	3	2	1	0
	0	0	0	0	SO13	SO12	SO11	SO10
CKOmn	Serial clock output of channel n							
0	Serial clock output value is 0.							
1	Serial clock output value is 1.							
SOmn	Serial data output of channel n							
0	Serial data output value is 0.							
1	Serial data output value is 1.							

Note In the 30- to 64-pin products with the ROM of no more than 128 Kbytes, the value of the SO1 register is 0303H following a reset.

Caution Be sure to clear bits 15 to 12 and 7 to 4 of the SO0 register to 0. Be sure to clear bits 15 to 10 and 7 to 2 of the SO1 register for 30- to 64-pin products with the ROM of no more than 128 Kbytes and bits 15 to 12 and 7 to 4 of the SO1 register for 80- to 128-pin products to 0.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

13. 17.3.4 Baud Rate Generator (Page 943)

Incorrect:

After the start bit is detected, the latch timing of receive data is determined by the counter specified with the baud rate generator control register (BRGCAn). If the whole frame including the stop bit has been received before this latching, reception can proceed correctly. Assuming that 11 bits of data are received, the theoretical values can be calculated as follows.

- The relation between 1-bit data length and baud rate

$$FL = (\text{Brate}) - 1$$

Brate: Baud rate of UART

k: Set value of BRGCAn register

FL: 1-bit data length

Margin of latch timing: 1 clock

- Minimum permissible data frame length (FLmin)

$$FL_{\min} = 11 \times FL - \frac{k-1}{2k} \times FL = \frac{21k+1}{2k} FL$$

- Maximum permissible baud rate for reception on the transmitting side (BRmax)

$$BR_{\max} = (FL_{\min}/11)^{-1} = \frac{22k}{21k+1} \text{ Brate}$$

- Maximum permissible data frame length (FLmax)

$$FL_{\max} = \frac{21k+1}{20k} FL \times 11$$

- Minimum permissible baud rate for reception on the transmitting side (BRmin)

$$BR_{\min} = (FL_{\max}/11)^{-1} = \frac{20k}{21k-1} \text{ Brate}$$

Table 17 - 5 shows the permissible baud rate error between UART and the transmitting side can be calculated from the above minimum and maximum baud rate expressions.

Table 17 - 5 Maximum/Minimum Permissible Baud Rate Error

Division ratio (k)	Maximum permissible baud rate error	Minimum permissible baud rate error
2	+2.32%	-2.43%
4	+3.52%	-3.61%
8	+4.14%	-4.19%
20	+4.51%	-4.53%
50	+4.66%	-4.67%
100	+4.71%	-4.71%
255	+4.74%	-4.74%

Remark 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the division ratio (k), the higher the permissible error.

Remark 2. k: Set value of BRGCAn register

Correct:

After the start bit is detected, the latch timing of receive data is determined by the counter specified with the baud rate generator control register (BRGCAn). If the whole frame including the stop bit has been received before this latching, reception can proceed correctly. Assuming that 11 bits of data are received, the theoretical values can be calculated as follows.

- The relation between 1-bit data length and baud rate

$$FL = (\text{Brate}) - 1$$

Brate: Baud rate of UART

k: Set value of BRGCAn register

FL: 1-bit data length

Margin of latch timing: 2 clock

- Minimum permissible data frame length (FLmin)

$$k = 3 \text{ to } 255: FL_{\min} = 11 \times FL - \frac{k-2}{2k} \times FL = \frac{21k+2}{2k} FL$$

- Maximum permissible baud rate for reception on the transmitting side (BRmax)

$$k = 2: BR_{\max} = \text{Brate} + \frac{1}{22k} \text{ Brate}$$

$$k = 3 \text{ to } 255: BR_{\max} = (FL_{\min}/11)^{-1} = \frac{22k}{21k+2} \text{ Brate}$$

- Maximum permissible data frame length (FLmax)

$$k = 3 \text{ to } 255: FL_{\max} = \frac{21k+2}{20k} FL \times 11$$

- Minimum permissible baud rate for reception on the transmitting side (BRmin)

$$k = 2: BR_{\min} = \text{Brate} - \frac{1}{22k} \text{ Brate}$$

$$k = 3 \text{ to } 255: BR_{\min} = (FL_{\max}/11)^{-1} = \frac{20k}{21k-2} \text{ Brate}$$

Table 17 - 5 shows the permissible baud rate error between UART and the transmitting side can be calculated from the above minimum and maximum baud rate expressions.

Table 17 - 5 Maximum/Minimum Permissible Baud Rate Error

Division ratio (k)	Maximum permissible baud rate error	Minimum permissible baud rate error
2	+2.27%	-2.27%
4	+2.33%	-2.44%
8	+3.53%	-3.61%
20	+4.27%	-4.31%
50	+4.56%	-4.58%
100	+4.66%	-4.67%
255	+4.72%	-4.73%

Remark 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the division ratio (k), the higher the permissible error.

Remark 2. k: Set value of BRGCAn register

14. 19.4.3 Repeat mode (Page 1024, Page 1025)

Incorrect:

(Page 1024)

(omitted)

1. Example 1 of using repeat mode: Outputting stepping motor control pulses using port pins
 The DTC is activated using the interval timer function of channel 0 of timer array unit 0, and the patterns of the motor control pulse stored in the code flash memory are transferred to the general-purpose port pins.
 - The vector address is **FEC14H** and control data is allocated at FFCD0H to FFCD7H.
 - Transfers 8-byte data at addresses from 02000H to 02007H of the code flash memory from the mirror area (F2000H to F2007H) to port register 1 (FFF01H).
 - A repeat mode interrupt is disabled.

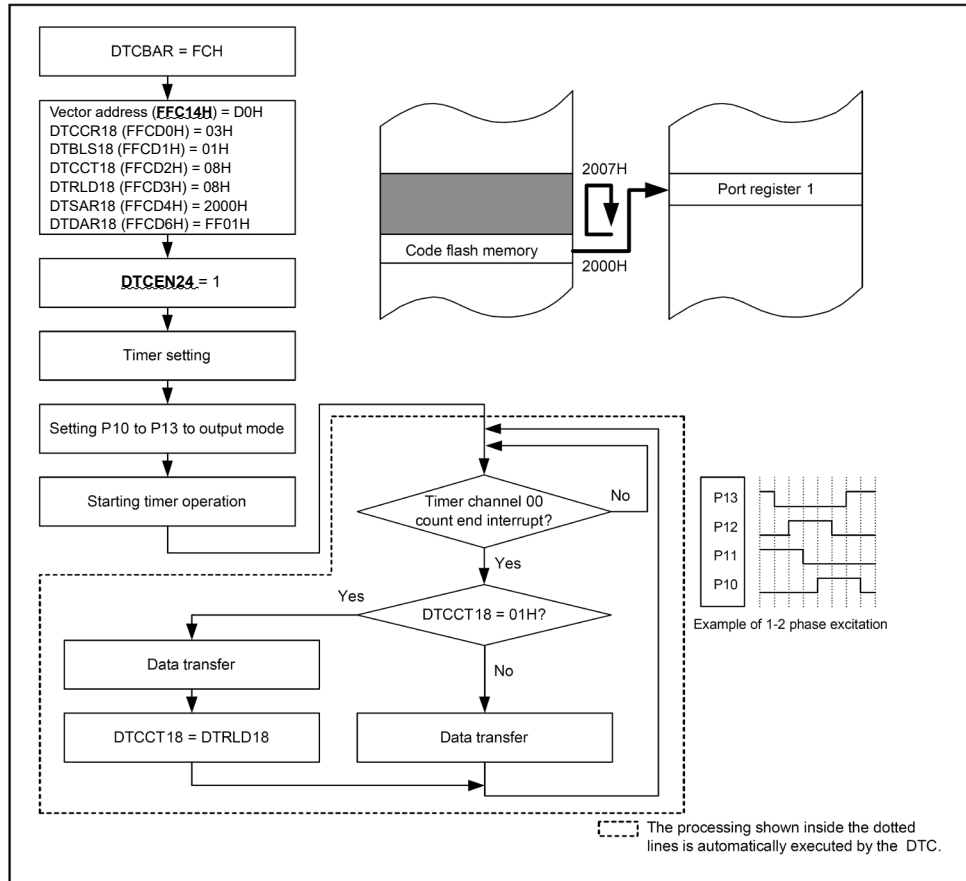
Correct:

(omitted)

1. Example 1 of using repeat mode: Outputting stepping motor control pulses using port pins
 The DTC is activated using the interval timer function of channel 0 of timer array unit 0, and the patterns of the motor control pulse stored in the code flash memory are transferred to the general-purpose port pins.
 - The vector address is **FFC17H** and control data is allocated at FFCD0H to FFCD7H.
 - Transfers 8-byte data at addresses from 02000H to 02007H of the code flash memory from the mirror area (F2000H to F2007H) to port register 1 (FFF01H).
 - A repeat mode interrupt is disabled.

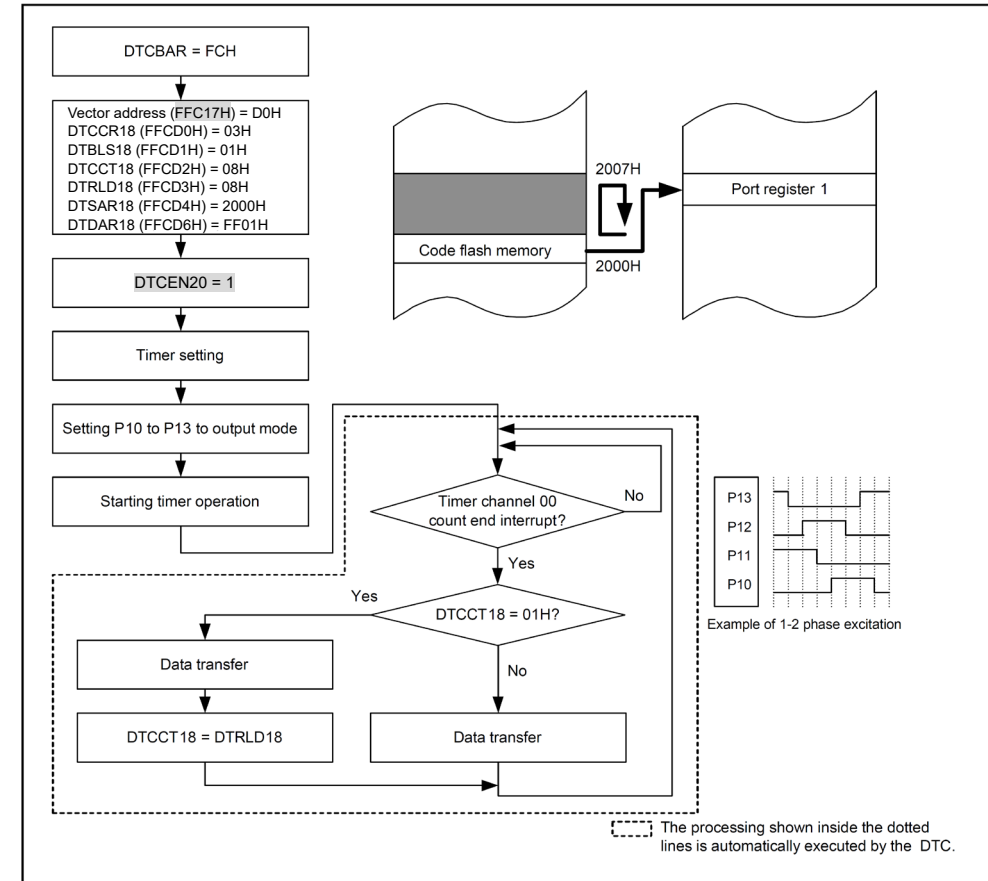
(Page 1024)

Figure 19 - 19 Example 1 of Using Repeat Mode: Outputting Stepping Motor Control Pulses Using Port Pins



To stop the output, stop the timer first and then clear **DTCEN24**.

Figure 19 - 19 Example 1 of Using Repeat Mode: Outputting Stepping Motor Control Pulses Using Port Pins



To stop the output, stop the timer first and then clear **DTCEN20**.

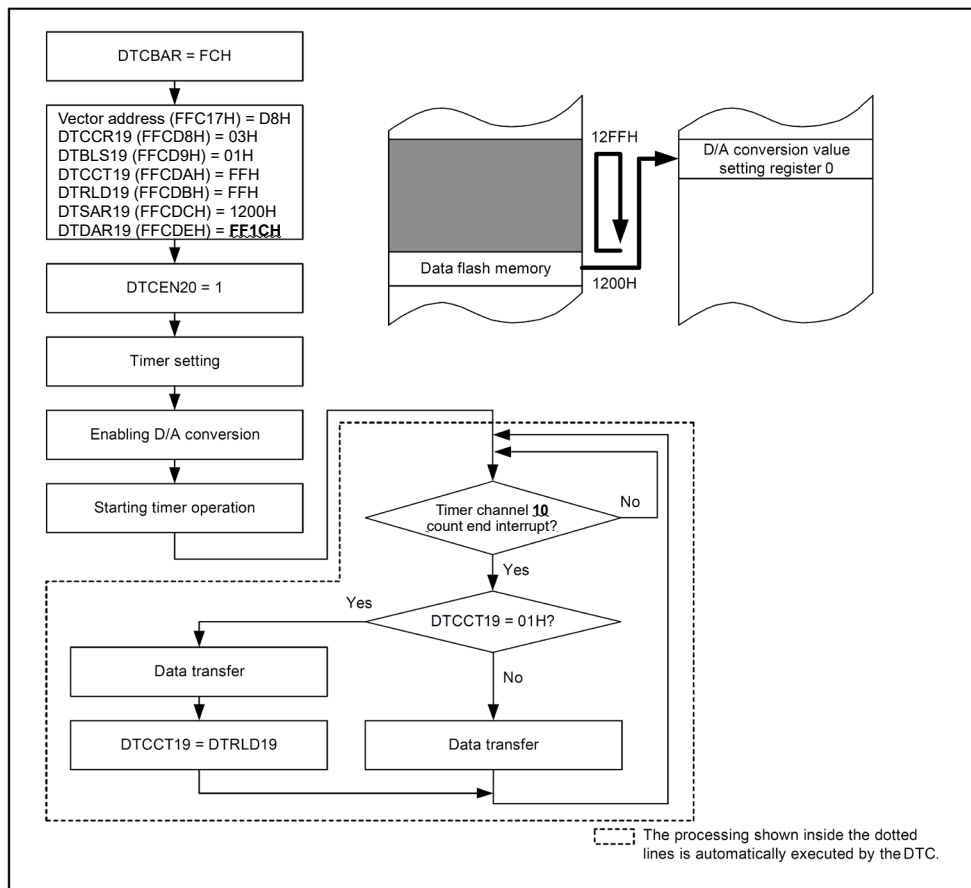
(Page 1025)

2. Example 2 of using repeat mode: Outputting a sine wave using the 8-bit D/A converter

The DTC is activated using an interrupt of the interval timer function of channel 0 of timer array unit 1, and the table of the sine wave stored in the data flash memory is transferred to the 8-bit D/A conversion value setting register 0 (F0330H). The timer interval time is set to the D/A output setup time.

(omitted)

Figure 19 - 20 Example 2 of Using Repeat Mode: Outputting a Sine Wave Using the 8-bit D/A Converter



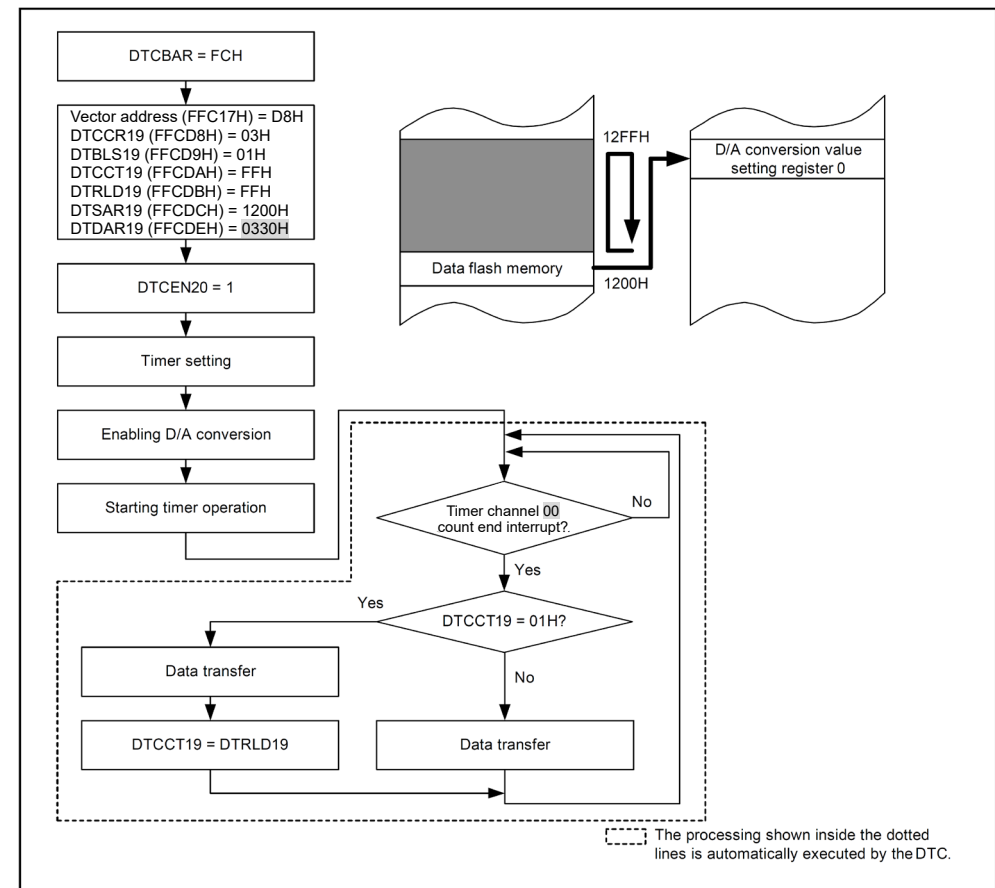
(omitted)

2. Example 2 of using repeat mode: Outputting a sine wave using the 8-bit D/A converter

The DTC is activated using an interrupt of the interval timer function of channel 0 of timer array unit 0, and the table of the sine wave stored in the data flash memory is transferred to the 8-bit D/A conversion value setting register 0 (F0330H). The timer interval time is set to the D/A output setup time.

(omitted)

Figure 19 - 20 Example 2 of Using Repeat Mode: Outputting a Sine Wave Using the 8-bit D/A Converter



(omitted)

15. 37.2.3 Characteristics of the On-chip Oscillators (Page 1401)

Incorrect:

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f _H		1		32	MHz

Middle-speed on-chip oscillator clock frequency ^{Note 3}	f _M		1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy ^{Note 1}			-12		+12	%
Middle-speed on-chip oscillator clock correction resolution				0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient					±0.17 ^{Note 4}	%/°C
Low-speed on-chip oscillator clock frequency ^{Note 3}	f _L			32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy ^{Note 1}			-15		+15	%
Low-speed on-chip oscillator clock correction resolution				0.3		%
Low-speed on-chip oscillator frequency temperature coefficient					±0.21 ^{Note 4}	%/°C

Note 1. The accuracy values were obtained in testing of this product.

Note 2. The listed condition applies when the setting of the FRQSEL3 bit is 1.

Note 3. The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.

Note 4. ~~Guaranteed by characterization results.~~

Correct:

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f _H		1		32	MHz

Middle-speed on-chip oscillator clock frequency ^{Note 3}	f _M		1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy ^{Note 1}			-12		+12	%
Middle-speed on-chip oscillator clock correction resolution				0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient					±0.17 ^{Note 4}	%/°C
Low-speed on-chip oscillator clock frequency ^{Note 3}	f _L			32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy ^{Note 1}			-15		+15	%
Low-speed on-chip oscillator clock correction resolution				0.3		%
Low-speed on-chip oscillator frequency temperature coefficient					±0.21 ^{Note 4}	%/°C

Note 1. The accuracy values were obtained in testing of this product.

Note 2. The listed condition applies when the setting of the FRQSEL3 bit is 1.

Note 3. The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.

Note 4. ~~These values are the results of characteristic evaluation and are not checked for shipment.~~

16. 37.3.1 Pin characteristics (Page 1406)

Incorrect:

(omitted)

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (3/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input voltage, high	VH1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8 EVDD0		EVDD0	V
	VH2	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2		EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0		EVDD0	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	1.5		EVDD0	V
	VH3	P20 to P27, P150 to P156		0.7 VDD		VDD	V
	VH4	P60 to P63		0.7 EVDD0		6.0	V
	VH5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8 VDD		VDD	V
Input voltage, low	VIL1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2 EVDD0	V
			TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0		0.5	V
	VIL2	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	0		0.32	V
	VIL3	P20 to P27, P150 to P156		0		0.3 VDD	V
	VIL4	P60 to P63		0		0.3 EVDD0	V
VIL5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2 VDD	V	

(omitted)

Correct:

(omitted)

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (3/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input voltage, high	VH1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8 EVDD0		EVDD0	V
	VH2	P01, P03, P04, P10, P11, P13 to P17, P41, P43, P44, P53 to P55, P71, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2		EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0		EVDD0	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	1.5		EVDD0	V
	VH3	P20 to P27, P150 to P156		0.7 VDD		VDD	V
	VH4	P60 to P63		0.7 EVDD0		6.0	V
	VH5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8 VDD		VDD	V
Input voltage, low	VIL1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2 EVDD0	V
			TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0		0.5	V
	VIL2	P01, P03, P04, P10, P11, P13 to P17, P41, P43, P44, P53 to P55, P71, P80, P81, P142, P143	TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	0		0.32	V
	VIL3	P20 to P27, P150 to P156		0		0.3 VDD	V
	VIL4	P60 to P63		0		0.3 EVDD0	V
VIL5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2 VDD	V	

(omitted)

17. 37.3.2 Supply current characteristics (Page 1411, Page 1414, Page 1418, Page 1421, Page 1425, Page 1428)

Incorrect:
(Page 1411)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (1/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	VDD = 5.0 V	1.3	—	mA
						VDD = 1.8 V	1.3	—	
					Normal operation	VDD = 5.0 V	3.0	5.0	mA
						VDD = 1.8 V	3.0	5.0	
				f _{MX} = 8 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V	0.9	1.4	mA
						VDD = 1.8 V	0.8	1.4	

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- ~~The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.~~

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

Correct:

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (1/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	VDD = 5.0 V	1.3	—	mA
						VDD = 1.8 V	1.3	—	
					Normal operation	VDD = 5.0 V	3.0	5.0	mA
						VDD = 1.8 V	3.0	5.0	
				f _{MX} = 8 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V	0.9	1.4	mA
						VDD = 1.8 V	0.8	1.4	

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1414)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current ^{Note 1}	I _{DD2} ^{Note 2}	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 3}	V _{DD} = 5.0 V		0.54	1.93	mA
					V _{DD} = 1.8 V		0.53	1.92	
				f _{MX} = 8 MHz ^{Note 5} , Resonator connection	V _{DD} = 5.0 V		0.21	0.58	mA
					V _{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.

- ~~The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.~~

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current ^{Note 1}	I _{DD2} ^{Note 2}	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 3}	V _{DD} = 5.0 V		0.54	1.93	mA
					V _{DD} = 1.8 V		0.53	1.92	
				f _{MX} = 8 MHz ^{Note 5} , Resonator connection	V _{DD} = 5.0 V		0.21	0.58	mA
					V _{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.

- The currents in the “Max.” column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1418)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (1/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	VDD = 5.0 V	1.4	—	mA
						VDD = 1.8 V	1.4	—	
				Normal operation	VDD = 5.0 V	3.0	5.0	mA	
					VDD = 1.8 V	3.0	5.0		

				f _{MX} = 8 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V	0.9	1.4	mA
						VDD = 1.8 V	0.8	1.4	

- Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.
- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
 - ~~The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.~~

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (1/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	VDD = 5.0 V	1.4	—	mA
						VDD = 1.8 V	1.4	—	
				Normal operation	VDD = 5.0 V	3.0	5.0	mA	
					VDD = 1.8 V	3.0	5.0		

				f _{MX} = 8 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V	0.9	1.4	mA
						VDD = 1.8 V	0.8	1.4	

- Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.
- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
 - The currents in the “Max.” column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1421)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current ^{Note 1}	IDD2 ^{Note 2}	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 3}	VDD = 5.0 V		0.57	1.97	mA
					VDD = 1.8 V		0.56	1.96	
				f _{MX} = 8 MHz ^{Note 5} , Resonator connection	VDD = 5.0 V		0.21	0.58	mA
					VDD = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.

~~· The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.~~

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current ^{Note 1}	IDD2 ^{Note 2}	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 3}	VDD = 5.0 V		0.57	1.97	mA
					VDD = 1.8 V		0.56	1.96	
				f _{MX} = 8 MHz ^{Note 5} , Resonator connection	VDD = 5.0 V		0.21	0.58	mA
					VDD = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.

· The currents in the “Max.” column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1425)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (1/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	VDD = 5.0 V	1.6	—	mA
						VDD = 1.8 V	1.5	—	
					Normal operation	VDD = 5.0 V	3.5	5.6	mA
						VDD = 1.8 V	3.5	5.6	

				f _{MX} = 8 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V	1.0	1.6	mA
						VDD = 1.8 V	1.0	1.6	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- ~~The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.~~

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (1/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	VDD = 5.0 V	1.6	—	mA
						VDD = 1.8 V	1.5	—	
					Normal operation	VDD = 5.0 V	3.5	5.6	mA
						VDD = 1.8 V	3.5	5.6	

				f _{MX} = 8 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V	1.0	1.6	mA
						VDD = 1.8 V	1.0	1.6	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

(Page 1428)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current ^{Note 1}	IDD2 ^{Note 2}	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 3}	VDD = 5.0 V		0.60	2.00	mA
					VDD = 1.8 V		0.59	1.99	
				f _{MX} = 8 MHz ^{Note 5} , Resonator connection	VDD = 5.0 V		0.22	0.59	mA
					VDD = 1.8 V		0.21	0.58	

Note 1. The listed currents are the total currents flowing into VDD, EVDD0 and EVDD1, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0, EVDD1 or VSS, EVSS0, EVSS1. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- ~~The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.~~

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current ^{Note 1}	IDD2 ^{Note 2}	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 3}	VDD = 5.0 V		0.60	2.00	mA
					VDD = 1.8 V		0.59	1.99	
				f _{MX} = 8 MHz ^{Note 5} , Resonator connection	VDD = 5.0 V		0.22	0.59	mA
					VDD = 1.8 V		0.21	0.58	

Note 1. The listed currents are the total currents flowing into VDD, EVDD0 and EVDD1, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0, EVDD1 or VSS, EVSS0, EVSS1. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the PCLBUZ, TAU, SAU and IICA.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(omitted)

18. 37.6.1 A/D converter characteristics (Page 1475, Page 1476)

Incorrect:
(Page 1475)

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1), target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		32	MHz
Overall error ^{Notes 1, 2, 3, 4}	AINL	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V		±7.5	LSB
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±9.0	LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±9.0	LSB
Conversion time ^{Note 5}	tCONV	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V	2.0		μs
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V	2.0		μs
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V	2.0		μs
Zero-scale error ^{Notes 1, 2, 3, 4, 6}	Ezs	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V		±0.17	%FSR
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±0.21	%FSR
Full-scale error ^{Notes 1, 2, 3, 4, 6}	Efs	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V		±0.17	%FSR
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±0.21	%FSR
Integral linearity error ^{Notes 1, 3, 4}	ILE	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V		±3.0	LSB
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±3.0	LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±3.0	LSB
Differential linearity error ^{Note 1}	DLE	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V	±1.0		LSB
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V	±1.0		LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V	±1.0		LSB
Analog input voltage	VAIN		0		AVREFP	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Correct:

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1), target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		32	MHz
Overall error ^{Notes 1, 2, 3, 4}	AINL	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V		±7.5	LSB
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±9.0	LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±9.0	LSB
Conversion time ^{Note 5}	tCONV	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V	2.0		μs
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V	2.0		μs
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V	2.0		μs
Zero-scale error ^{Notes 1, 2, 3, 4, 6}	Ezs	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V		±0.17	%FSR
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±0.21	%FSR
Full-scale error ^{Notes 1, 2, 3, 4, 6}	Efs	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V		±0.17	%FSR
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±0.21	%FSR
Integral linearity error ^{Notes 1, 3, 4}	ILE	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V		±3.0	LSB
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±3.0	LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±3.0	LSB
Differential linearity error ^{Note 1}	DLE	12-bit resolution	4.5 V ≤ AVREFP = VDD ≤ 5.5 V	±1.0		LSB
			2.7 V ≤ AVREFP = VDD ≤ 5.5 V	±1.0		LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V	±1.0		LSB
Analog input voltage	VAIN		0		AVREFP	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. When pins ANI16 to ANI26 are selected as the target pins for conversion or the TSCAP voltage of the CTSU is to be A/D converted, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

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2. Low-voltage modes 1 and 2

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{AVREFP} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = 0\text{ V}$, reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1), target pins ANI2 to ANI14, internal reference voltage^{Note 1}, and temperature sensor output voltage^{Note 1})

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	f _{AD}		1		24	MHz
Overall error ^{Notes 2, 3, 4, 5}	AINL	12-bit resolution	$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±9	LSB
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±9	LSB
			$1.8\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±11.5	LSB
			$1.6\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±12.0	LSB
Conversion time ^{Note 6}	t _{CONV}	12-bit resolution	$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	3.33		µs
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	5.0		µs
			$1.8\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	10.0		µs
			$1.6\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	20.0		µs
Zero-scale error ^{Notes 2, 3, 4, 5, 7}	EzS	12-bit resolution	$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.21	%FSR
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.21	%FSR
			$1.8\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.27	%FSR
			$1.6\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.28	%FSR
Full-scale error ^{Notes 2, 3, 4, 5, 7}	EFS	12-bit resolution	$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.21	%FSR
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.21	%FSR
			$1.8\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.27	%FSR
			$1.6\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.28	%FSR
Analog input voltage	V _{AIN}		0		AVREFP	V

Note 1. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VDD must be at least 1.8 V.

Note 2. This value does not include the quantization error (±1/2 LSB).

Note 3. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

2. Low-voltage modes 1 and 2

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{AVREFP} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = 0\text{ V}$, reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1), target pins ANI2 to ANI14, internal reference voltage^{Note 1}, and temperature sensor output voltage^{Note 1})

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	f _{AD}		1		24	MHz
Overall error ^{Notes 2, 3, 4, 5}	AINL	12-bit resolution	$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±9	LSB
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±9	LSB
			$1.8\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±11.5	LSB
			$1.6\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±12.0	LSB
Conversion time ^{Note 6}	t _{CONV}	12-bit resolution	$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	3.33		µs
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	5.0		µs
			$1.8\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	10.0		µs
			$1.6\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	20.0		µs
Zero-scale error ^{Notes 2, 3, 4, 5, 7}	EzS	12-bit resolution	$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.21	%FSR
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.21	%FSR
			$1.8\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.27	%FSR
			$1.6\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.28	%FSR
Full-scale error ^{Notes 2, 3, 4, 5, 7}	EFS	12-bit resolution	$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.21	%FSR
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.21	%FSR
			$1.8\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.27	%FSR
			$1.6\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		±0.28	%FSR
Analog input voltage	V _{AIN}		0		AVREFP	V

Note 1. If the internal reference voltage, temperature sensor output voltage, or voltage on the TSCAP pin of the CTSU is to be A/D converted, VDD must be at least 1.8 V.

Note 2. This value does not include the quantization error (±1/2 LSB).

Note 3. When pins ANI16 to ANI26 are selected as the target pins for conversion or the TSCAP voltage of the CTSU is to be A/D converted, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.