Date: Apr. 26, 2024

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0133A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G23 Descriptions in the User's Manual: Hardware Rev. 1.30 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G23 Group	Lot No. All lots	Reference Document	RL78/G23 User's Manual: Hardware Rev. 1.30 R01UH0896EJ0130 (Jan. 2024)		

This document describes misstatements found in the RL78/G23 User's Manual: Hardware Rev. 1.30 (R01UH0896EJ0130).

Corrections

Applicable Item	Applicable Page	Contents
3.1 Memory Space	Page 147 to Page 153, Page 160	Incorrect descriptions revised
33.6.1 Self-programming procedure	Page 1315	Incorrect descriptions revised
33.10.1 Overview of the data flash memory	Page 1366	Incorrect descriptions revised
34.3 Security Settings for On-chip Debugging	Page 1369	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0896EJ0130	
1	3.1 Memory Space		Page 147 to Page 153, Page 160	Page 3 to Page 10
2	33.6.1 Self-programming procedure		Page 1315	Page 11
3	33.10.1 Overview of the data flash memory		Page 1366	Page 12
4	34.3 Security Settings for On-chip Debugging		Page 1369	Page 13

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G23 Correction for incorrect description notice

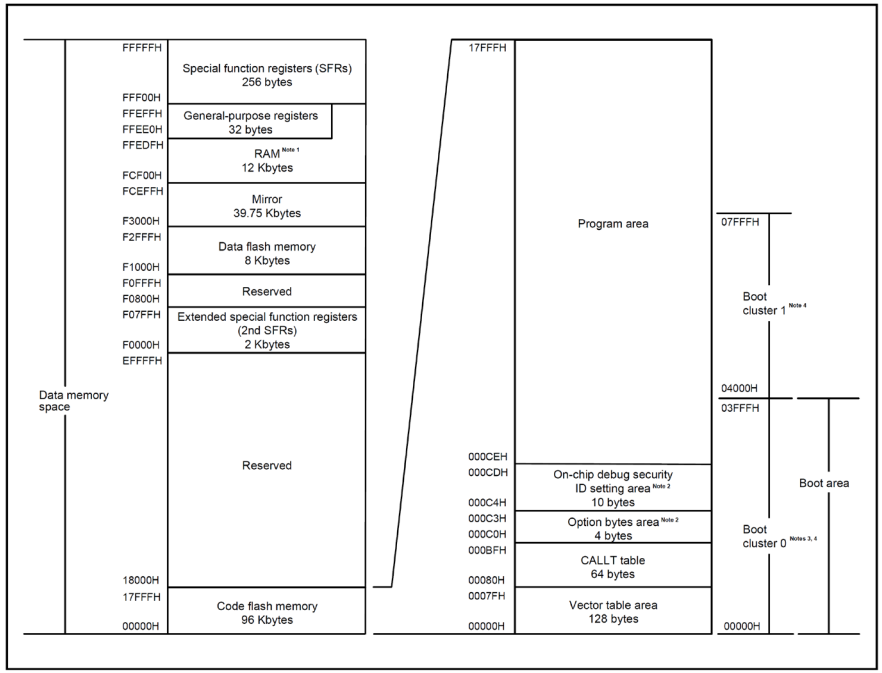
Document Number	Issue Date	Description
TN-RL*-A0133A/E	Apr. 26, 2024	First edition issued Corrections No.1 to No.4 revised (this document)

1. **3.1 Memory Space (Page 147 to Page 153, Page 160)**

Incorrect:
(Page 147)

Products in the RL78/G23 can access a 1 MB address space. Figure 3 - 1 to Figure 3 - 3 show the memory maps.

Figure 3 - 1 Memory Map (R7F100GxF (x = A, B, C, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

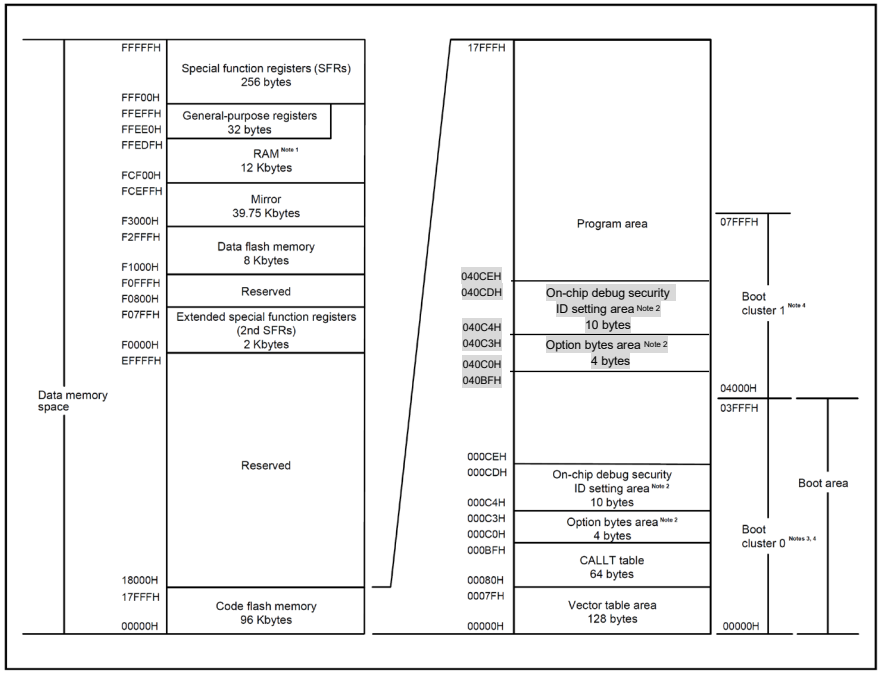
Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Correct:

Products in the RL78/G23 can access a 1 MB address space. Figure 3 - 1 to Figure 3 - 3 show the memory maps.

Figure 3 - 1 Memory Map (R7F100GxF (x = A, B, C, E, F, G, J, L))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.
When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

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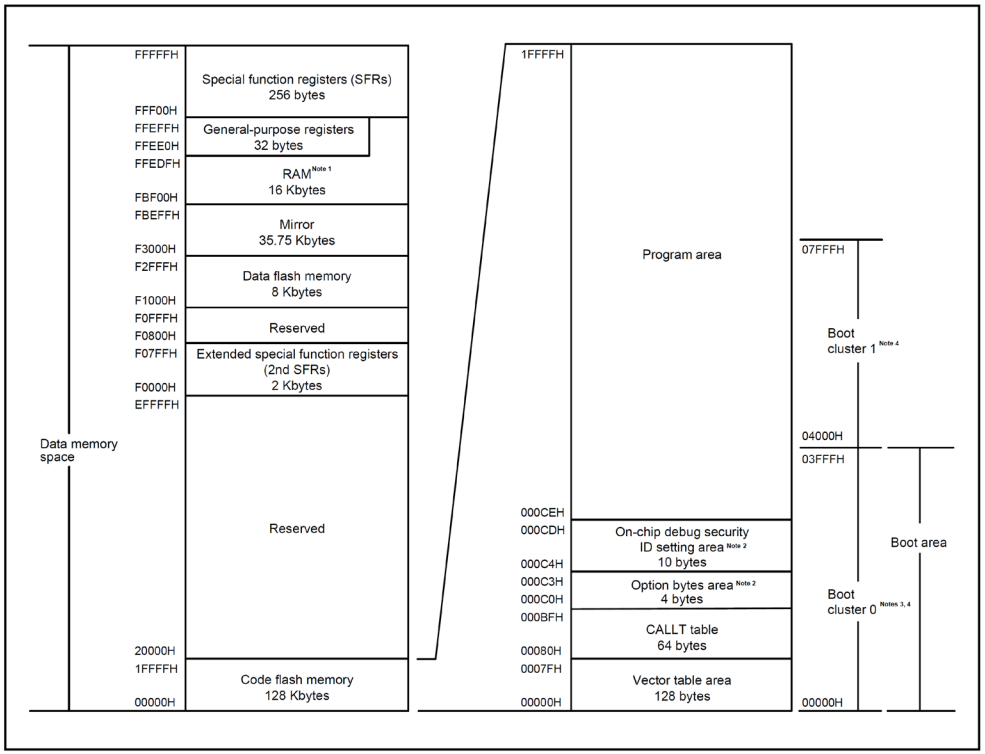
Figure 3 - 2 Memory Map (R7F100GxG (x = A, B, C, E, F, G, J, L, M, P))



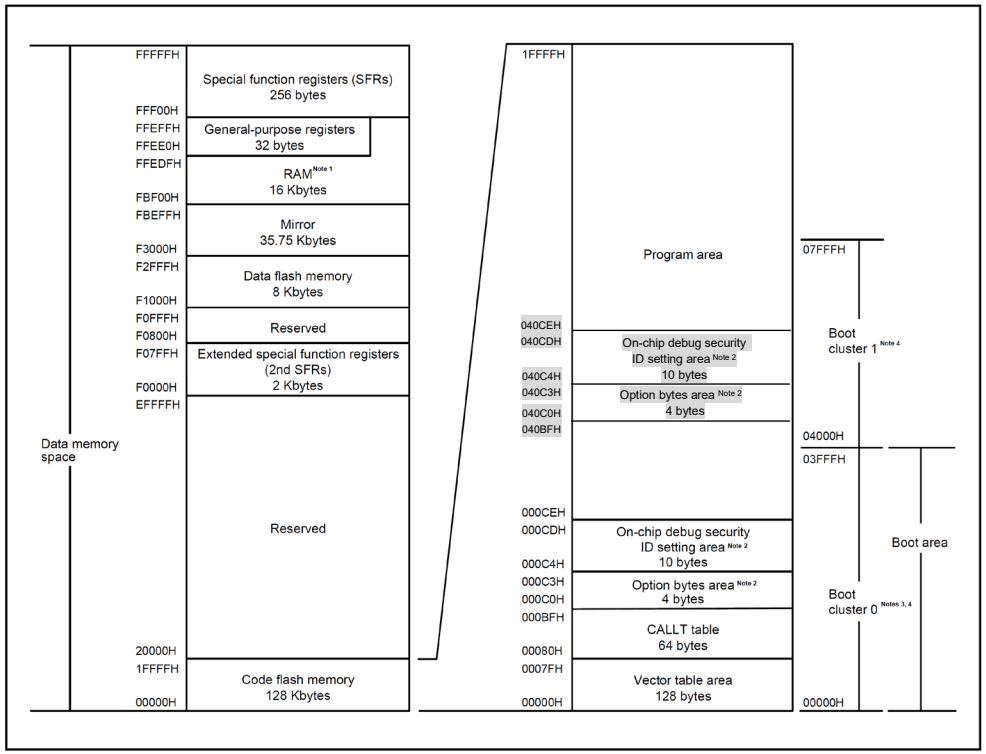
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 2 Memory Map (R7F100GxG (x = A, B, C, E, F, G, J, L, M, P))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

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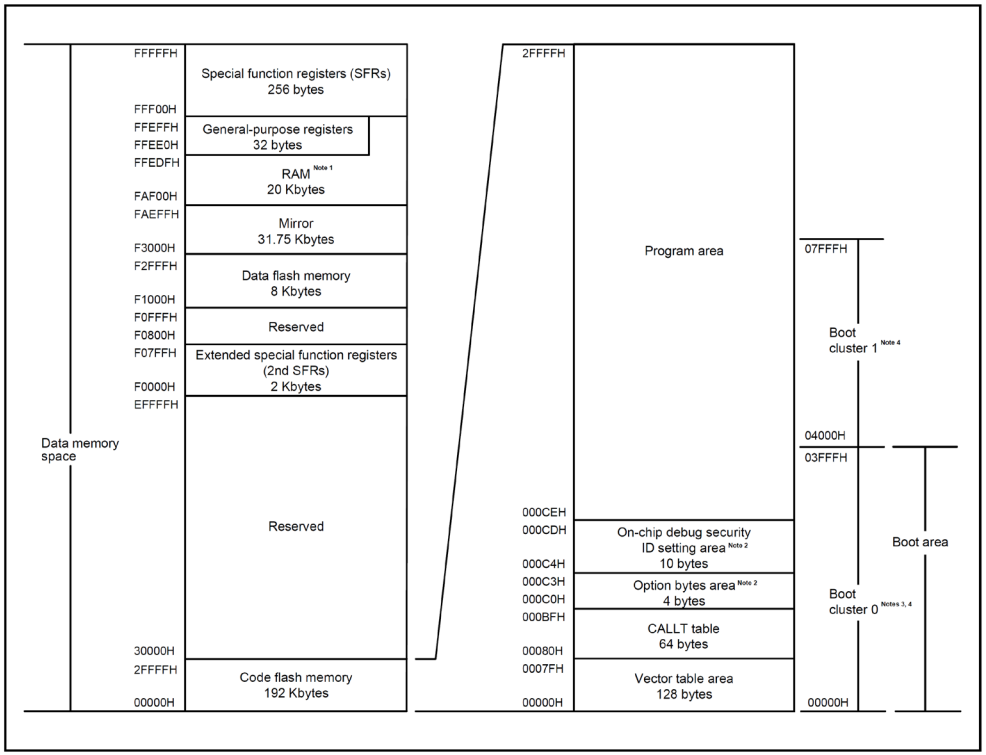
Figure 3 - 3 Memory Map (R7F100GxH (x = A, B, C, E, F, G, J, L, M, P))



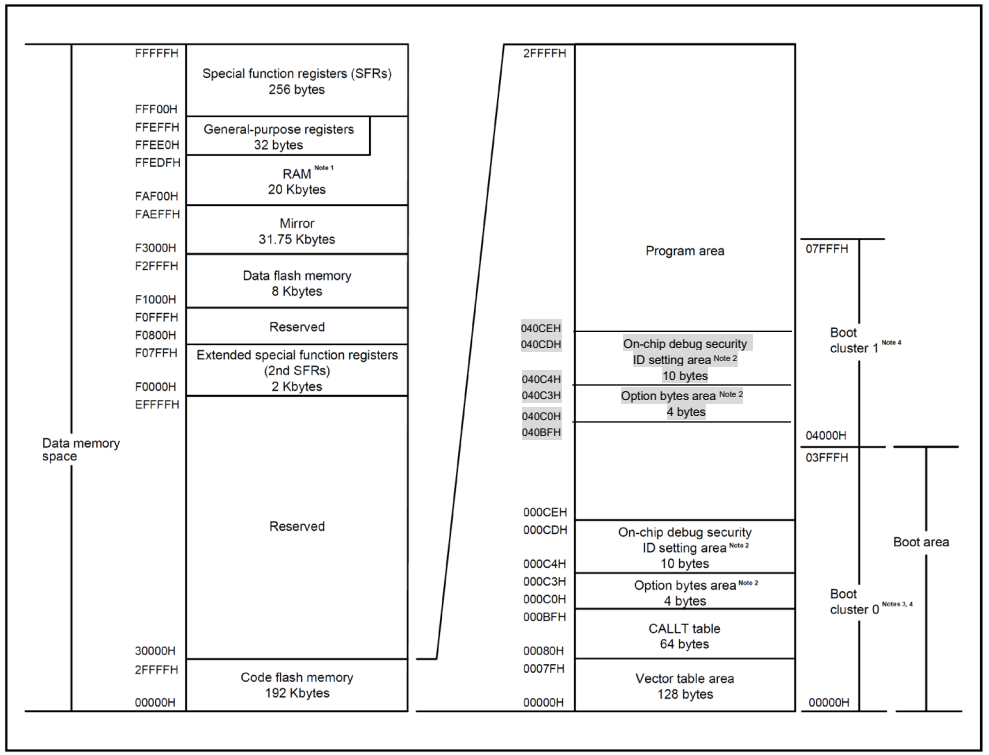
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 3 Memory Map (R7F100GxH (x = A, B, C, E, F, G, J, L, M, P))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

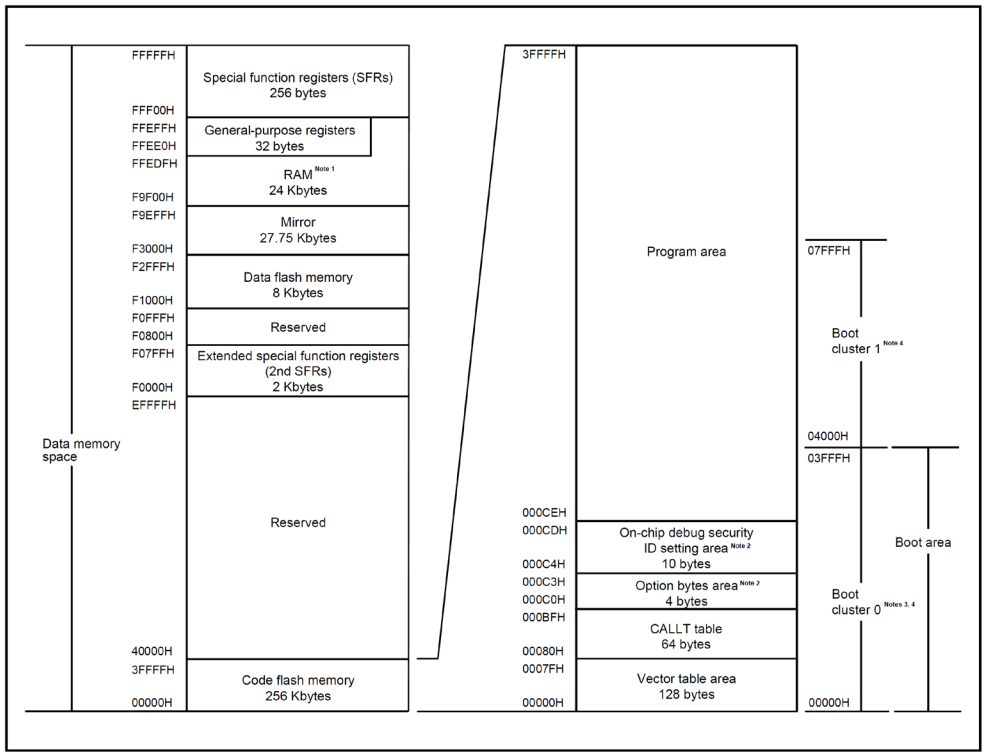
Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 150)

Figure 3 - 4 Memory Map (R7F100GxJ (x = A, B, C, E, F, G, J, L, M, P, S))



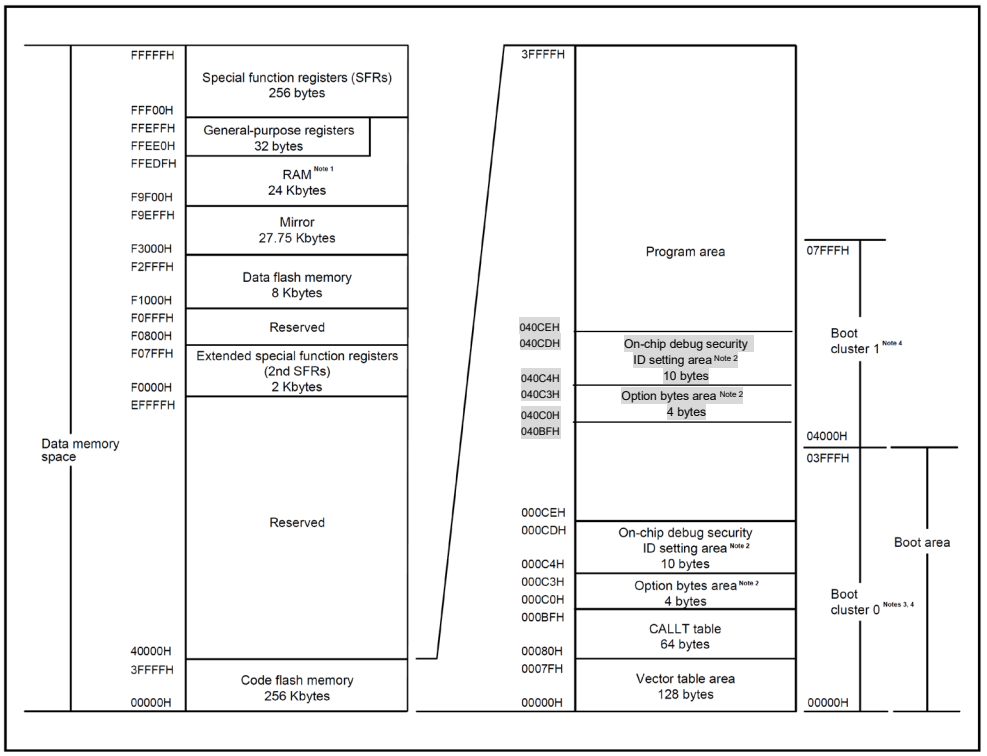
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 4 Memory Map (R7F100GxJ (x = A, B, C, E, F, G, J, L, M, P, S))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

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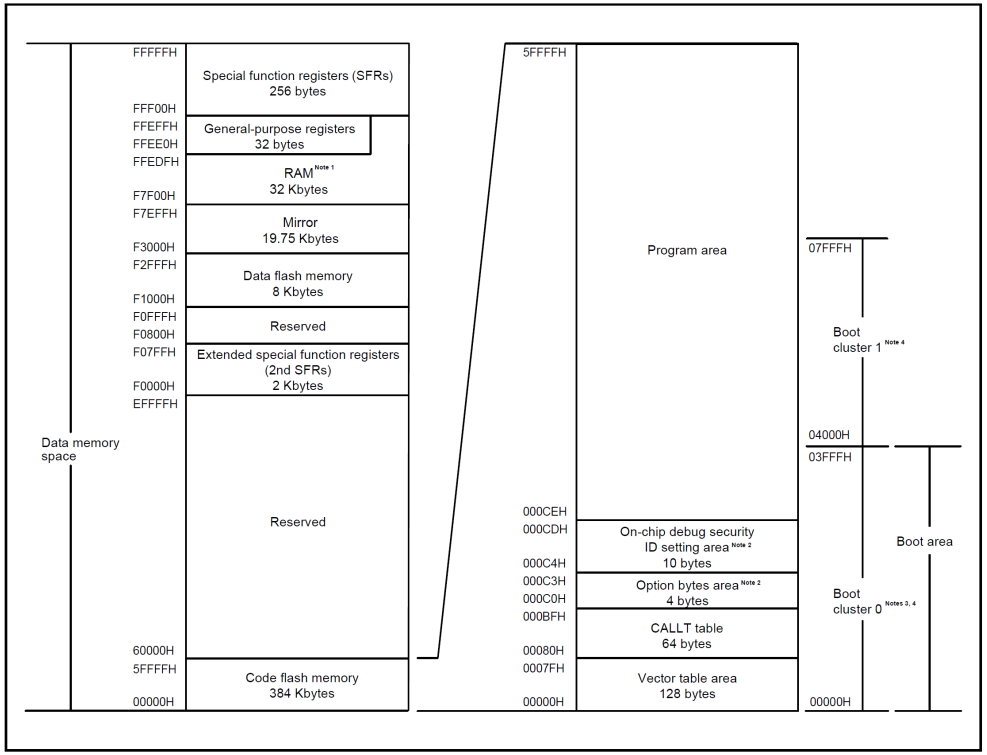
Figure 3 - 5 Memory Map (R7F100GxK (x = F, G, J, L, M, P, S))



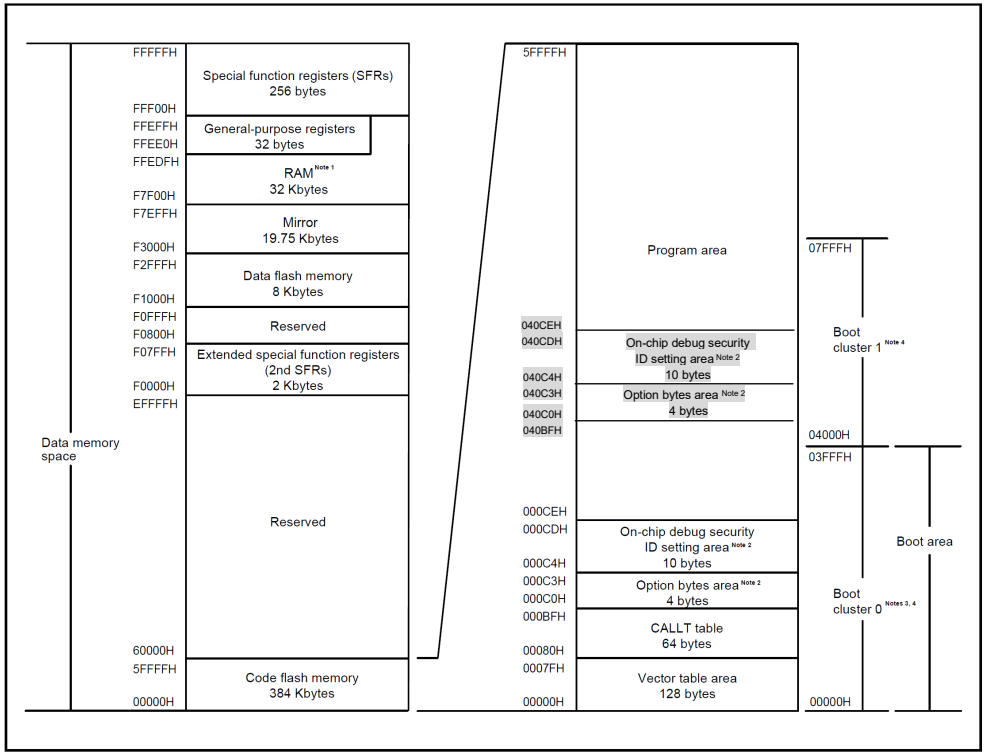
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 5 Memory Map (R7F100GxK (x = F, G, J, L, M, P, S))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

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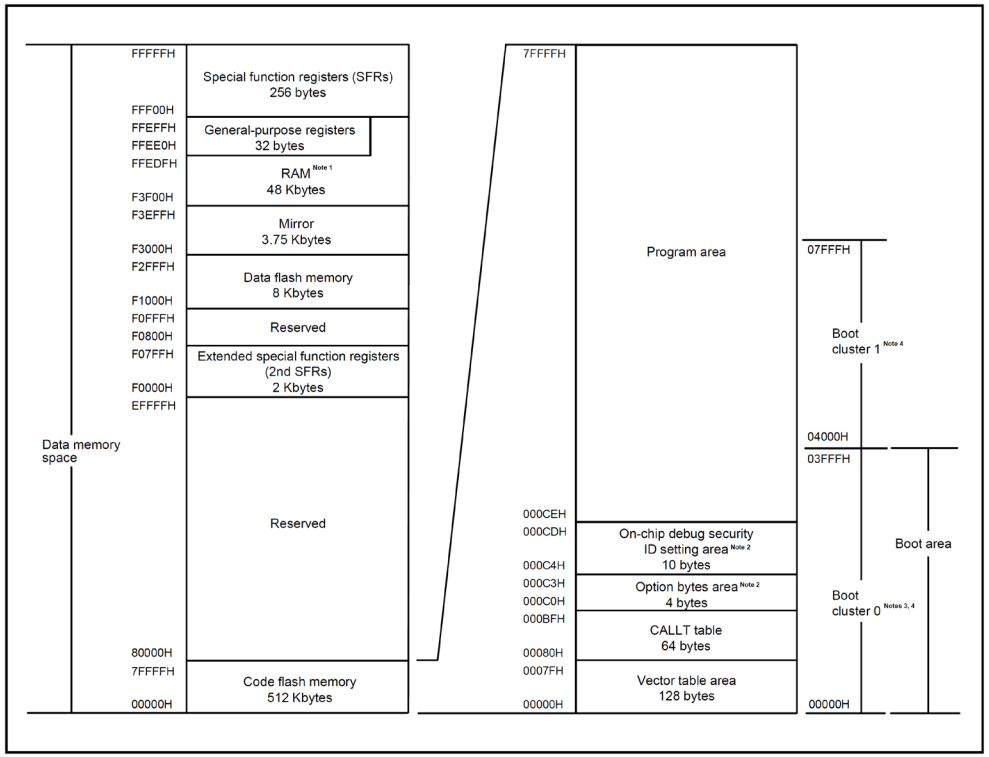
Figure 3 - 6 Memory Map (R7F100GxL (x = F, G, J, L, M, P, S))



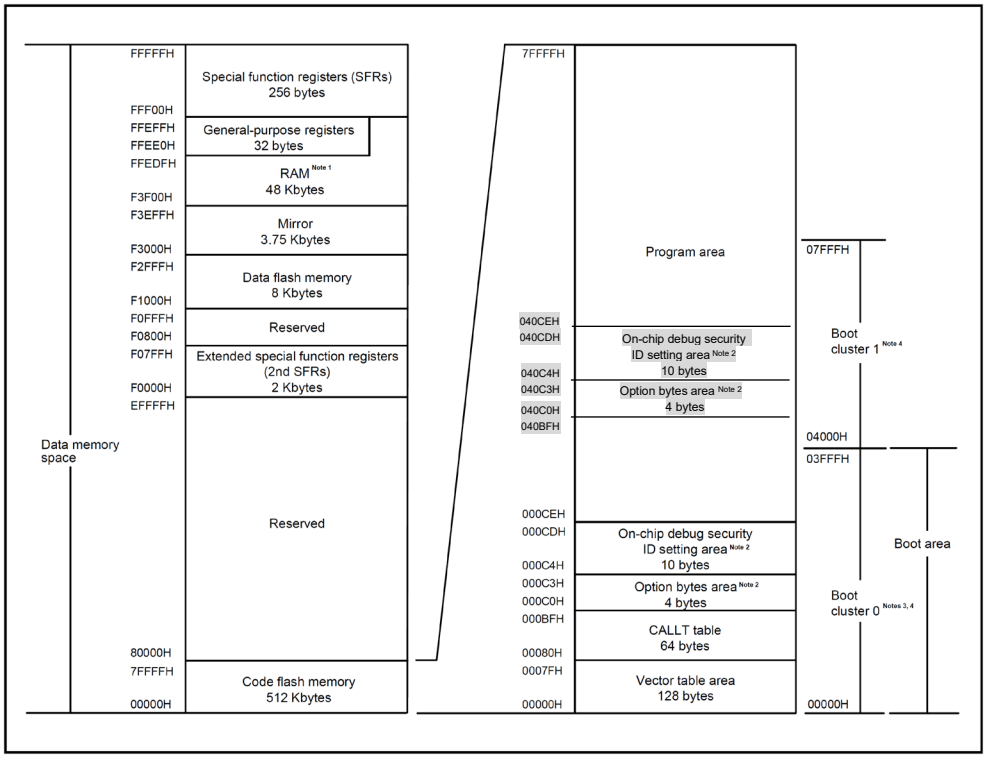
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 6 Memory Map (R7F100GxL (x = F, G, J, L, M, P, S))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

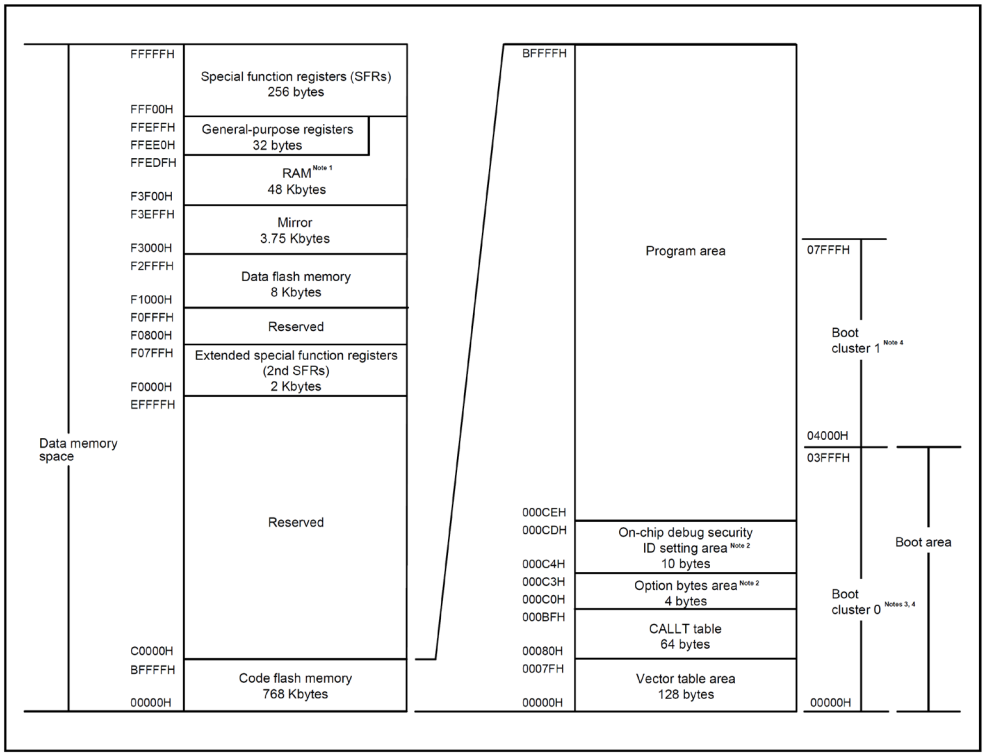
Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 153)

Figure 3 - 7 Memory Map (R7F100GxN (x = F, G, J, L, M, P, S))



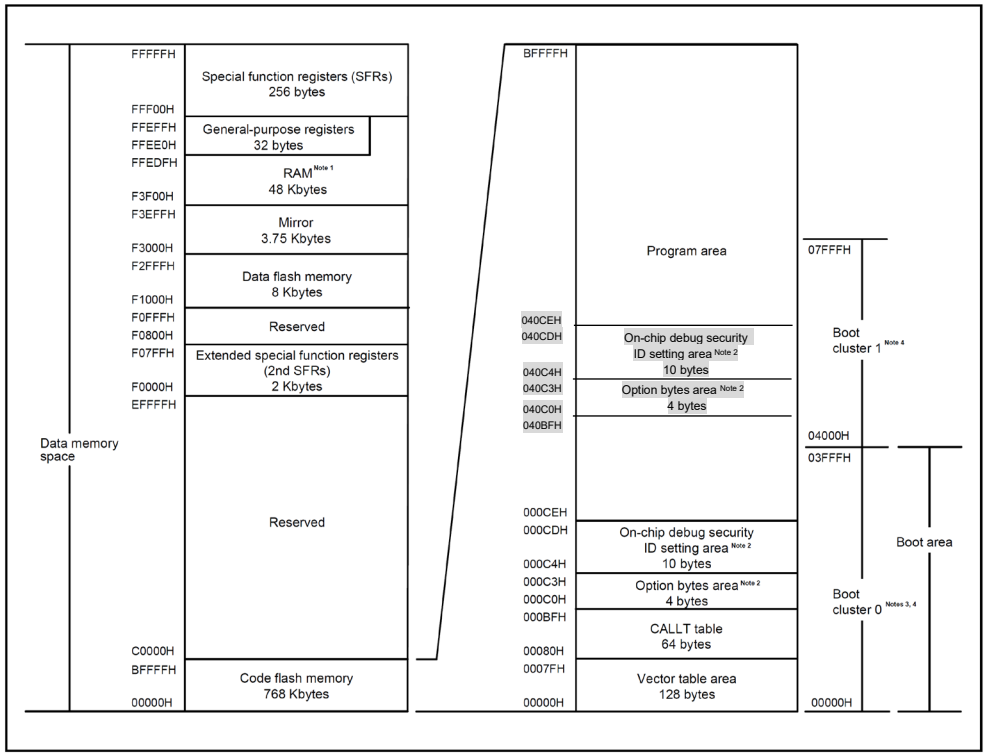
Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. **When boot swap is not used:** Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

Figure 3 - 7 Memory Map (R7F100GxN (x = F, G, J, L, M, P, S))



Note 1. Instructions can be executed from the RAM area excluding the general-purpose register area.

Note 2. When boot swapping is not to be used, that is, when the value of the BTFLG bit in the FLSEC register is 1, set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0, set the option bytes to 000C0H to 000C3H and 040C0H to 040C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 040C4H to 040CDH.

(omitted)

(Page 160)

(omitted)

3. Option bytes area
   A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when **the boot swap is used**. For details, see Section 32 Option Bytes.
4. On-chip debug security ID setting area
   A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. **Set the on-chip debug security ID of 10 bytes at 000C4H to 000CDH when the boot swap is not used and at 000C4H to 000CDH and at 040C4H to 040CDH when the boot swap is used.** For details, see Section 34 On-chip Debugging.

(omitted)

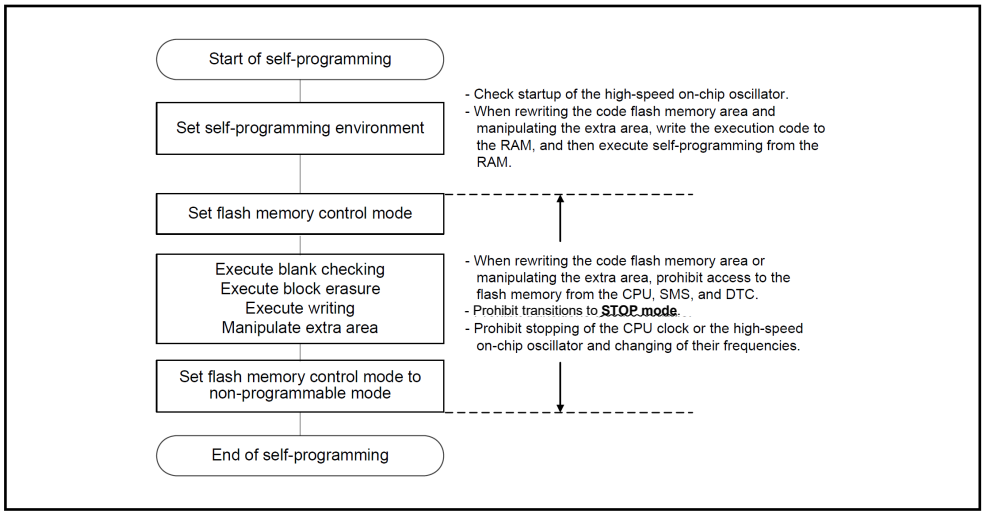
3. Option bytes area
   A 4-byte area of 000C0H to 000C3H can be used as an option bytes area. Set the option byte at 040C0H to 040C3H when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0. For details, see Section 32 Option Bytes.
4. On-chip debug security ID setting area
   A 10-byte area of 000C4H to 000CDH and 040C4H to 040CDH can be used as an on-chip debug security ID setting area. Set the 10−byte security ID for on-chip debugging at 000C4H to 000CDH when boot swapping is not to be used, that is, the value of the BTFLG bit in the FLSEC register is 1, and at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0. For details, see Section 34 On-chip Debugging.

2. 33.6.1 Self-programming procedure (Page 1315)

Incorrect:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 33.6.2 Registers to control the flash memory.

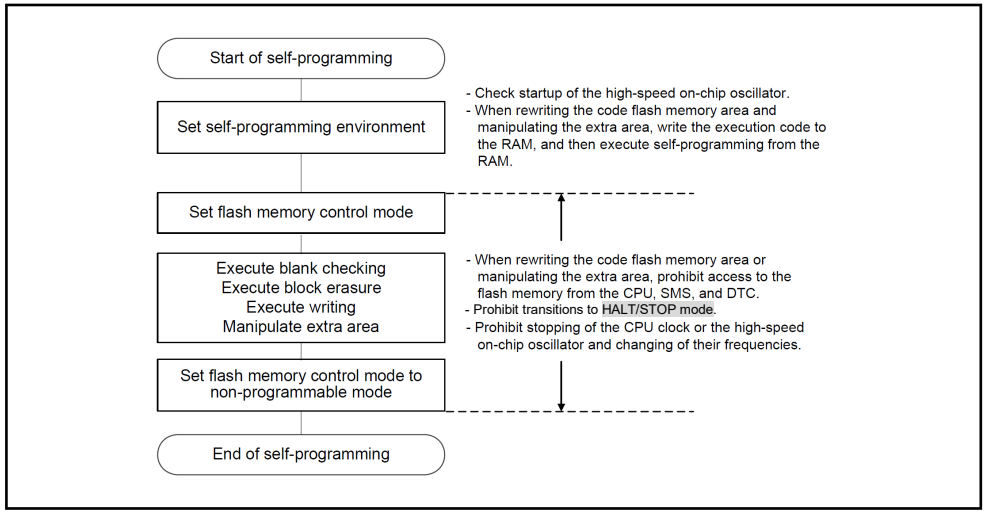
Figure 33 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



Correct:

The following figure illustrates a flow for rewriting the flash memory by using self-programming. For details on registers for use in self-programming, see 33.6.2 Registers to control the flash memory.

Figure 33 - 8 Flow of Self-Programming (Rewriting the Flash Memory)



3. 33.10.1 Overview of the data flash memory (Page 1366)

Incorrect:

An overview of the data flash memory is provided below.

(omitted)

- Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.
- Transition to the **STOP mode** is prohibited while rewriting the data flash memory.

(omitted)

Correct:

An overview of the data flash memory is provided below.

(omitted)

- Manipulating the DFLCTL register is prohibited while rewriting the data flash memory.
- Transition to the HALT/STOP mode is prohibited while rewriting the data flash memory.

(omitted)

4. 34.3 Security Settings for On-chip Debugging (Page 1369)

Incorrect:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 33.9 Security Settings in Section 33 Flash Memory).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 32 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.Note 1

Table 34 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID codeNote 2
040C4H to 040CDH	

Note 1. The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.

Note 2. The setting FFFFFFFFFFFFFFFFFFFFH is not allowed.

Correct:

To protect against third parties reading the contents of memory, on-chip debugging includes the following functionality.

- Disabling of connection between the RL78 microcontroller and the programmer or on-chip debugger (see 33.9 Security Settings in Section 33 Flash Memory).
- On-chip debugging control bits in the flash memory at 000C3H (see Section 32 Option Bytes)
- An area in the range from 000C4H to 000CDH to hold the security ID code for on-chip debugging.Note

Note The area to hold the security ID code for use in on-chip debugging is also used to hold the ID code for the programmer connection ID authentication when a programmer is to be used.

Table 34 - 1 On-chip Debug Security ID

Address	Security ID Code for On-chip Debugging
000C4H to 000CDH	Any 10-byte ID codeNote 2, 3
040C4H to 040CDH	

Note 1. The setting FFFFFFFFFFFFFFFFFFFFH is not allowed.

Note 2. Set the 10-byte security ID for on-chip debugging at both 000C4H to 000CDH and 040C4H to 040CDH when boot swapping is to be used or the value of the BTFLG bit in the FLSEC register is 0.