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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0153A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice Descriptions of errors in the RL78/F15 User's Manual: Hardware Rev.1.00		Information Category	Technical Notification		
Applicable Product	RL78/F15 Group	Lot No. All lots	Reference Document	RL78/F15 User's Manual: Hardware Rev.1.00 (R01UH0559EJ0100)		

This document describes misstatements found in RL78/F15 User's Manual: Hardware Rev.1.00 (R01UH0559EJ0100).

Related documents:

- Published technical updates [TN-RL*-A068A/E, TN-RL*-A0091A/E, TN-RL*-A0096A/E, TN-RL*-A0123A/E]
- RL78/F13, F14 User's Manual: Hardware Rev 2.10 (R01UH0368EJ0210) errata [TN-RL*-A0099B/J]
- RL78/F13, F14 User's Manual: Hardware Rev 2.30 [R01UH0368EJ0230]
- PCN "Supplier addition on Cu wire for LQFP products" [EPPO2-EX-25-0026]

Corrections:

(1/4)

No	Corrections	R01UH0559EJ0100	Pages in this document
1	Update "Table 1-3. Order Information for RL78/F15".	P.16	P.5
2	Correct the P40/TOOL0 part in Table 2-4.	P.52	P.5
3	Correct the "After reset" of MDIV register in Table 3-6.	P.107	P.5
4	Correct the port block diagram. (POMxx signal and built-in pull-up resistor ON/OFF control)	P.177 to P.184, P.225 to P.228	P.6
5	Add Note 1 (Nch open-drain output) and Note 2 (TTL input buffer) to the bottom of the port block diagram.	P.177, P.178, P.180, P.181, P.183, P.184, P.227, P.228, P.237, P.238	P.6
6	Add Note (Nch open-drain output) to the bottom of the port block diagram.	P.179, P.182, P.225, P.226, P.239, P.270	P.6
7	Add Note (TTL input buffer) to the bottom of the port block diagram.	P.196, P.219, P.240	P.6
8	Correct the port block diagram (added the abbreviation for Schmitt circuit to the input section).	P.199, P.247, P.248, P.249, P.250, P.251, P.252, P.253, P.254, P.257, P.260	P.7
9	Correct the port block diagram (ON/OFF control of the built-in pull-up resistor by the POMxx and PMCxx signals).	P.237 to P.241, P.267, P.270	P.7
10	Correct the description of the port state at reset in "4.2.11 Port 10".	P.258	P.8
11	Correct the information in the "Figure 4-82 Block diagram of P137".	P.276	P.8
12	Add a description of when using the IICA0 function to "4.4.4 Connecting to external devices with different potential (3 V)".	P.330	P.8
13	Correct typos in the "Table 4-31. Settings of Port Mode Register and Output Latch When Using Alternate Function".	P331 to P.340	P.9
14	Add Note 6 at the bottom of Figure 5-5.	P.354	P.10
15	Correct a typo in the Note at the bottom of Figure 5-11.	P.365	P.10

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No	Corrections	R01UH0559EJ0100	Pages in this document
16	Add a Note at the bottom of Figure 5-13.	P.367	P.10
17	Add description to PLLMUL bit in Figure 5-17.	P.371	P.11
18	Add a Caution 14 at the bottom of Figure 5-17.	P.372	P.11
19	Correct typo in Figure 5-24.	P.389	P.11
20	Add a description in Table 5-3.	P.393, P.394	P.11
21	Add a description to chapter “5.6.9”.	P.402	P.12
22	Correct information of Timn/TOmn pin in Figure 6-2.	P.410	P.12
23	Correct typos in the Notes in Chapter “6.3”.	P.419	P.12
24	Correct the description of the CCSmn bit in Figure 6-13.	P.426	P.13
25	Correct Notes in Figure 6-13.	P.430, P.431	P.13
26	Correct the error in the INTTMmn signal in Figure 6-33.	P.463	P.14
27	Correct the error in Figure Title and Figure 6-35.	P.465	P.14
28	Correct typos in Figure 6-42.	P.473	P.15
29	Correct the reference Figure in chapter “6.6.5”.	P.474	P.15
30	Correct information of setting NFENx register in the Figure.	P.485, P.490, P.496, P.501, P.506, P.513, P.514	P.15
31	Correct typo in chapter “6.9.1”.	P.531	P.16
32	Correct access size of registers TRJMR0 and TRJISR0 in Table 7-3.	P.534	P.16
33	Correct the information of WUTMMCK0 bit in Figure 7-3.	P.536	P.16
34	Correct the information of bits PM41 and TEDGSEL in Table 7-7.	P.552	P.16
35	Correct typo at the bottom of Figure 8-40.	P.604	P.16
36	Correct typo in Table 8-14.	P.614	P.16
37	Correct the information of count source clock in chapter “8.5.4”.	P.639	P.17
38	Delete description in Caution 2 at the bottom of Figure 9-2.	P.648	P.17
39	Correct typo of bit 0 in the TIS1 register in Figure 9-4.	P.650	P.17
40	Correct typo in Caution at the bottom of Figure 9-7.	P.653	P.17
41	Add the description of RWAIT bit in Figure 9-8.	P.655	P.17
42	Correct typo of AMPM bit in Table 9-2.	P.658	P.18
43	Add the description of Caution at the bottom of Figure 9-23.	P.668	P.18
44	Add the description of Caution 1 at the bottom of Figure 9-24.	P.669	P.18
45	Correct typo in Remark 1 at the bottom of Figure 9-25.	P.670	P.18
46	Correct the information of “16-bit counter value” in Figure 9-27.	P.674	P.18
47	Correct typo of output latch pin in Figure 10-1.	P.676	P.19
48	Add the description to chapter “11.1”.	P.682	P.19
49	Correct the information of interval time controller in Figure 11-1.	P.683	P.19
50	Correct typo of Caution 2 in chapter “11.4.1”.	P.685	P.19
51	Add the Note in Table 11-4.	P.687	P.19
52	Correct the description of Caution 1 at the bottom of Table 12-3.	P.700 to P.703	P.20
53	Correct the information of INTAD signal in Figure 12-5.	P.704	P.20
54	Correct the information of Caution 2 at the bottom of Figures 12-12 and 12-13.	P.713	P.20
55	Correct the information of “ADCE = 0” in Figures 12-25, 12-26 and 12-27.	P.728 to P.730	P.21
56	Correct the information of ADRCK bit in Figures 12-32 to 12-36.	P.736 to P.740	P.21
57	Correct typo of address of the PER1 register in Figure 13-3.	P.754	P.21
58	Correct typo of address of the PM8 register in Figure 13-7.	P.758	P.21
59	Correct description of Caution 1 in chapter “13.4.2”.	P.761	P.21
60	Correct typo of access size of the PER1 register and register name of PM8 register in Table 14-3.	P.765	P.22
61	Correct the address of the CMPSEL register and description of bits CEGN and CEGP in Figure 14-3.	P.766	P.22
62	Correct the address of the CMPSEL register in Figure 14-4.	P.768	P.22
63	Correct typos in chapter “14.2.4” and Figure 14-5.	P.769	P.22
64	Correct typos in chapter “14.2.7”.	P.772	P.23
65	Correct typo of reference Figure in chapter “14.3.5”.	P.776	P.23
66	Correct the information in Figure 15-1.	P.785	P.24
67	Correct the information in Figure 15-2.	P.786	P.25
68	Correct the information in Figure 15-3.	P.787	P.26

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No	Corrections	R01UH0559EJ0100	Pages in this document
69	Correct the description of Note 1 at the bottom of Figure 15-10.	P.797 to P.798	P.27
70	Correct the description of Note at the bottom of Figure 15-12.	P.800	P.27
71	Correct the description of Note at the bottom of Figure 15-13.	P.801, P.802	P.27
72	Correct typo of SEm register in chapter “15.3.11”.	P.805	P.27
73	Correct typo of Caution at the bottom of Figure 15-18.	P.807	P.27
74	Correct typo of Figure Title of Figure 15-27.	P.817	P.28
75	Correct typos of Remark at the bottom of Figures 15-30, 15-74 and 15-77.	P.825, P.874, P.877	P.28
76	Correct typos of list for slave reception in chapter “15.6.5”.	P.955	P.28
77	Correct typo of SSEm register symbol in Figure 15-142.	P.957	P.28
78	Correct the information of SCRmn.DLSmn[1:0] bit in Figure 15-157.	P.978, P.979	P.29
79	Correct the information of SCRmn.DLSmn[1:0] bit in Figure 15-171.	P.993	P.29
80	Correct description in chapter “15.9.5”.	P.1037	P.30
81	Correct description and add Remark in chapter “16.3.7”.	P.1059	P.30
82	Add the description of Note 3 in chapter “16.4.2”.	P.1064	P.30
83	Correct typo at the bottom of Figure 16-33.	P.1126	P.30
84	Correct description of LDBmn register in chapter “17.2.1 (24)”.	P.1161	P.30
85	Correct description of HTRC flag in chapter “17.2.2 (18)”.	P.1182	P.30
86	Correct description of LDBmn register in chapter “17.2.2 (23)”.	P.1189	P.31
87	Correct description of LUTDRn register in chapter “17.2.3 (24)”.	P.1217	P.31
88	Correct the information of bit error detection in Figure 17-21.	P.1248	P.31
89	Add Caution 5 to chapter “17.5.1 (5)”.	P.1258	P.31
90	Correct the information in Tables 17-21 to 17-24.	P.1259	P.32
91	Correct the information of the LWBRn register in chapter “17.6”.	P.1269 to P.1274	P.33
92	Add the Note of CFSTSk register in chapter “18.3.47”.	P.1383	P.34
93	Add the Note of THLSTSk register in chapter “18.3.75”.	P.1414	P.34
94	Correct typo of the TMCp register symbol in chapter “18.15”.	P.1470	P.35
95	Add the description of CAN interrupt in chapter “18.15”.	P.1470	P.35
96	Correct typo of bits DTCEN20 in Table 20-6.	P.1550	P.35
97	Correct the information of the SELHS0 register in Figure 20-13.	P.1555	P.36
98	Correct the information of the SELHS1 register in Figure 20-14.	P.1556	P.36
99	Correct typos of value of registers DTCCT12 and DTRLD12 in Figure 20-22.	P.1563	P.36
100	Add the description of chain transfer operation in chapter “20.3.4”.	P.1568	P.37
101	Correct typo of Remak at the bottom of Table 21-3.	P.1581	P.37
102	Correct typos of interrupt flag in Table 22-2.	P.1599 to P.1601	P.37
103	Correct the description of Caution in chapter “23.1”.	P.1633	P.38
104	Correct the information of clock state of sub/low-speed OCO in Figure 24-5.	P.1647	P.38
105	Correct typo of OSTS register of Note 2 in Figure 24-6.	P.1651	P.38
106	Correct typo of option byte address in chapter “24.3.3”.	P.1654	P.39
107	Correct the description of Caution and Remark in chapter “26.1”.	P.1670	P.39
108	Correct the information of source clock in Figure 26-3.	P.1674	P.39
109	Correct the information of detection level in chapter “27.1”.	P.1676	P.39
110	Correct the information of LVD circuit in Figure 27-1.	P.1677	P.40
111	Correct typo in Table 27-1.	P.1680	P.40
112	Delete the information of IEC61508 in chapters “28.1 and 28.3.2”.	P.1694, P.1701	P.40
113	Correct typo of Figure Title and bit information of ECCDWRVR register in Figure 28-13.	P.1708	P.41
114	Add the description of “(3) Cautions for use” in chapter “28.3.5”.	P.1715	P.41
115	Correct the information of Remark in Figure 30-4.	P.1734	P.41
116	Add the description of Caution 4 in chapter “31.8.3”.	P.1760	P.41
117	Correct the information of “RAM Area Used” in Table 32-1.	P.1762	P.42
118	Correct typo of reference figure in chapter “32.4.1”.	P.1764	P.42
119	Correct the information of address in Table 34-1.	P.1766	P.42
120	Correct the information of saddrp in Table 34-1.	P.1771	P.42
121	Add the Caution for N-ch open-drain mode in chapters “35.3.1 and 36.3.1”.	P.1799, P.1852	P.43
122	Correct the information of conditions for IOL1 in chapter “35.3.1”.	P.1800	P.43

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No	Corrections	R01UH0559EJ0100	Pages in this document
123	Correct typo of Note 2 in chapters “35.3.2 and 36.3.2”.	P.1809, P.1861	P.43
124	Correct typo in the Notes at the bottom of the table in chapter “35.5.1 (2), (3), (9) and 36.5.1 (2), (3), (9)”.	P.1814, P.1815, P.1825, P.1866, P.1867, P.1876	P.43
125	Correct the information of conditions in chapters “35.5.2 and 36.5.2”.	P.1832, P.1884	P.43
126	Correct the information of conditions for “Overall error” in chapters “35.6.1 and 36.6.1”.	P.1834 to P.1836, P.1886 to P.1888	P.44
127	Correct the information of “target ANI pin” in chapters “35.6.1 and 36.6.1”.	P.1837, P.1889	P.44
128	Add the information of Note and timing figure in chapters “35.6.5 and 36.6.5”.	P.1839, P.1891	P.44
129	Correct chapter title, Note at the bottom of table, and timing figure in chapters “35.8 and 36.8”.	P.1842, P.1894	P.45
130	Correct the information of conditions and Note 1 at the bottom of table in chapters “35.9 and 36.9”.	P.1843, P.1894	P.45

No.1: Update “Table 1-3. Order Information for RL78/F15”

Update 48/64/80/100-pin LQFP products order name.

Table 1-3. Order Information for RL78/F15

Package	Device	Order name
48-pin plastic LFQFP	Grade L	R5F113GKCLFB, R5F113GLCLFB
	Grade K	R5F113GKCKFB, R5F113GLCKFB
48-pin plastic HVQFN	Grade L	R5F113GKLNA, R5F113GLLNA
	Grade K	R5F113GKKNA, R5F113GLKNA
64-pin plastic LFQFP	Grade L	R5F113LKCLFB, R5F113LLCLFB
	Grade K	R5F113LKCKFB, R5F113LLCKFB
80-pin plastic LFQFP	Grade L	R5F113MKCLFB, R5F113MLCLFB
	Grade K	R5F113MKCKFB, R5F113MLCKFB
100-pin plastic LFQFP	Grade L	R5F113PGCLFB, R5F113PHCLFB, R5F113PJCLFB, R5F113PKCLFB, R5F113PLCLFB
	Grade K	R5F113PGCKFB, R5F113PHCKFB, R5F113PJCKFB, R5F113PKCKFB, R5F113PLCKFB
144-pin plastic LFQFP	Grade L	R5F113TGLFB, R5F113THLFB, R5F113TJLFB, R5F113TKLFB, R5F113TLLFB
	Grade K	R5F113TGKFB, R5F113THKFB, R5F113TJKFB, R5F113TKKFB, R5F113TLKFB

No.2: Correct the P40/TOOL0 part in Table 2-4

Change the description of P40/TOOL0 pin in the "Recommended Connection of Unused Pins".

Table 2-4. Connection of Unused Pins (144-Pin Products) (2/4)

Pin Name	I/O	Recommended Connection of Unused Pins
P40/TOOL0	I/O	Input: Independently connect to EV_{DD0} and EV_{DD1} via a resistor or leave open. (Note: For leave open, the condition PU40 = 1.) Output: Leave open.
P41/TI10/TO10/TRJIO0/VCOUT0/ SNZOUT2	I/O	Input: Independently connect to EV_{DD0} and EV_{DD1}, or EV_{SS0} and EV_{SS1} via a resistor. Output: Leave open.
P42/(LTXD0)		
:		

No.3: Correct the “After reset” of MDIV register in Table 3-6

Added a Note 3 to the reset value of MDIV register (F02C7H).

Table 3-6. Extended SFR (2nd SFR) List (12/52)

Address	Special Function Register (2nd SFR) Name	Symbol	R/W	Manipulable Bit Range			After reset
				1-bit	8-bit	16-bit	
:							
F02C7H	f_{MP} clock division register	MDIV	R/W	–	✓	–	00H Note 3
:							

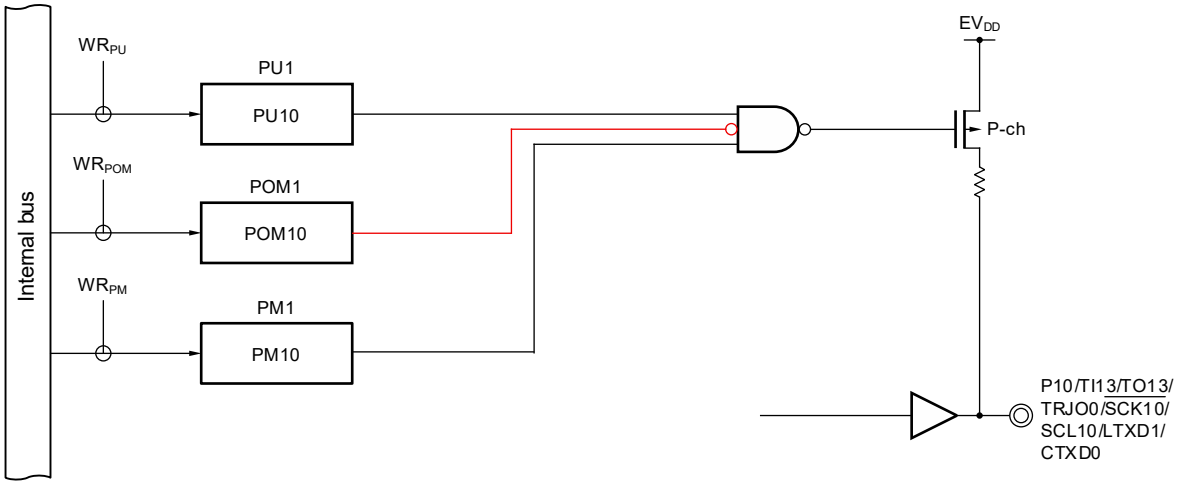
Note 3. The value of the FRQSEL4 bit in the user option byte (000C2H/020C2H) becomes the initial value of the MDIV0 bit in the MDIV register.

No.4: Correct the port block diagram (POMxx signal and built-in pull-up resistor ON/OFF control)

Target: Figures 4-7 to 4-14 (P10 to P17), Figures 4-45 to 4-48 (P60 to P63)

Added signal description for POMxx (N-ch open-drain control) to the control section of the built-in pull-up resistor (as an example, the block diagram for P10 is shown. The red line has been added).

Figure 4-7. Block Diagram of P10



No.5: Add Note (Nch open-drain output and TTL input buffer) to the bottom of the port block diagram

Target: Figure 4-7 (P10), Figure 4-8 (P11), Figure 4-10 (P13), Figure 4-11 (P14), Figure 4-13 (P16), Figure 4-14 (P17), Figure 4-47 (P62), Figure 4-48 (P63), Figure 4-53 (P70), Figure 4-54 (P71)

Cautions 1. The input buffer is enabled even if the pin is operating as an output when the N-ch open drain output mode is selected by the corresponding bit in the port output mode register (POMm). This may lead to a through current flowing through the pin when the voltage level on this pin is intermediate.

2. When the pin is set to TTL input buffer by the corresponding bit in the port input mode register (PIMm) and is driven high, a through current may flow through the pin due to the configuration of the TTL input buffer. When transitioning to standby mode, set the pins to low to reduce current consumption.

No.6: Add Note (Nch open-drain output) to the bottom of the port block diagram

Target: Figure 4-9 (P12), Figure 4-12 (P15), Figure 4-45 (P60), Figure 4-46 (P61), Figure 4-55 (P72), Figure 4-74 (P120)

Caution The input buffer is enabled even if the pin is operating as an output when the N-ch open drain output mode is selected by the corresponding bit in the port output mode register (POMm). This may lead to a through current flowing through the pin when the voltage level on this pin is intermediate.

No.7: Add Note (TTL input buffer) to the bottom of the port block diagram

Target: Figure 4-22 (P30), Figure 4-41 (P54), Figure 4-56 (P73), Figure 4-77 (P125)

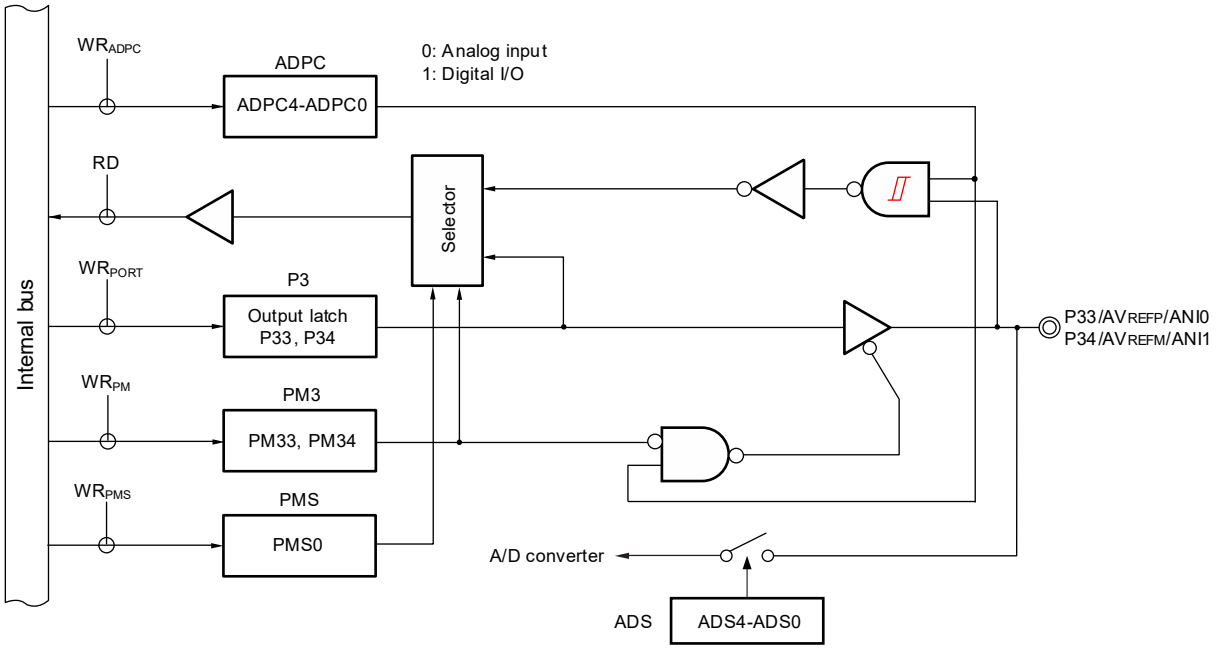
Caution When the pin is set to TTL input buffer by the corresponding bit in the port input mode register (PIMm) and is driven high, a through current may flow through the pin due to the configuration of the TTL input buffer. When transitioning to standby mode, set the pins to low to reduce current consumption.

No.8: Correct the port block diagram (added the abbreviation for Schmitt circuit to the input section)

Target: Figure 4-25 (P33, P34), Figures 4-61 to 4-68 (P80 to P87), Figure 4-69 (P90 to P97), Figure 4-70 (P100 to P105)

Added the abbreviation for the Schmitt circuit to the signal input section of the port (as an example, the block diagram for P33 and P34 is shown. The red line has been added).

Figure 4-25. Block Diagram of P33 and P34

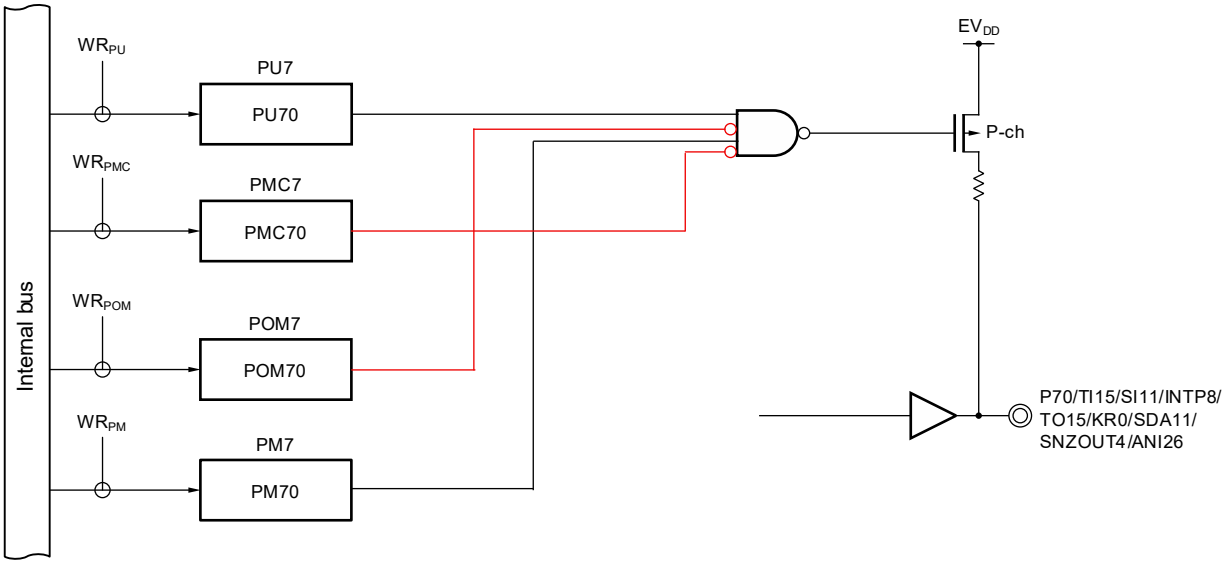


No.9: Correct the port block diagram (built-in pull-up resistor control by the POMxx and PMCxx signals)

Target: Figures 4-53 to 4-57 (P70 to P74), Figure 4-74 (P120), Figure 4-77 (P125)

Added signal descriptions for POMxx (N-ch open-drain control) and PMCxx (analog input selection) to the control section of the built-in pull-up resistor (as an example, the block diagram for P70 is shown. The red line has been added).

Figure 4-53. Block Diagram of P70



No.10: Correct the description of the port state at reset in “4.2.11 Port 10”

4.2.11 Port 10

Port 10 is an I/O port with an output latch. Port 10 can be set to the input mode or output mode in 1-bit units using port mode register 10 (PM10).

When the P106 and P107 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 10 (PU10). For the P107 pin input, the threshold of the input buffer can be specified in 1-bit units using the port input threshold control register 10 (PITHL10).

This port can also be used for A/D converter analog input and LIN serial data I/O.

To use P100/ANI18 to P105/ANI23 as digital I/O pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode or the output mode by using the PM10 register. Use these pins starting from the upper bit.

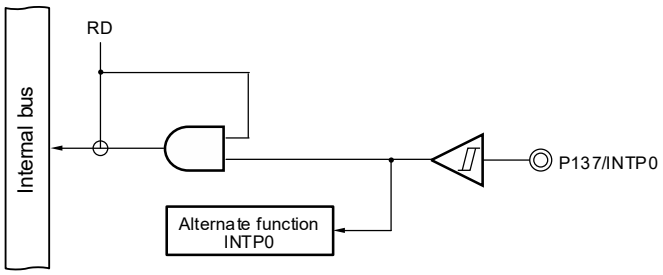
~~Reset signal generation sets this port to input mode.~~

To use P100/ANI18 to P105/ANI23 as analog input pins, set them in the analog input mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM10 register. Use these pins starting from the lower bit.

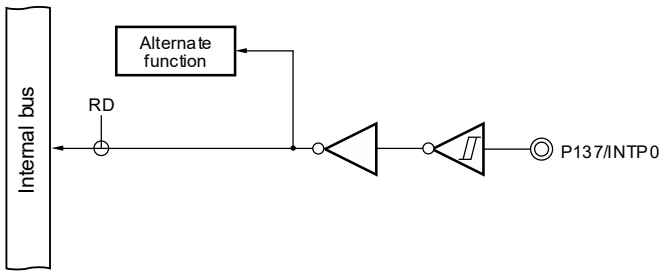
~~Reset signal generation sets this port to analog input mode~~ Reset signal generation sets P100 to P105 to analog input mode and P106 to P107 to input mode.

No.11: Correct the information in the “Figure 4-82 Block diagram of P137”

(Incorrect)



(Correct)



No.12: Add a description of when using the IICA0 function to chapter "4.4.4"

4.4.4 Connecting to external device with different potential (3 V)

(3) Setting procedure when using I/O pins of serial interface IICA0 function

<1> Externally pull up the pin to be used (on-chip pull-up resistor cannot be used). In case of IICA0 function: P62, P63

<2> After reset release, the port mode is the input mode (Hi-Z).

<3> Set the output latch of the corresponding port to 0.

<4> Set the corresponding bit of the POM6 register to 1 to set the N-ch open-drain output (EVDD tolerance) mode.

<5> Set the corresponding bit of the PIM6 register to 1 to switch to the TTL input buffer.

<6> Set the corresponding bit of the PM6 register to the output mode (data I/O is possible in the output mode).

<7> Enable the operation of the serial interface IICA0 function.

No.13: Correct typos in the Table 4-31

Table 4-31. Settings of Port Mode Register and Output Latch When Using Alternate Function

Pin Name	Alternate Function		PIORXX	POMXX	PMCXX	PMXX	PXX	PIMXX	PITHLXX
	Function Name	I/O							
P04	INTP15	Input	~~0~~ —	—	—	1	×	—	—
P10	TRJO0	Output	~~×~~ —	0	—	0	0	×	×
P11	CRXD0	Input	0	×	—	1	×	0	~~0/1~~ 0
P12	INTP5	Input	~~×~~ —	×	—	1	×	—	—
P14	TRDIOC0	Input	~~×~~ —	×	—	1	×	0	0/1
		Output	~~×~~ —	0	—	0	0	×	×
P15	TRDIOA1	Input	~~×~~ —	×	—	1	×	—	—
		Output	~~×~~ —	0	—	0	0	—	—
P16	TRDIOC1	Input	~~×~~ —	×	—	1	×	0	0/1
		Output	~~×~~ —	0	—	0	0	×	×
P17	TRDIOB1	Input	~~×~~ —	×	—	1	×	0	0/1
		Output	~~×~~ —	0	—	0	0	×	×
P30	TRDIOD1	Input	~~×~~ —	—	—	1	×	0	0/1
		Output	~~×~~ —	—	—	0	0	×	×
P31	STOPST	Output	~~×~~ —	—	—	0	0	—	—
P32	INTP7	Input	~~×~~ —	—	—	1	×	—	—
P33	ANI0 Note 1	Input	~~×~~ —	—	—	1	×	—	—
	AV_{REFP} Note 1	Input	~~×~~ —	—	—	1	×	—	—
P34	ANI0 Note 1	Input	~~×~~ —	—	—	1	×	—	—
	AV_{REFM} Note 1	Input	~~×~~ —	—	—	1	×	—	—
P37	(CRXD1)	Input	1	—	—	1	×	—	~~0/1~~ 0
P40	TOOL0	I/O	~~×~~ —	—	—	×	×	—	—
P41	TRJIO0	Input	~~×~~ —	—	—	1	×	—	—
		Output	~~×~~ —	—	—	0	0	—	—
	VCOUT0	Output	~~×~~ —	—	—	0	0	—	—
P47	INTP13	Input	~~×~~ —	—	—	1	×	—	—
P51	INTP11	Input	~~×~~ —	—	—	1	×	—	—
P52	(STOPST) ~~Note~~ Note 2	Output	~~×~~ —	—	—	0	0	—	—
P53	INTP10	Input	~~×~~ —	—	—	1	×	—	0/1
P60	CRXD1	Input	0	×	—	1	×	—	~~0/1~~ 0
P62	SCLA0	I/O	~~×~~ —	1	—	0	0	0/1	0/1
P63	SDAA0	I/O	~~×~~ —	1	—	0	0	0/1	0/1
P70	ANI26	Input	~~×~~ —	×	1	1	×	×	×
	INTP8	Input	~~×~~ —	×	0	1	×	0	0/1
P71	ANI27	Input	~~×~~ —	×	1	1	×	×	×
	INTP6	Input	~~×~~ —	×	0	1	×	0	0/1
P72	ANI28	Input	~~×~~ —	×	1	1	×	—	—
P73	ANI29	Input	~~×~~ —	—	1	1	×	×	×
	(CRXD0)	Input	1	—	0	1	×	0	~~0/1~~ 0
P74	ANI30	Input	~~×~~ —	—	1	1	×	—	—
P77	INTP12	Input	~~×~~ —	—	—	1	×	—	0/1
P80	ANI2 Note 1	Input	~~×~~ —	—	—	1	×	—	—
	ANO0 Note 1	Output	~~×~~ —	—	—	1	×	—	—
P81	ANI3 Note 1	Input	~~×~~ —	—	—	1	×	—	—
	IVCMP00 Note 1	Input	~~×~~ —	—	—	1	×	—	—
P82	ANI4 Note 1	Input	~~×~~ —	—	—	1	×	—	—
	IVCMP01 Note 1	Input	~~×~~ —	—	—	1	×	—	—
P83	ANI5 Note 1	Input	~~×~~ —	—	—	1	×	—	—
	IVCMP02 Note 1	Input	~~×~~ —	—	—	1	×	—	—
P84	ANI6 Note 1	Input	~~×~~ —	—	—	1	×	—	—
	IVCMP03 Note 1	Input	~~×~~ —	—	—	1	×	—	—

Notes 1. It must be assigned to analog input by setting the A/D port configuration register (ADPC).

2. The STOPST function can be assigned via settings in the STOP status output control register (STPSTC).

Table 4-31. Settings of Port Mode Register and Output Latch When Using Alternate Function

Pin Name	Alternate Function		PIORXX	POMXX	PMCXX	PMXX	PXX	PIMXX	PITHLXX
	Function Name	I/O							
P85	ANI7Note	Input	~~×~~ —	—	—	1	×	—	—
	IVREF0Note	Input	~~×~~ —	—	—	1	×	—	—
P86-P87	ANI8-ANI9Note	Input	~~×~~ —	—	—	1	×	—	—
P90-P97	ANI10-ANI17Note	Input	~~×~~ —	—	—	1	×	—	—
P100-P105	ANI18-ANI23Note	Input	~~×~~ —	—	—	1	×	—	—
P120	ANI25	Input	~~×~~ —	×	1	1	×	—	—
	INTP4	Input	~~×~~ —	×	0	1	×	—	—
P125	ANI24	Input	~~×~~ —	—	1	1	×	×	×
	INTP1	Input	~~×~~ —	—	0	1	×	0	0/1
P130	RESOUT	Output	~~×~~ —	—	—	—	0	—	—
P131	INTP14	Input	~~×~~ —	—	—	1	×	—	—
P137	INTP0	Input	~~×~~ —	—	—	—	×	—	—
P140	PCLBUZ0	Output	~~×~~ —	—	—	0	0	—	—
P154	LRXD2	Input	~~×~~ —	—	—	1	×	—	0/1
P155	LTXD2	Output	~~×~~ —	—	—	0	0	—	—

Note It must be assigned to analog input by setting the A/D port configuration register (ADPC).

No.14: Add Note 6 at the bottom of Figure 5-5

Figure 5-5. Format of Clock Operation Status Control Register (CSC)

Caution 6. The setting of the flags of the register to stop clock oscillation (invalidate the external clock input) and the condition before clock oscillation is to be stopped are as Table 5-2. Before stopping the clock oscillation, check the conditions.

No.15: Correct a typo in the Note at the bottom of Figure 5-11

Figure 5-11. Format of Operation Speed Mode Control Register (OSMC)

WUTMMCK0 Note	Low-speed on-chip oscillator control
0	Low-speed on-chip oscillator stopped
1	Low-speed on-chip oscillator operating

Note To stop the low-speed on-chip oscillator, set bit 4 (WUTMMCK0) to 0 and ~~bit 1~~ bit 0 (SELLOSC) of the clock select register (CKSEL) to 0.

No.16: Add a Note at the bottom of Figure 5-13

Figure 5-13. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H リセット時：注 R/W

略号	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
			⋮			
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The reset value differs for each chip.

Remark The HIOTRM register holds a six-bit value used to adjust the high-speed on-chip oscillator with an increment of 1 corresponding to an increase of frequency by about 0.05%.

No.17: Add description to PLLMUL bit in Figure 5-17

Figure 5-17. Format of PLL Control Register (PLLCTL)

PLLMUL	Control of PLL multiplication selection
0	Multiplies the clock frequency by 12.
1	Multiplies the clock frequency by 16.
After setting the PLLMUL bit, wait 1 μs or more before setting the PLLON bit to 1.	

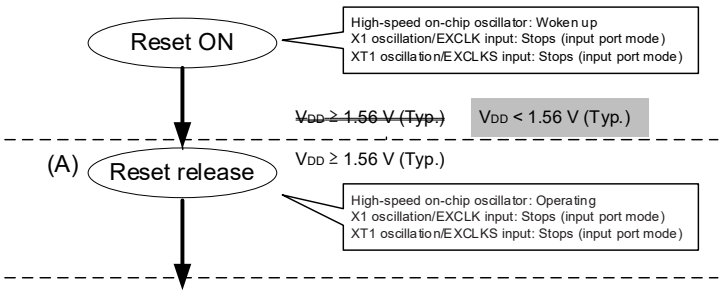
No.18: Add a Caution 14 at the bottom of Figure 5-17

Cautions 13. To change the SELPLL bit from 1 to 0 while PLLDIV1 = 1 (fPLL > 32 MHz), stop counting by the timer RD (setting the TSTART0 and TSTART1 bits in the TRDSTR register to 0) before changing the SELPLL bit.

14. Do not change the value of LCKSEL1, LCKSEL0, PLLDIV1, PLLDIV0, and PLLMUL bits while the PLLON bit is set to 1.

No.19: Correct typo in Figure 5-24

Figure 5-24. CPU Clock Status Transition Diagram



No.20: Add a description in Table 5-3

Table 5-3. Changing CPU Clock

CPU Clock		Conditions before Change	Processing after Change
Before Change	After Change		
High-speed on-chip oscillator clock	X1 clock	X1 oscillation is stable. • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time	~~Stopping the high-speed on-chip oscillator (HIOSTOP = 1) can reduce the operating current.~~ The operating current can be reduced by stopping the highspeed on-chip oscillator (HIOSTOP = 1) after checking that the CPU clock is changed.
	External main system clock	External clock input from the EXCLK pin is enabled. • OSCSEL = 1, EXCLK = 1, MSTOP = 0	
	:	:	
X1 clock	High-speed on-chip oscillator clock	The high-speed on-chip oscillator starts oscillation. • HIOSTOP = 0	~~The external main system clock input can be disabled. (MSTOP = 1)~~ X1 oscillation can be stopped (MSTOP = 1) after checking that the CPU clock is changed.
	External main system clock	Prohibited to change. (To change the CPU clock, clear the settings first and then reset the settings.)	–
	XT1 clock	XT1 oscillation is stable, and the subsystem clock is selected as the subsystem/low-speed on-chip oscillator select clock. • OSCSELS = 1, EXCLKS = 0, XTSTOP = 0 • SELLOSC = 0 • After elapse of oscillation stabilization time	~~The external main system clock input can be disabled. (MSTOP = 1)~~ X1 oscillation can be stopped (MSTOP = 1) after checking that the CPU clock is changed.
	:	:	
	PLL clock	PLL oscillation is stable. • LOCK = 1, PLLON = 1	The X1 clock cannot be stopped because it is the PLL input clock.

No.21: Add a description to chapter “5.6.9”

5.6.9 Conditions Before Clock Oscillation Is Stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped. Before stopping the clock oscillation, check the conditions before the clock oscillation is stopped.

No.22: Correct information of Timn/TOmn pin in Figure 6-2

Table 6-2. Timer I/O Pins provided in Each Product

Timer array unit channels		I/O Pins of Each Product	
		144-pin	~~100-pin~~ 100/80/64/48-pin
Unit 0	Channel 0	~~P17/TI00/TO00~~ TI00/TO00	
	Channel 1	~~P30/TI01/TO01~~ TI01/TO01	
	Channel 2	~~P16/TI02/TO02~~ TI02/TO02	
	Channel 3	~~P125/TI03/TO03~~ TI03/TO03	
	Channel 4	~~P13/TI04/TO04~~ TI04/TO04	
	Channel 5	~~P15/TI05/TO04~~ TI05/TO05	
	Channel 6	~~P14/TI06/TO06~~ TI06/TO06	
	Channel 7	~~P120/TI07/TO07~~ TI07/TO07	
Unit 1	Channel 0	~~P41/TI10/TO10~~ TI10/TO10	
	Channel 1	~~P12/TI11/TO11~~ TI11/TO11	
	Channel 2	~~P11/TI12/TO12~~ TI12/TO12	
	Channel 3	~~P10/TI13/TO13~~ TI13/TO13	
	Channel 4	~~P31/TI14/TO14~~ TI14/TO14	
	Channel 5	~~P70/TI15/TO14~~ TI15/TO15	
	Channel 6	~~P32/TI16/TO16~~ TI16/TO16	
	Channel 7	~~P71/TI17/TO17~~ TI17/TO17	
Unit 2	Channel 0	~~P110/TI20/TO20~~ TI20/TO20	×
	Channel 1	~~P111/TI21/TO21~~ TI21/TO21	×
	Channel 2	~~P112/TI22/TO22~~ TI22/TO22	×
	Channel 3	~~P113/TI23/TO23~~ TI23/TO23	×
	Channel 4	~~P114/TI24/TO24~~ TI24/TO24	×
	Channel 5	~~P115/TI25/TO25~~ TI25/TO25	×
	Channel 6	~~P116/TI26/TO26~~ TI26/TO26	×
	Channel 7	~~P117/TI27/TO27~~ TI27/TO27	×

No.23: Correct typos in the Notes in Chapter “6.3”

6.3 Registers Controlling Timer Array Unit

- PWM output delay control register 1 (PWMDLY1)
- PWM output delay control register 2 (PWMDLY2)
- PWM output delay control register 3 (PWMDLY3) Note 2
- Noise filter enable registers 1, 2, 3 (NFEN1, NFEN2, NFEN3) Note 2
- Port mode register (PMxx) ~~Note~~ Note 1
- Port register (Pxx) ~~Note~~ Note 1
- Unit select register (UTSEL) Note 2

Notes 1. The port mode registers (PMxx) and port registers (Pxx) to be set differ depending on the product. For details, see 6.3.17 Port mode registers 0, 1, 3, 4, 5, 6, 7, 11, 12, 14 (PM0, PM1, PM3, PM4, PM5, PM6, PM7, PM11, PM12, PM14).

2. PWM output delay control register (PWMDLY3), unit select register (UTSEL) and noise filter enable register (NFEN3) are incorporated only in 144-pin products.

No.24: Correct the description of the CCSmn bit in Figure 6-13

Figure 6-13 Format of Timer Mode Register mn (TMRmn) (1/4)

CCS mn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin ~~Valid edge of input signal selected by TIS1 in TAU0 channel 5~~ When using unit 0: In channel 0 to 3, Valid edge of input signal selected by TIS0 In channel 4 to 7, Valid edge of input signal selected by TIS1 When using unit 1: In channel 6 and 7, Valid edge of input signal selected by TIS2
Count clock (f_{TCLK}) is used for the timer/counter, output controller, and interrupt controller.	

No.25: Correct Notes in Figure 6-13

Figure 6-13 Format of Timer Mode Register mn (TMRmn) (4/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07), F01D0H, F01D1H (TMR10) to F01DEH, F01DFH (TMR17), F01D0H, F01D1H (TMR20) to F01DEH, F01DFH (TMR27) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0 ~~Note~~ Note 1	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD mn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode ~~Note 1~~ Note 2 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation ~~Note 2~~ Note 3. At that time, ~~interrupt is also generated~~ interrupt is not generated, either.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Notes 1. Bit 11 is a read-only bit and fixed to 0. Writing to this bit is ignored.

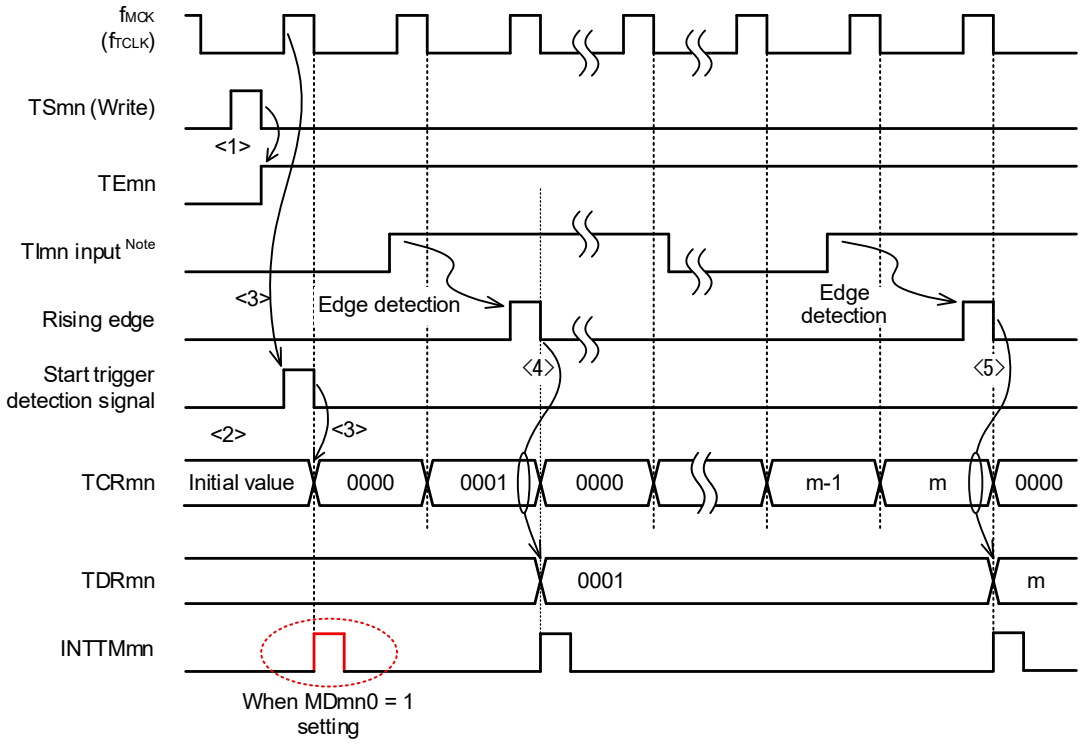
2. In one-count mode, interrupt output (INTTMmn) when starting a count operation and TOmn output are not controlled.

3. If the start trigger (TSmn = 1) is issued during operation, the counter is initialized and recounting is started (no interrupt request is generated).

No.26: Correct the error in the INTTMmn signal in Figure 6-33

When MDmn0 = 1, an interrupt request (INTTMmn) is generated when counting starts. The red line has been added.

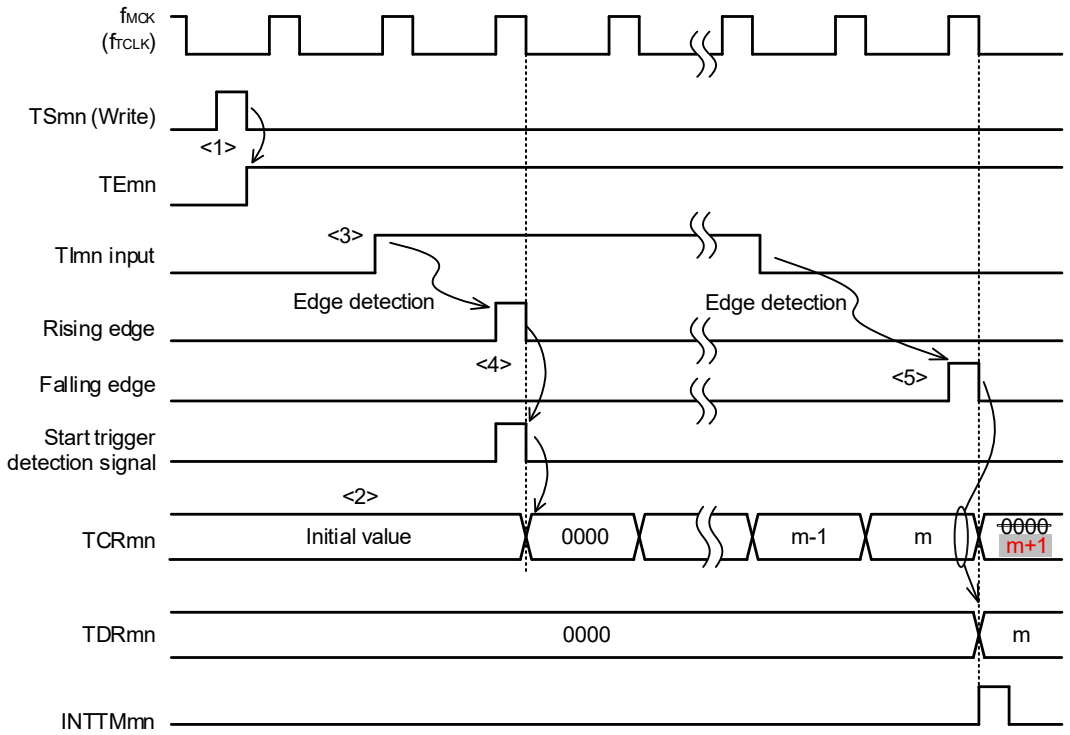
Figure 6-33 Operation Timing (In Capture Mode : Input Pulse Interval Measurement)



No.27: Correct the error in Figure Title and Figure 6-35

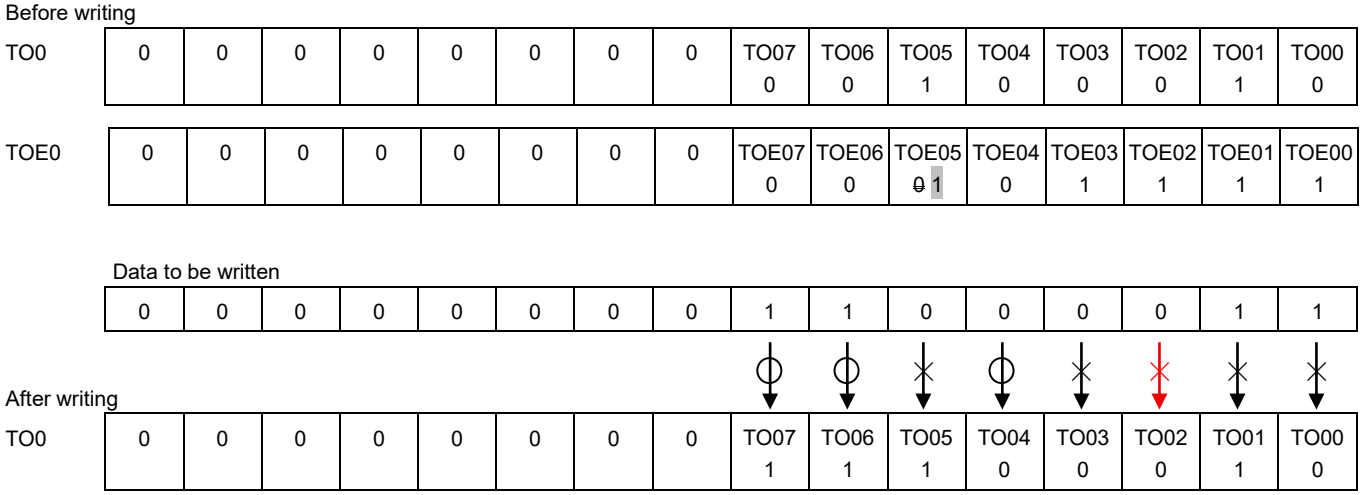
Under these conditions, TCRmn becomes 0000H when a rising edge is detected.

Figure 6-35 Operation Timing (In Capture & One-count Mode: High-level Width Measurement)



No.28: Correct typos in Figure 6-42

Figure 6-42 Example of TO0n Bit Collective Manipulation



No.29: Correct the reference Figure in chapter “6.6.5”

6.6.5 Timer Interrupt and TOmn Pin Output at Operation Start

In the interval timer mode or capture mode, the MDmn0 bit in timer mode register mn (TMRmn) sets whether or not to generate a timer interrupt at count start.

When MDmn0 is set to 1, the count operation start timing can be known by the timer interrupt (INTTMmn) generation.

In the other modes, neither timer interrupt at count operation start nor TOmn output is controlled.

~~Figures 6-37~~ Figure 6-44 shows operation examples when the interval timer mode (TOEmn = 1, TOMmn = 0) is set.

No.30: Correct information of setting NFENx register in the Figure

Target: Figure 6-52, Figure 6-56, Figure 6-60, Figure 6-64, Figure 6-68, Figure 6-73

Move the setting location for the Noise Filter Enable Registers (NFEN1, 2, 3) from "During operation" to "Channel default setting" (as an example, Figure 6-52 shows the operating procedure when using the external event counter function).

Figure 6-52 Operation Procedure When External Event Counter Function Is Used

	Software Operation	Hardware Status
TAU default setting	:	:
Channel default setting	Sets corresponding bit of noise filter enable registers 1, 2 and 3 (NFEN1, NFEN2 and NFEN3) to 1. Sets timer mode register mn (TMRmn) (determines operation mode of channel). Sets number of counts to timer data register mn (TDRmn). Clears the TOEmn bit of timer output enable register m (TOEm) to 0.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	:	:
During operation	Set value of the TDRmn register can be changed. ~~Sets corresponding bit of noise filter enable registers 1, 2 and 3 (NFEN1, NFEN2 and NFEN3) to 1.~~ The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	Counter (TCRmn) counts down each time input edge of the TImn pin has been detected. When count value reaches 0000H, the value of the TDRmn register is loaded to the TCRmn register again, and the count operation is continued. By detecting TCRmn = 0000H, the INTTMmn output is generated. After that, the above operation is repeated.
Operation stop	:	:
TAU stop	:	:

Operation is resumed.

No.31: Correct typo in chapter “6.9.1”

6.9.1 Cautions When Using Timer output

(1) When the ~~PCLK~~ f_{CLK} (not divided) is selected as the operating clock for the timer array unit and ~~TDRnm (n = 0 to 2; m = 0 to 7)~~ TDRmn (m = 0 to 2, n = 0 to 7) are set to 0000H, an interrupt signal from the timer array unit is fixed to high, and an interrupt request cannot be detected.
To use this setting, the interrupt function should be masked.

No.32: Correct access size of registers TRJMR0 and TRJISR0 in Table 7-3

Table 7-3. Timer RJ Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RJ Mode Register 0	TRJMR0	00H	F0242H	~~8~~ 1, 8
Timer RJ Event Pin Select Register 0	TRJISR0	00H	F0243H	~~8~~ 1, 8

No.33: Correct the information of WUTMMCK0 bit in Figure 7-3

Figure 7-3. Format of Operation Speed Mode Control Register (OSMC)

WUTMMCK0	Low-speed on-chip oscillator operation control
0	Low-speed on-chip oscillator ~~operating~~ stopped
1	Low-speed on-chip oscillator ~~stopped~~ operating

No.34: Correct the information of bits PM41 and TEDGSEL in Table 7-7

Table 7-7. TRJIO0 Pin Setting

Operating Mode	PM4 Register ~~PMXX Bit~~ Note PM41 Bit	TRJIOC0 Register TEDGSEL Bit	TRJIO0 Pin I/O
Timer mode	0 or 1	0 or 1	Input (Not used)
Pulse output mode	1	0 or 1	Output disabled (Hi-z output)
	0	1	Normal output
		0	Inverted output
Event counter mode	1	0 or 1	Input
Pulse width measurement mode			
Pulse period measurement mode			

~~**Note** The port mode register (PMxx) bit corresponding to port multiplexed with TRJIO0 function.~~

No.35: Correct typo at the bottom of Figure 8-40

Figure 8-40. Count Source Block Diagram

Remark ~~TDC_CKSEL~~ TRD_CKSEL: Bit in CKSEL register

No.36: Correct typo in Table 8-14

Table 8-14. Input Capture Function Specifications

Item	Specification
Count sources Note	f_{CLK}, f_{PLL}, f_{IH}, f_{SUB}, ~~f_{PL}~~ f_{IL} External signal input to the TRDCLK0 pin (active edge selected by a program)
:	:

No.37: Correct the information of count source clock in chapter “8.5.4”

8.5.4 Input Capture Function

- In input capture mode, an input capture interrupt request for the active edge of the TRDIOji input is also generated when the ~~TRDTSTARTi~~ TSTARTi bit in the TRDSTR register is 0 (count stops) if the edge selected by bits TRDIOj0 and TRDIOj1 in the TRDIORji register is input to the TRDIOji pin (i = 0 or 1; j = A, B, C, or D). Set the pulse width of the input capture signal to three or more cycles of the timer RD operating clock (f_{TRD}).

No.38: Delete description in Caution 2 at the bottom of Figure 9-2

Figure 9-2. Format of Peripheral Enable Register 0 (PER0)

Caution 2. Clock supply to peripheral functions other than the real-time clock can be stopped in HALT mode when the subsystem/low-speed on-chip oscillator select clock is used, by setting the RTCLPC bit of the operation speed mode control register (OSMC) to 1. ~~In this case, set the RTCEN bit of the PER0 register to 1 and the other bits (bits 0 to 6) to 0.~~

No.39: Correct typo of bit 0 in the TIS1 register in Figure 9-4

Figure 9-4. Format of Timer Input Select Register 1 (TIS1)

Address: F0075H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS1	TIS17	TIS16	0	TIS14	0	TIS12	0	~~TIS0~~ TIS10

No.40: Correct typo in Caution at the bottom of Figure 9-7

Figure 9-7. Format of Real-time Clock Control Register 0 (RTCC0)

Address: FFF9DH After reset: 00H R/W

Symbol	<7>	6	<5>	4	3	2	1	0
RTCC0	RTCE	0	RCLOE1	0	AMPM	CT2	CT1	CT0

Caution Do not change the value of the ~~RTCLOE1~~ RCLOE1 bit when RTCE = 1.

No.41: Add the description of RWAIT bit in Figure 9-8

Figure 9-8. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value.

This bit controls the operation of the counter.
Be sure to write “1” to it to read or write the counter value.
As the internal counter (16 bits) is continuing to run, complete reading or writing within one second and turn back to 0.
When RWAIT = 1, it takes up to 1 operating clock (f_{RTC}) until the counter value can be read or written (RWST = 1). Notes 1, 2

When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second).
Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.
When the internal counter (16 bits) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

No.42: Correct typo of AMPM bit in Table 9-2

Table 9-2. Displayed Time Digits

24-Hour Display (AMPM = 1)		12-Hour Display (~~AMPM = 1~~ AMPM = 0)	
Time	Hour Register	Time	Hour Register
0	00H	12 a.m.	12H
:	:	:	:

No.43: Add the description of Caution at the bottom of Figure 9-23

Figure 9-23. Procedure for Reading Real-time Clock

Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

No.44: Add the description of Caution 1 at the bottom of Figure 9-24

Figure 9-24. Procedure for Writing Real-time Clock

Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

No.45: Correct typo in Remark 1 at the bottom of Figure 9-25

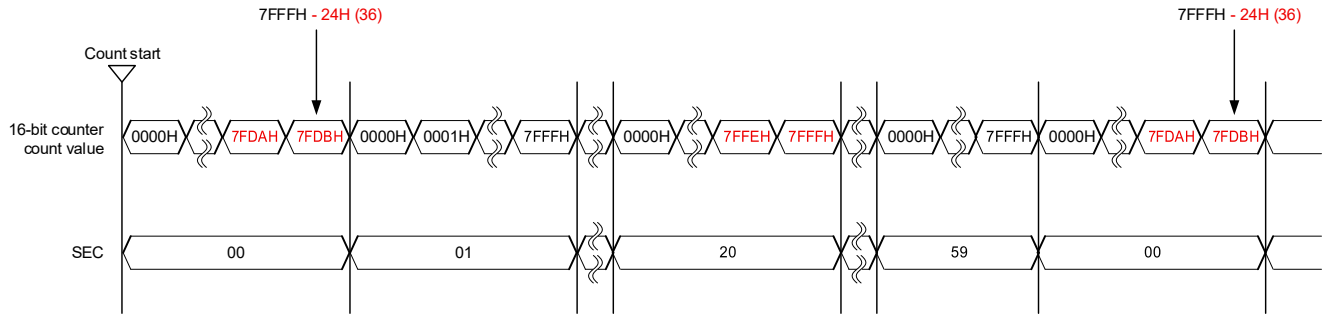
Figure 9-25. Alarm Setting Procedure

Remarks 1. The alarm week register (~~ALARMWW~~ ALARMWM), alarm hour register (ALARMWH), and alarm week register (ALARMWW) may be written in any sequence.

No.46: Correct the information of “16-bit counter value” in Figure 9-27

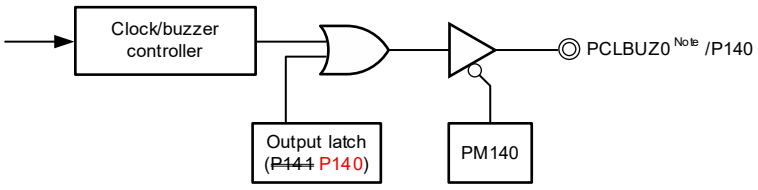
The conditions and diagram are different, so we will make corrections (correct the parts written in red).

Figure 9-27. Operation when (DEV, F12, F11, F10, F9, F8, F7, F6, F5, F4, F3, F2, F1, F0) = (1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 1, 1, 1, 0)



No.47: Correct typo of output latch pin in Figure 10-1

Figure 10-1. Block Diagram of Clock Output/Buzzer Output Controller



No.48: Add the description to chapter "11.1"

11.1 Functions of Watchdog Timer

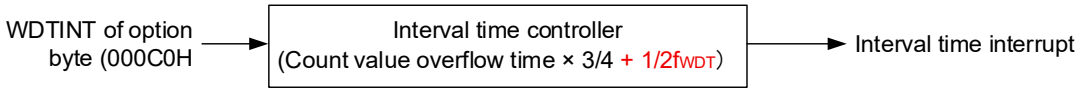
When a reset occurs due to the watchdog timer, bit 4 (WDCLRF) of the reset control flag register (RESF) is set to 1. For details of the RESF register, see **CHAPTER 25 RESET FUNCTION**.

When 75% of the overflow time + 1/2 f_{WDT} is reached, an interval interrupt can be generated.

Caution If "window open period" is set to 75 % (WINDOW1, WINDOW0 = 10B), please perform counter-clear within the period except for just 50%.

No.49: Correct the information of interval time controller in Figure 11-1

Figure 11-1. Block Diagram of Watchdog Timer



No.50: Correct typo of Caution 2 in chapter "11.4.1"

11.4.1 Controlling operation of watchdog timer

Caution 2. If the watchdog timer counter is cleared by writing "ACH" to the WDTE register, the actual overflow time may be different from the overflow time set by the option byte by up to ~~2/fIL~~ 2/f_{WDT} seconds.

No.51: Add the Note in Table 11-4

Table 11-4. Setting Window Open Period of Watchdog Timer

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	Setting prohibited
0	1	50 %
1	0	75 % Note
1	1	100 %

Note When the window open period is set to 75%, clearing the counter of the watchdog timer (writing ACH to WDTE) must proceed outside the corresponding period from among those listed below, over which clearing of the counter is prohibited (for example, confirming that the interval timer interrupt request flag (WDTIIF) of the watchdog timer is set).

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time (f_{WDT} = 17.25 kHz (MAX.))	Period over which clearing the counter is prohibited when the window open period is set to 75%
0	0	0	$2^6/f_{WDT}$ (3.71 ms)	1.85 ms to 2.51 ms
0	0	1	$2^7/f_{WDT}$ (7.42 ms)	3.71 ms to 5.02 ms
0	1	0	$2^8/f_{WDT}$ (14.84 ms)	7.42 ms to 10.04 ms
0	1	1	$2^9/f_{WDT}$ (29.68 ms)	14.84 ms to 20.08 ms
1	0	0	$2^{11}/f_{WDT}$ (118.72 ms)	59.36 ms to 80.32 ms
1	0	1	$2^{13}/f_{WDT}$ (474.89 ms)	237.44 ms to 321.26 ms
1	1	0	$2^{14}/f_{WDT}$ (949.79 ms)	474.89 ms to 642.51 ms
1	1	1	$2^{16}/f_{WDT}$ (3799.18 ms)	1899.59 ms to 2570.04 ms

No.52: Correct the description of Caution 1 at the bottom of Table 12-3

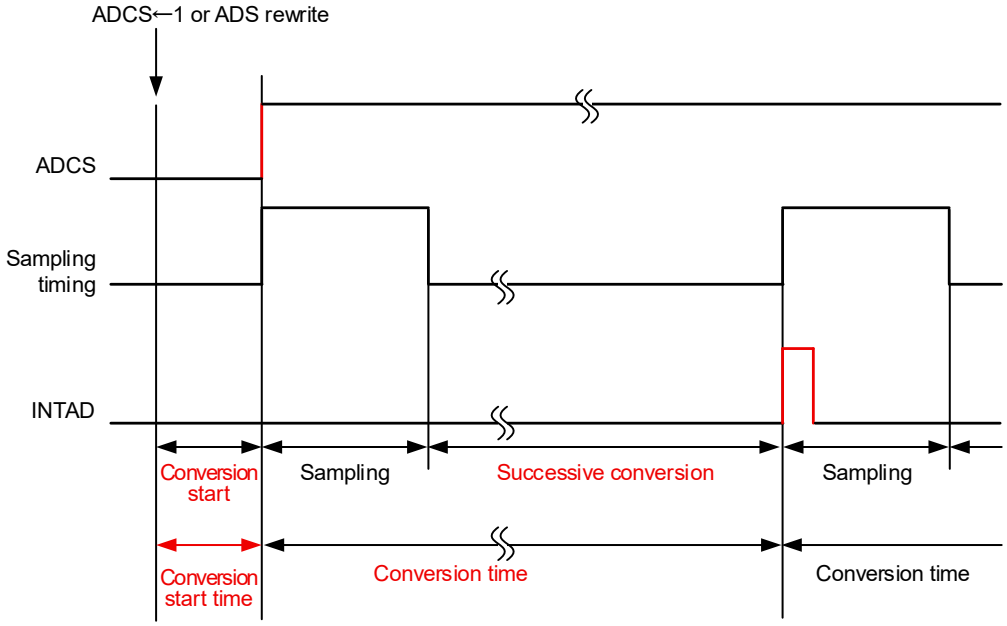
Table 12-3. A/D Conversion Time Selection

Cautions 1. When rewriting the FR2 to FR0, LV1, and LV0 bits to other than the same data, ~~stop A/D conversion once (ADCS = 0) beforehand~~ while conversion is stopped (ADCS = 0, ADCE = 0).

No.53: Correct the information of INTAD signal in Figure 12-5

The changes are indicated by red lines and text.

Figure 12-5. A/D Converter Sampling and A/D Conversion Timing (Example for Software Trigger Mode)



No.54: Correct the information of Caution 2 at the bottom of Figures 12-12 and 12-13

Figure 12-12. Format of Conversion Result Comparison Upper Limit Setting Register (ADUL)

Caution 2. Writing new values to the ADUL and ADLL registers is prohibited while conversion is enabled. Write new values to these registers while conversion is stopped (ADCE = 0, ADCS = 0).

Figure 12-13. Format of Conversion Result Comparison Lower Limit Setting Register (ADLL)

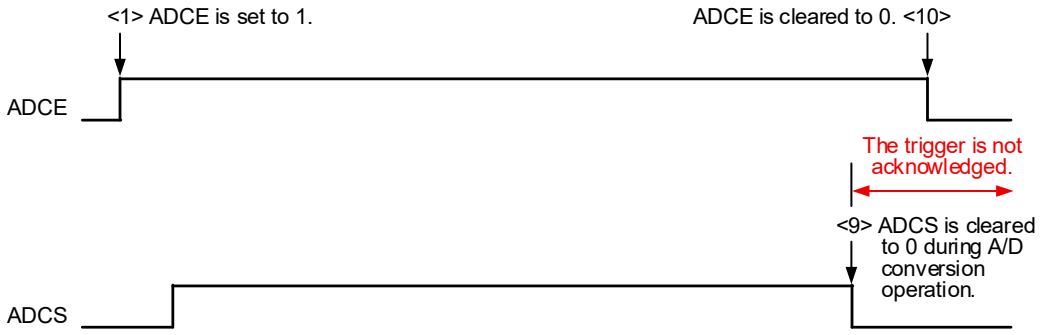
Caution 2. Writing new values to the ADUL and ADLL registers is prohibited while conversion is enabled. Write new values to these registers while conversion is stopped (ADCE = 0, ADCS = 0).

No.55: Correct the information of “ADCE = 0” in Figures 12-25, 12-26 and 12-27

Target: Figure 12-25, Figure 12-26, Figure 12-27

Corrected the "Trigger standby status" in the "ADCE = 0 setting" section of the timing diagram (see Figure 12-25 as an example. The parts in red are the changes).

Figure 12-25. Example of Hardware Trigger No-Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing



No.56: Correct the information of ADRCK bit in Figures 12-32 to 12-36

Corrected the description of the ADM2 register setting section in the flowchart.

Incorrect: • ADM2 register

ADREFP1, ADREFP0, and ADREFM bits: These are used to select the reference voltage source.

ADRCK bit: This is used to select the range of values for comparison with the result of A/D conversion in the generation of interrupt signals in response to results being in either area 1 or areas 3 and 2.

ADTYP bit: 8-bit/10-bit resolution

Correct: • ADM2 register

ADREFP1, ADREFP0, and ADREFM bits: These are used to select the reference voltage source.

ADRCK bit: Set the ADRCK bit to 0 or 1.

ADTYP bit: 8-bit/10-bit resolution

No.57: Correct typo of address of the PER1 register in Figure 13-3

Figure 13-3. Format of Peripheral Enable Register 1 (PER1)

Address: ~~F007AH~~ F02C0H After reset: 00H

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER1	DACEN	0	CMPEN	TRD0EN	DTCEN	TAU2EN Note	SAU2EN	TRJ0EN

No.58: Correct typo of address of the PM8 register in Figure 13-7

Figure 13-7. Format of Port Mode Register 8 (PM8)

Address: ~~FFF22H~~ FFF28H After reset: FFH

Symbol	7	6	5	4	3	2	1	0
PM8	PM87	PM86	PM85	PM84	PM83	PM82	PM81	PM80

No.59: Correct description of Caution 1 in chapter “13.4.2”

13.4.2 Operation in Real-Time Output Mode

Cautions 1. ~~Even if 1, 0, and then 1 is set to the DACE0 bit~~ Even if the DACE0 bit setting is 1 to 0 and then 1, there is a wait after 1 is set for the last time.

No.60: Correct typo of access size of the PER1 register and register name of PM8 register in Table 14-3

Table 14-3. Registers to Control the Comparator

Register Name	Symbol	After Reset	Address	Access Size
Peripheral Enable Register 1	PER1	00H	F02C0H	~~8~~ 1, 8
~~Port mode register~~ Port mode register 8	PM8	FFH	FFF28H	1, 8

No.61: Correct the address of the CMPSEL register and description of bits CEGN, CEGP in Figure 14-3

Figure 14-3. Format of Comparator Control Register (CMPCTL)

Address: ~~F0341H~~ F02A0H After reset: 00H

Symbol	<7>	6	5	4	3	2	1	0
CMPCTL	HCMPON	CDFS1	CDFS0	CEGN	CEGP	CSTEN	COE	CINV

CEGN	CEGP	Selection of valid edge of INTCMP interrupt signal	R/W
0	0	No edge selection	R/W
0	1	~~Falling edge selection~~ Rising edge selection	
1	0	~~Rising edge selection~~ Falling edge selection	
1	1	Both-edge selection	
The valid edge is set for the signal after the comparator polarity is selected by using the CINV bit and the filter is selected by using CDFS1 and CDFS0 bits.			

No.62: Correct the address of the CMPSEL register in Figure 14-4

Figure 14-4. Format of Comparator I/O Select Register (CMPSEL)

Address: ~~F0340H~~ F02A1H After reset: 00H

Symbol	7	<6>	5	4	3	2	1	0
CMPSEL	0 Note 4	CPOE	CVRS1	CVRS0	CMPSEL3	CMPSEL2	CMPSEL1	CMPSEL0

No.63: Correct typos in chapter “14.2.4” and Figure 14-5

14.2.4 Comparator Output Monitor Register (CMPMON)

This register is used to monitor the comparator output.

The CMPMON register can be ~~set~~ read by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 14-5. Format of Comparator Output Monitor Register (CMPMON)

CMPMON0	Comparator output monitor value	R/W
0	When CINV = 0 (comparator output is not inverted) • Comparator input voltage (IVCMP0n) < reference voltage • Comparator operation disabled (HCMPON = 0) • Comparator output is disabled (COE = 0) When CINV = 1 (converter output is inverted) • Comparator input voltage (IVCMP0n) > reference voltage	~~R/W~~ R
1	When CINV = 0 (comparator output is not inverted) • Comparator input voltage (IVCMP0n) > reference voltage When CINV = 1 (comparator output is inverted) • Comparator input voltage (IVCMP0n) < reference voltage • Comparator operation disabled (HCMPON = 0) • Comparator output is disabled (COE = 0)	

No.64: Correct typos in chapter “14.2.7”

14.2.7 Port mode register 4 (PM4)

This register is used to set input/output of port 4 in 1-bit units.

When using the port (P41/VCOUT0) to be shared with the comparator output pin, set the corresponding bit in the port mode register 4 (PM4) and ~~port mode register 4~~ port register 4 (P4) to 0.

The PM4 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to ~~00H~~ FFH.

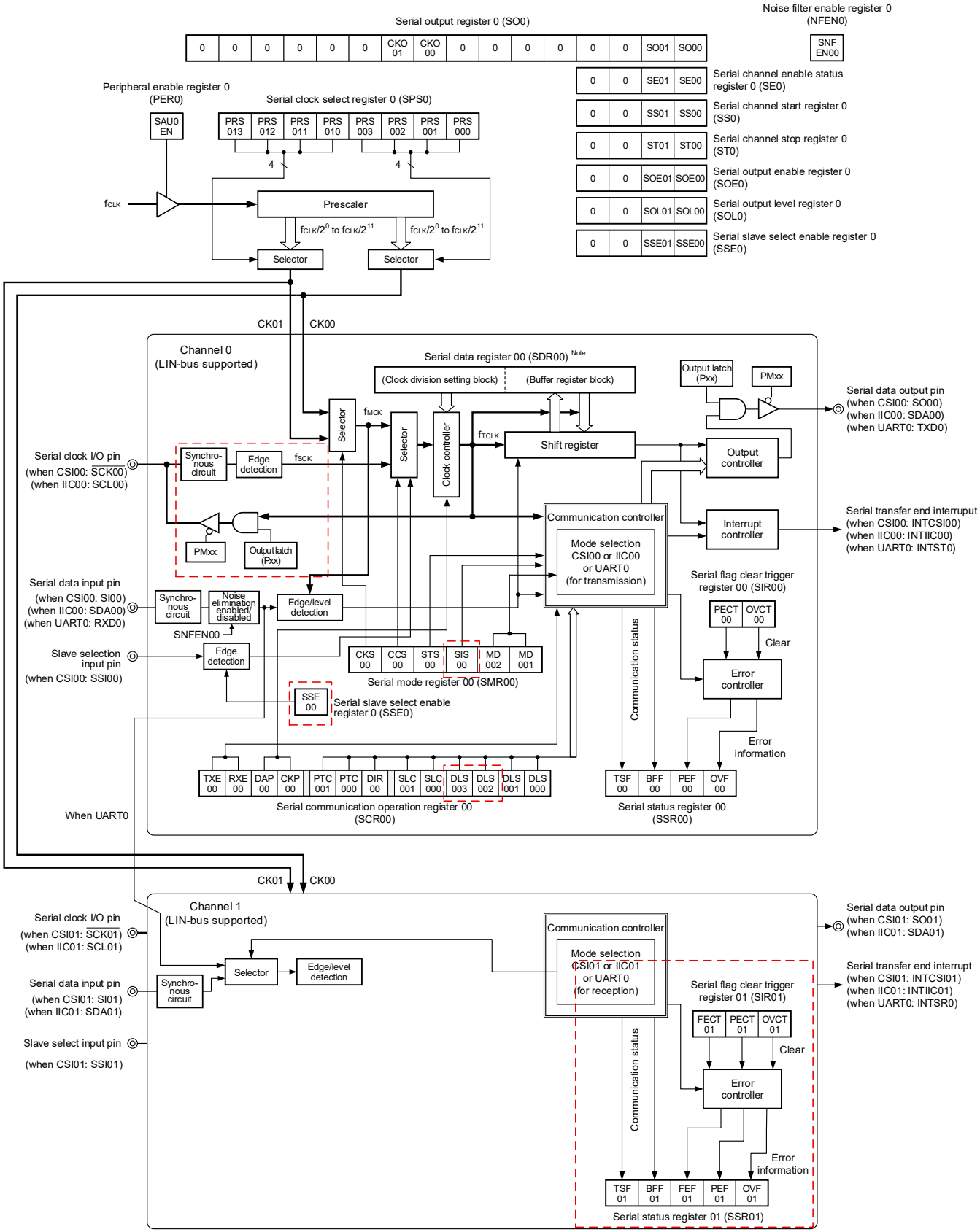
No.65: Correct typo of reference Figure in chapter “14.3.5”

14.3.5 Stopping or Supplying Comparator Clock

When the clock is stopped by setting PER1, all the internal registers in the comparator are initialized. To use the comparator again, follow the procedure in ~~Table 14-13~~ Figure 14-13 to set the registers.

No.66: Correct the information in Figure 15-1

Figure 15-1. Block Diagram of Serial Array Unit 0

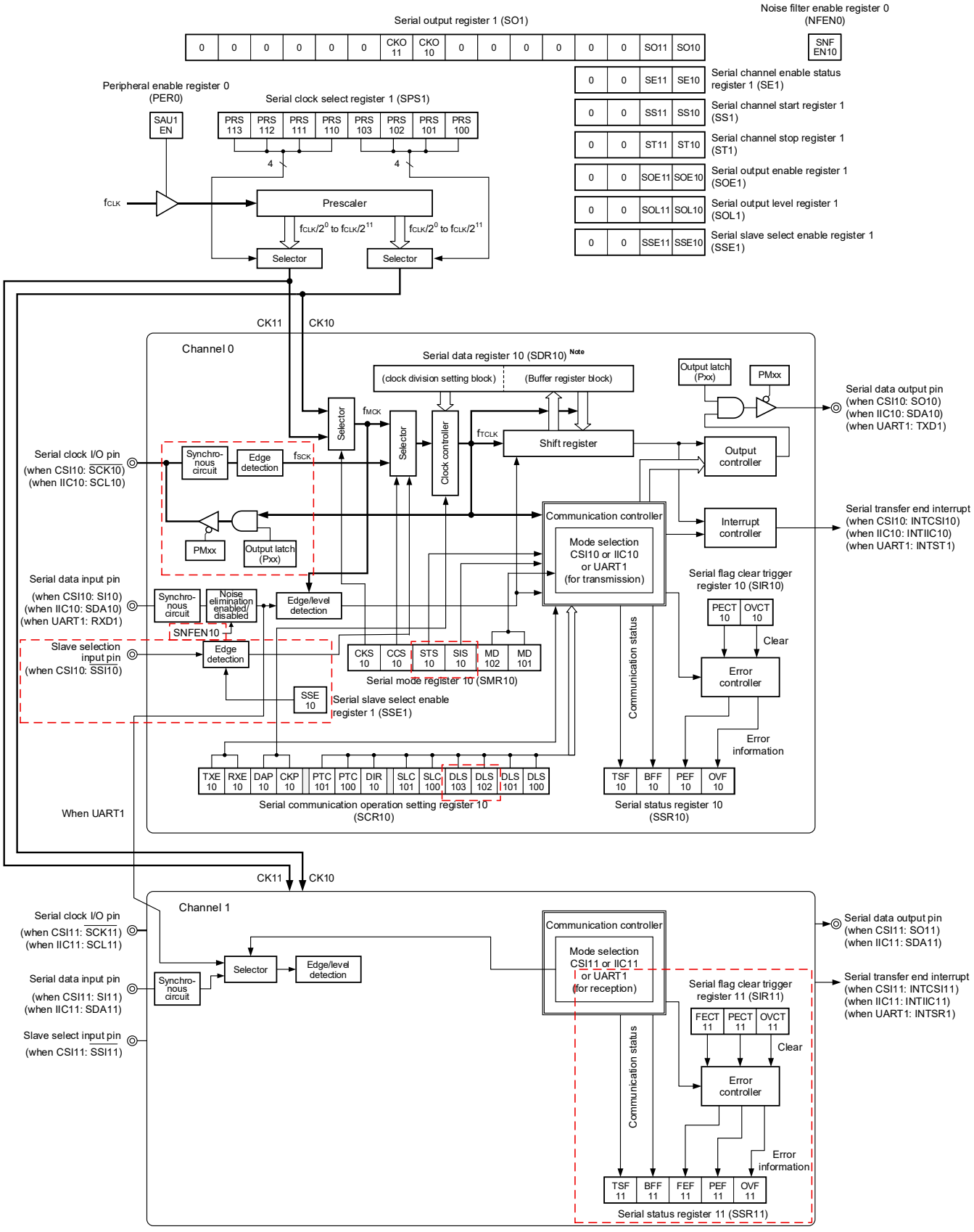


~~**Caution**~~ **Note:** If operation is stopped (SEmn = 0), the upper 7 bits set the clock division, and the lower bits have no meaning.

If operation is in progress (SEmn = 1), the ~~serial data register 10~~ serial data register mn functions as the buffer register.

No.67: Correct the information in Figure 15-2

Figure 15-2. Block Diagram of Serial Array Unit 1

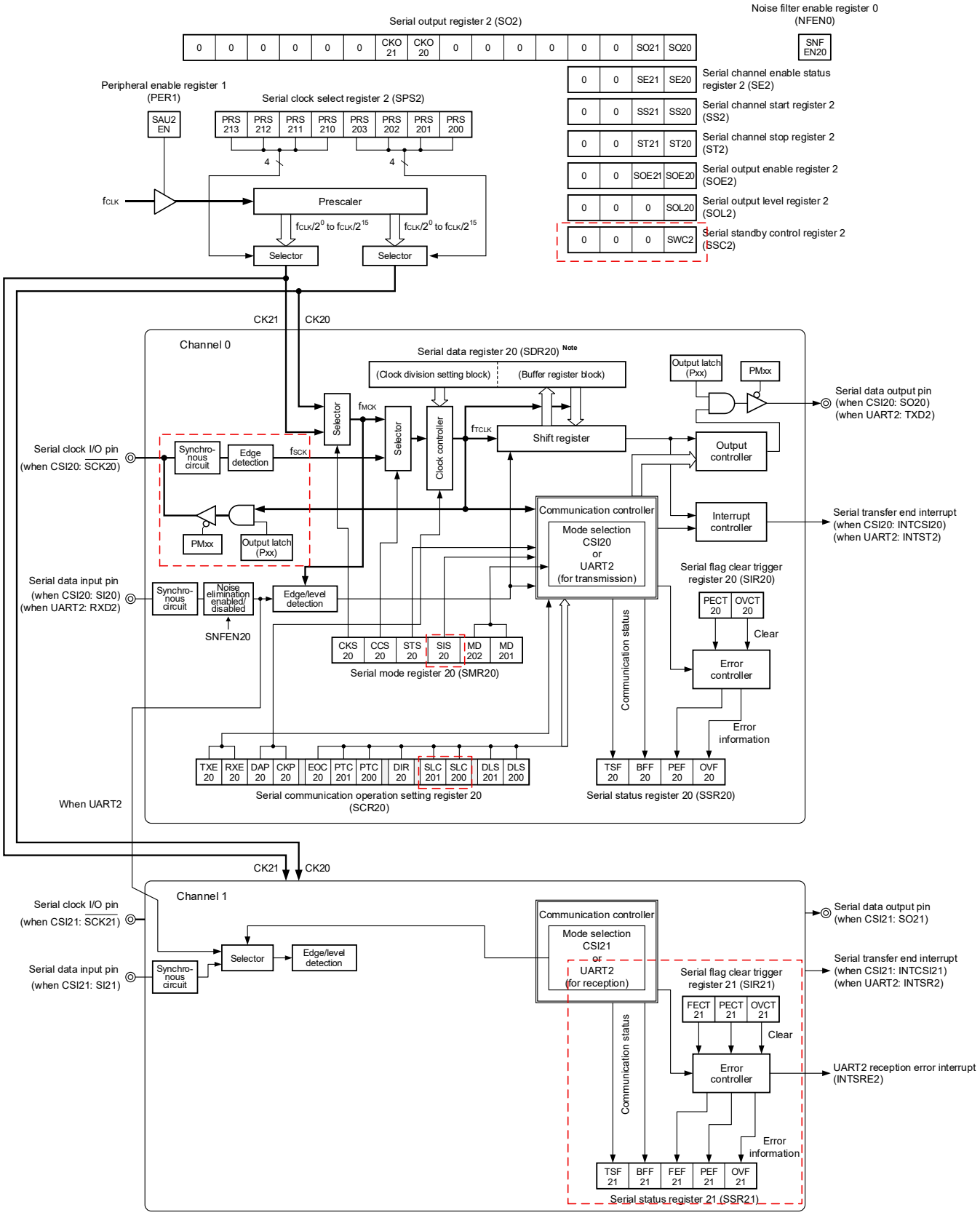


~~**Caution**~~ **Note:** If operation is stopped (SEmn = 0), the upper 7 bits set the clock division, and the lower bits have no meaning.

If operation is in progress (SEmn = 1), the ~~serial data register 10~~ serial data register mn functions as the buffer register.

No.68: Correct the information in Figure 15-3

Figure 15-3. Block Diagram of Serial Array Unit 2 (144 and 100-pin only)



~~**Caution**~~ **Note:** If operation is stopped (SEmn = 0), the upper 7 bits set the clock division, and the lower bits have no meaning.

If operation is in progress (SEmn = 1), the ~~serial data register 10~~ serial data register mn functions as the buffer register.

No.69: Correct the description of Note 1 at the bottom of Figure 15-10

Figure 15-10. Format of Serial Communication Operation Setting Register mn (SCRmn)

Address: F010CH, F010DH (SCR00), F010EH, F010FH (SCR01), After reset: 0087H R/W
F014CH, F014DH (SCR10), F014EH, F014FH (SCR11),
F0158H, F0159H (SCR20), F015AH, F015BH (SCR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn Note 1	PTC mn1	PTC mn0	DIR mn	0	SLC mn1	SLC mn0	DLS mn3 Note 2	DLS mn2 Note 2	DLS mn1	DLS mn0

Notes 1. ~~m = 2~~ SCR21 register only.
2. m = 0, 1 only.

No.70: Correct the description of Note at the bottom of Figure 15-12

Figure 15-12. Format of Serial Flag Clear Trigger Register mn (SIRmn)

Address: F0104H, F0105H (SIR00), F0106H, F0107H (SIR01), After reset: 0000H R/W
F0144H, F0145H (SIR10), F0146H, F0147H (SIR11),
F0148H, F0149H (SIR20), F014AH, F014BH (SIR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRmn	0	0	0	0	0	0	0	0	0	0	0	0	0	FECT mn Note	PECT mn	OVCT mn

Note ~~Unit 2 incorporates only SIR21~~ SIR01, SIR11 and SIR21 only.

No.71: Correct the description of Note at the bottom of Figure 15-13

Figure 15-13. Format of Serial Status Register mn (SSRmn)

Address: F0100H, F0101H (SSR00), F0102H, F0103H (SSR01), After reset: 0000H R
F0140H, F0141H (SSR10), F0142H, F0143H (SSR11),
F0140H, F0141H (SSR20), F0142H, F0143H (SSR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSRmn	0	0	0	0	0	0	0	0	0	TSF mn	BFF mn	0	0	FEF mn Note	PEF mn	OVF mn

Note ~~Unit 2 incorporates only SSR21~~ SSR01, SSR11 and SSR21 only.

No.72: Correct typo of SEm register in chapter “15.3.11”

15.3.11 Serial channel enable status register m (SEm)

Read the SEm register by a 16-bit memory manipulation instruction.
Read the lower 8 bits of the SEm register with a 1-bit or 8-bit memory manipulation instruction with ~~SFmL~~ SEmL.
Reset signal generation clears the SEm register to 0000H.

No.73: Correct typo of Caution at the bottom of Figure 15-18

Figure 15-18. Format of Serial Output Register m (SOm)

Address: F0118H, F0119H (SO0), F0158H, F0159H (SO1), After reset: 0303H R/W
F0168H, F0169H (SO2)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm	0	0	0	0	0	0	CKO m1	CKO m0	0	0	0	0	0	0	SO m1	SO m0

Caution Be sure to clear bits ~~15 to 12~~ 15 to 10 and 7 to 2 of the SOm register to 0.

No.74: Correct typo of Figure Title of Figure 15-27

Figure 15-27. Format of Port Mode Registers 0 to 7, 12, 15 (PM0 to ~~PIM7, PIM12, PIM15~~)

Figure 15-27. Format of Port Mode Registers 0 to 7, 12, 15 (PM0 to PM7, PM12, PM15)

No.75: Correct typos of Remark at the bottom of Figures 15-30, 15-74 and 15-77

There is an error in the Remark at the bottom of the figure. (See Figure 15-30 for an example.)

Figure 15-30. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) (1/2)

Remarks 1. m: Unit number (m = ~~0, 1~~ 0 to 2), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01, 10, 11, 20, 21), mn = 00, 01, 10, 11, 20, 21

No.76: Correct typos of list for slave reception in chapter “15.6.5”

15.6.5 Slave reception

Slave reception is an operation wherein this MCU receives data from another device in the state of a transfer clock being input from another device.

SPI Function	CSI00	CSI01	CSI10	CSI11
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	~~Channel 2 of SAU0~~ Channel 0 of SAU1	~~Channel 3 of SAU0~~ Channel 1 of SAU1
Pins used	~~SCK00, SI00, SII00~~ SCK00, SI00, SSI00	~~SCK01, SI01, SII01~~ SCK01, SI01, SSI01	~~SCK10, SI10, SII10~~ SCK10, SI10, SSI10	~~SCK11, SI11, SII11~~ SCK11, SI11, SSI11
:	:	:	:	:

No.77: Correct typo of SSEm register symbol in Figure 15-142

Figure 15-142. Example of Contents of Registers for Slave Reception of SPI Function (CSI00, CSI01, CSI10, CSI11) (2/2)

(g) Serial slave select enable register m (SSEm) … Controls the SSI00, SSI01, SSI10, and SSI11 pin inputs of the target channel in slave mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
~~SSm~~ SSEm	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SSEm1 0/1	SSEm0 0/1

No.78: Correct the information of SCRmn.DLSmn[1:0] bit in Figure 15-157

Figure 15-157. Example of Contents of Registers for UART Transmission of UART (UART0, UART1, UART2) (1/2)

(b) Serial communication operation setting register mn (SCRmn)

(1) UART0, UART1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn	0	0	PTCmn1	PTCmn0	DIRmn	0	SLCmn1	SLCmn0	DLSmn3	DLSmn2	DLSmn1	DLSmn0
	1	0	0	0			0/1	0/1	0/1		0/1	0/1	0/1	0/1	0/1	0/1

Setting of data length
0110B: 7 bits
0111B: 8 bits
1000B: 9 bits
1111B: ~~10 bits~~ 16 bits

(2) UART2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn	0	EOCmn	PTCmn1	PTCmn0	DIRmn	0	SLCmn1	SLCmn0	0	1	DLSmn1	DLSmn0
	1	0	0	0		0	0/1	0/1	0/1		0/1	0/1			0/1	0/1

Setting of data length
10B: 7 bits
11B: 8 bits
01B: 9 bits

No.79: Correct the information of SCRmn.DLSmn[1:0] bit in Figure 15-171

Figure 15-171. Example of Contents of Registers for UART Reception of UART (UART0, UART1, UART2) (1/2)

(c) Serial communication operation setting register mn (SCRmn)

(1) UART0, UART1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn	0	0	PTCmn1	PTCmn0	DIRmn	0	SLCmn1	SLCmn0	DLSmn3	DLSmn2	DLSmn1	DLSmn0
	0	1	0	0			0/1	0/1	0/1		0	1	0/1	0/1	0/1	0/1

Setting of data length
0110B: 7 bits
0111B: 8 bits
1000B: 9 bits
1111B: ~~10 bits~~ 16 bits

(2) UART2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn	0	EOCmn	PTCmn1	PTCmn0	DIRmn	0	0	0	0	1	DLSmn1	DLSmn0
	0	1	0	0		0/1	0/1	0/1	0/1						0/1	0/1

Setting of data length
~~0110B~~ 10B: 7 bits
~~0111B~~ 11B: 8 bits
~~1000B~~ 01B: 9 bits
~~1111B: 10 bits~~

No.80: Correct description in chapter “15.9.5”

15.9.5 Calculating transfer rate

The transfer rate for simplified I²C (IIC00, IIC01, IIC10, IIC11, ~~IIC20, IIC21, IIC30, IIC31~~) communication can be calculated by the following expressions.

No.81: Correct description and add Remark in chapter “16.3.7”

16.3.7 IICA high-level width setting register 0 (IICWH0)

This register is used to set the high-level width of the SCLA0 pin signal that is output by serial interface IICA.

The IICWH0 register can be set by an 8-bit memory manipulation instruction.

Set the IICWH0 register while operation of I2C is disabled (bit 7 (IICE0) of IICA control register 00 (IICCTL00) is 0).

Reset signal generation sets this register to FFH.

For details about setting the IICWH0 register, see **16.4.2 Setting Transfer Clock by Using IICWL0 and IICWH0 registers**.

Remark ~~**For how to set the transfer clock by using the IICWL0 and IICWH0 registers, see 16.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers.**~~ The minimum serial clock cycle is (IICWL0 + 1) + (IICWH0 + 1).

No.82: Add the description of Note 3 in chapter “16.4.2”

16.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers

Caution 3. The minimum serial clock cycle is (IICWL0 + 1) + (IICWH0 + 1). Determine the values to be set in the IICWL0 and IICWH0 registers by considering the rise time (t_R) and fall time (t_F) of the SDAA0 and SCLA0 signals.

No.83: Correct typo at the bottom of Figure 16-33

Figure 16-33. Example of Slave to Master Communication
(When 8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)

The meanings of <8> to <19> in (3) Data ~ data ~ stop condition in Figure 16-33 are explained below.

<8> The master device sets a wait status (SCLA0 = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICA0: end of transfer). Because of ~~ACKE0 = 0~~ ACKE0 = 1 in the master device, the master device then sends an ACK by hardware to the slave device.

No.84: Correct description of LDBmn register in chapter “17.2.1 (24)”

(24) LIN/UART Data Buffer m Register (LDBnm) (m = 1 to 8)

For response reception:

These registers hold the data received in the response field.

The received data is overwritten. If an error is detected, ~~the data prior to reception interruption is stored in the register~~ the data up to the byte in which the error was detected are stored in the register.

Do not read these registers when the FTS bit is 1 (frame transmission or wake-up transmission/reception is started).

No.85: Correct description of HTRC flag in chapter “17.2.2 (18)”

(18) LIN/UART Status Register (LSTn)

HTRC flag (~~successful header transmission flag~~ successful header reception flag)

Only 0 can be written to the HTRC flag; when 1 is written, the bit retains the value that has been retained before 1 is written.

The HTRC flag is set to 1 upon completion of ~~header transmission~~ header reception. Here, an interrupt is generated if the SHIE bit in the LIEn register is 1 (interrupt is enabled). Note that when header reception is completed with the HTRC flag set to 1, an interrupt is not generated. To clear the bit to 0, write 0 to the bit.

After the reception of a header, clear this bit after reading it as 1 so that a new header will be detectable.

No.86: Correct description of LDBmn register in chapter “17.2.2 (23)”

(23) LIN/UART Data Buffer m Register (LDBnm) (m = 1 to 8)

For response reception:

These registers hold the data received in the response field.

The received data is overwritten. If an error is detected, ~~the data prior to reception interruption is stored in the register~~ the data up to the byte in which the error was detected are stored in the register.

Do not read these registers when the RTS bit is 1 (response transmission/reception is started).

No.87: Correct description of LUTDRn register in chapter “17.2.3 (24)”

(24) UART Transmission Data Register (LUTDRn)

The LUTDRn register sets the data to be transmitted from the ~~transmission data register~~ UART transmission data register.

Writing data to this register with the UTOE bit in the LUOERn register set to 1 starts transmission.

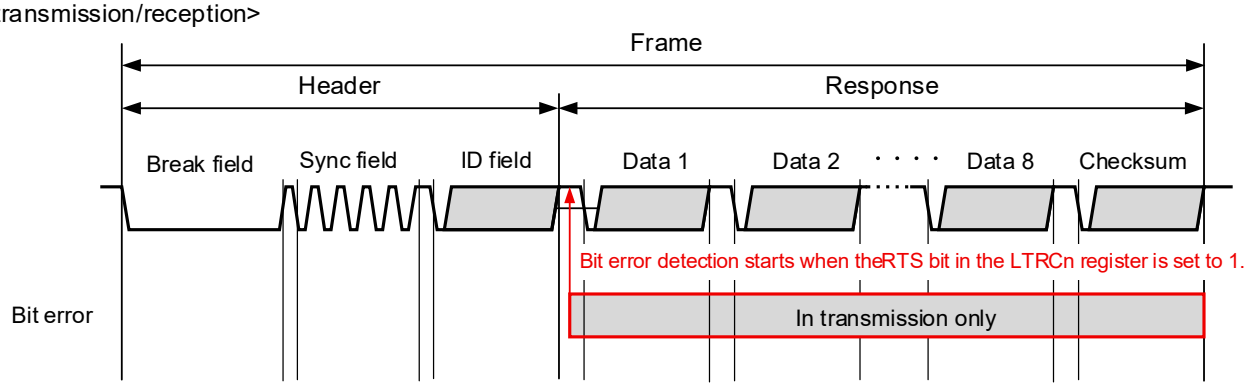
This register can be accessed in 8 bits.

No.88: Correct the information of bit error detection in Figure 17-21

Added explanation of bit error detection timing (revisions are indicated in red text and underlined in red).

Figure 17-21. Target Time Area for LIN Error Detection (LIN Slave Mode)

<Frame transmission/reception>



No.89: Add Caution 5 to chapter “17.5.1 (5)”

(5) SNOOZE Mode Function

Caution 5. The CPU enters from the STOP mode to the SNOOZE mode at the falling edge of the LRXDn signal. Note that the UART frame reception in the LIN/UART module (UART mode) may not start and the CPU may keep the SNOOZE mode in case an input pulse on the LRXDn pin is too short to be detected as a start bit. In such cases, data in the next UART frame does not be received correctly, and a reception error occurs.

No.90: Correct the information in Tables 17-21 to 17-24

Changed the description to take into account the grade K products (oscillation accuracy (±3%) of the high-speed on-chip oscillator).

Table 17-21. Baud Rate Setting for UART Reception in SNOOZE Mode (LIN communication clock source = 32 MHz, FRQSEL4 = 0)

UART Baud Rate (target)	Device Grade	LIN Communication Clock Source	Prescaler LPRS[2:0]	Baud Rate Generators 0 and 1 LBRP0 and LBRP1
1200 bps	Grade L	32 MHz ± 2%	001B (1/2)	828
2400 bps	Grade L			412
4800 bps	Grade L			203

Table 17-22. Baud Rate Setting for UART Reception in SNOOZE Mode (LIN communication clock source = 24 MHz, FRQSEL4 = 0)

UART Baud Rate (target)	Device Grade	LIN Communication Clock Source	Prescaler LPRS[2:0]	Baud Rate Generators 0 and 1 LBRP0 and LBRP1
1200 bps	Grade L	24 MHz ± 2%	001B (1/2)	621
	Grade K	24 MHz ± 3%		621
2400 bps	Grade L	24 MHz ± 2%	001B (1/2)	308
	Grade K	24 MHz ± 3%		308
4800 bps	Grade L	24 MHz ± 2%	001B (1/2)	152
	Grade K	24 MHz ± 3%		152

Table 17-23. Baud Rate Setting for UART Reception in SNOOZE Mode (LIN communication clock source = 32 MHz, FRQSEL4 =1)

UART Baud Rate (target)	Device Grade	LIN Communication Clock Source	Prescaler LPRS[2:0]	Baud Rate Generators 0 and 1 LBRP0 and LBRP1
1200 bps	Grade L	32 MHz ± 2%	001B (1/2)	826
2400 bps	Grade L			410

Table 17-24. Baud Rate Setting for UART Reception in SNOOZE Mode (LIN communication clock source = 24 MHz, FRQSEL4 =1)

UART Baud Rate (target)	Device Grade	LIN Communication Clock Source	Prescaler LPRS[2:0]	Baud Rate Generators 0 and 1 LBRP0 and LBRP1
1200 bps	Grade L	24 MHz ± 2%	001B (1/2)	619
	Grade K	24 MHz ± 3%		619
2400 bps	Grade L	24 MHz ± 2%	001B (1/2)	307
	Grade K	24 MHz ± 3%		307

No.91: Correct the information of the LWBRn register in chapter “17.6”

17.6 LIN Self-Test Mode

In the LIN self-test mode, the LIN/UART module operates at the highest baud rate regardless of the setting of the baud rate generator. The baud rate is <frequency of the LIN communications clock source>/16 bps regardless of the settings of the baud rate related registers (the NSPB bit in the LWBRn register must be set to 0000b or 1111b, and the LPRS bit of the LWBRn register must be set to 000b).

17.6.2 Transmission in LIN Master Self-Test Mode

To execute a self-test on LIN master transmission, perform the procedure below:

• Set registers related to the baud rate, noise filter, and interrupt output.
LWBRn register = ~~0000xxxxb~~ 0000000xb Note 1

Notes 1. The following register settings do not affect the operations in LIN self-test mode. Therefore, setting them is not mandatory.
~~LPRS bits in LWBRn register~~, LBRPn0 register, LBRPn1 register, and LCKS bits in LMDn register

17.6.3 Reception in LIN Master Self-Test Mode

To execute a self-test on LIN master reception, perform the procedure below:

• Set registers related to the baud rate, noise filter, and interrupt output.
LWBRn register = ~~0000xxxxb~~ 0000000xb Note 1

Notes 1. The following register settings do not affect the operations in LIN self-test mode. Therefore, setting them is not mandatory.
~~LPRS bits in LWBRn register,~~ LBRPn0 register, LBRPn1 register, LCKS bits in LMDn register, and IBS bits in LSCn register

17.6.4 Transmission in LIN Slave Self-Test Mode

To execute a self-test on LIN slave transmission, perform the procedure below:

• Set registers related to the baud rate, noise filter, and interrupt output.
LWBRn register = ~~0000xxx0b~~ 00000000b Note 1

Notes 1. The following register settings do not affect the operations in LIN self-test mode. Therefore, setting them is not mandatory.
~~LPRS bits in LWBRn register,~~ LBRPn0 register, and LBRPn1 register

17.6.5 Reception in LIN Slave Self-Test Mode

To execute a self-test on LIN slave reception, perform the procedure below:

• Set registers related to the baud rate, noise filter, and interrupt output.
LWBRn register = ~~0000xxx0b~~ 00000000b Note 1

Notes 1. The following register settings do not affect the operations in LIN self-test mode. Therefore, setting them is not mandatory.
~~LPRS bits in LWBRn register,~~ LBRPn0 register, LBRPn1 register, and IBS bits in LSCn register

No.92: Add the Note of CFSTSk register in chapter “18.3.47”

18.3.47 CANi Transmit/Receive FIFO Status Register k (CFSTSk) (i = 0, 1, k = 0, 1)

Address CFSTS0: F0358H, CFSTS1: F035AH

The CFSTSk register can be accessed in 16-bit units. In addition, the CFSTSk register can be accessed in 8-bit units as CFSTSkL, CFSTSkH register.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	–	–	CFMC[5:0]						–	–	–	CF TXIF	CF RXIF	CF MLT	CF FLL	CF EMP
After Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
:	:	:	:	:
4	CFTXIF	Transmit/Receive FIFO Transmit Interrupt Request Flag	0: No transmit/receive FIFO transmit interrupt request is present. 1: A transmit/receive FIFO transmit interrupt request is present.	R(/W)Note
3	CFRXIF	Transmit/Receive FIFO Receive Interrupt Request Flag	0: No transmit/receive FIFO receive interrupt request is present. 1: A transmit/receive FIFO receive interrupt request is present.	R(/W)Note
2	CFMLT	Transmit/Receive FIFO Message Lost Flag	0: No transmit/receive FIFO message is lost. 1: A transmit/receive FIFO message is lost.	R(/W)Note
:	:	:	:	:

Note The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state. To write 0 to this flag bit, write by using an 8-bit data transfer instruction or a 16-bit data transfer instruction.

In case this bit is set to 1 by the CAN module and cleared to 0 by the CPU instruction at the same time, the setting by the CAN module is prioritized. For the details, refer to chapter "**18.15 Notes on the CAN Module**".

No.93: Add the Note of THLSTSk register in chapter “18.3.75”

18.3.75 CANi Transmit History Buffer Status Register (THLSTSi) (i = 0, 1)

Address THLSTS0: F0380H, THLSTS1: F0382H

The THLSTSi register can be accessed in 16-bit units. In addition, the THLSTSi register can be accessed in 8-bit units as THLSTSiL, THLSTSiH register.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	–	–	–	–	THLMC[3:0]				–	–	–	–	THL IF	THL ELT	THL FLL	THL EMP
After Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
:	:	:	:	:
3	THLIF	Transmit History Interrupt Request Flag	0: No transmit history interrupt request is present. 1: A transmit history interrupt request is present.	R(/W)Note
2	THLELT	Transmit History Buffer Overflow Flag	0: Transmit history buffer overflow has not occurred. 1: Transmit history buffer overflow has occurred.	R(/W)Note
:	:	:	:	:

Note The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state. To write 0 to this flag bit, write by using an 8-bit data transfer instruction or a 16-bit data transfer instruction.

In case this bit is set to 1 by the CAN module and cleared to 0 by the CPU instruction at the same time, the setting by the CAN module is prioritized. For the details, refer to chapter "**18.15 Notes on the CAN Module**".

No.94: Correct typo of the TMCp register symbol in chapter “18.15”

18.15 Notes on the CAN Module

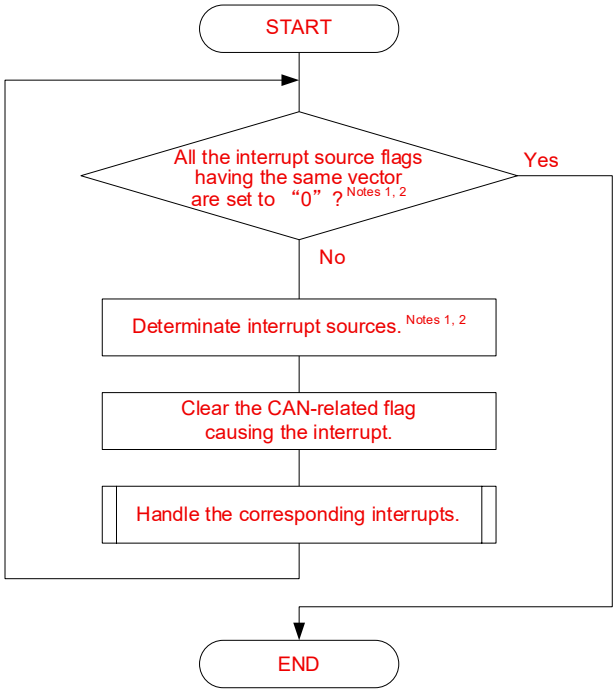
- When linking transmit buffers to transmit/receive FIFO buffers, set the control register (~~TCMp~~ TMCp) of the corresponding transmit buffer to H'00. The status register (TMSTSp) of the corresponding transmit buffer should not be used. Flags in other status registers (registers TMTRSTS, TMTCSTS, and TMTASTS), which correspond to transmit buffers linked to transmit/receive FIFO buffers remain unchanged. Set the enable bit in the corresponding interrupt enable register (the TMIEC register) to 0 (transmit buffer interrupt is disabled).

No.95: Add the description of CAN interrupt in chapter “18.15”

18.15 Notes on the CAN Module

- Since an interrupt request flag in the CAN module is not automatically cleared to 0 when an interrupt is accepted, the flags must be cleared to 0 by software. After the corresponding interrupt request flag has been set to 1, an interrupt is not generated even if an interrupt source condition is satisfied.
  When using interrupts, make sure that all request flags in the CAN module corresponding to interrupt factors are “0” responsible. See the **Figure 18-38** below.

Figure 18-38. Notes on the CAN Module Interrupt



Notes 1. Before finishing the interrupt handling, make sure that interrupt request flags of the CAN module corresponding to the interrupt source have all been cleared (set to 0).

eg) If only the receiving FIFO buffer 0 is enabled (the RFIE flag of the RFCC0 register is 1) and the receive FIFO interrupt is used, set the RFIF flag of the RFSTS0 register to 0 within the interrupt handling. After that, confirm that the RFIF flag of the RFSTS0 register has reached “0” and end the interrupt handling.

2. The CANi wakeup interrupt request flag does not exist in CAN module, because the interrupt function controls CANi wakeup interrupt.

No.96: Correct typo of bits DTCEN20 in Table 20-6

Table 20-6. Correspondences between Interrupt Sources and Bits DTCENi0 to DTCENi7

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
:	:	:	:	:	:	:	:	:
DTCEN2	CAN0 reception end	CAN1 reception end	End of channel 0 of timer array unit 0 count or capture	End of channel 1 of timer array unit 0 count or capture	End of channel 2 of timer array unit 0 count or capture	End of channel 3 of timer array unit 0 count or capture	End of channel 4 of timer array unit 0 count or capture	End of channel 5 of ~~timer array unit 1~~ timer array unit 0 count or capture
:	:	:	:	:	:	:	:	:

No.97: Correct the information of the SELHS0 register in Figure 20-13

Figure 20-13. Format of High-speed DTC Channel Select Register 0 (SELHS0)

Symbol	7	6	5	4	3	2	1	0
SELHS0	0	0	SELHS05	SELHS04	SELHS03	SELHS02	SELHS01	SELHS00

SELHS05 to SELHS00						Description
0	0	0	0	0	0	Activation source number 0 is selected as high-speed channel 0.
0	0	0	0	0	1	Activation source number 1 is selected as high-speed channel 0.
0	0	0	0	1	~~1~~ 0	Activation source number 2 is selected as high-speed channel 0.
:						:
1	1	0	0	1	0	Activation source number 50 is selected as high-speed channel 0.
1	1	0	0	1	1	Activation source number 51 is selected as high-speed channel 0. Note
1	1	0	1	0	0	Activation source number 52 is selected as high-speed channel 0. Note
1	1	1	1	1	1	High-speed channel 0 is not used.
Other than above						Setting prohibited

Note 144-pin products only.

No.98: Correct the information of the SELHS1 register in Figure 20-14

Figure 20-14. Format of High-speed DTC Channel Select Register 1 (SELHS1)

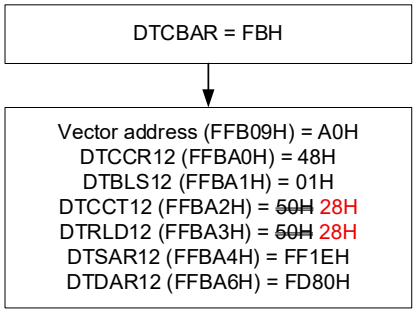
Symbol	7	6	5	4	3	2	1	0
SELHS1	0	0	SELHS15	SELHS14	SELHS13	SELHS12	SELHS11	SELHS10

SELHS15 to SELHS10						Description
0	0	0	0	0	0	Activation source number 0 is selected as high-speed channel 1.
0	0	0	0	0	1	Activation source number 1 is selected as high-speed channel 1.
0	0	0	0	1	~~1~~ 0	Activation source number 2 is selected as high-speed channel 1.
:						:
1	1	0	0	1	0	Activation source number 50 is selected as high-speed channel 1.
1	1	0	0	1	1	Activation source number 51 is selected as high-speed channel 1. Note
1	1	0	1	0	0	Activation source number 52 is selected as high-speed channel 1. Note
1	1	1	1	1	1	High-speed channel 1 is not used.
Other than above						Setting prohibited

Note 144-pin products only.

No.99: Correct typos of value of registers DTCCT12 and DTRLD12 in Figure 20-22

Figure 20-22. Example 1 of Using Normal Mode: Consecutively Capturing A/D Conversion Results



No.100: Add the description of chain transfer operation in chapter “20.3.4”

20.3.4 Chain Transfers

When the CHNE bit in the DTCCRj (j = 0 to 22) register is 1 (chain transfers enabled), multiple data transfers can be continuously performed by one activation source.

When the DTC is activated, one control data is selected according to the data read from the DTC vector address corresponding to the activation source, and the selected control data is read from the DTC control data area. When the CHNE bit for the control data is 1 (chain transfers enabled), the next control data immediately following the current control data is read and transferred after the current transfer is completed. This operation is repeated until the data transfer with the control data for which the CHNE bit is 0 (chain transfers disabled) is completed.

In chain transfers with the use of multiple control data sets, if the normal mode is selected by the second or subsequent control data, the number of transfers set in the first of the control data is valid and settings for the number of transfers in the second or subsequent control data are invalid.

On the other hand, if the repeat mode is selected by the second or subsequent control data, the second or subsequent control data are written back, so the number of transfers needs to be set for each of the control data.

Figure 20-26 shows data transfers in chain transfers.

No.101: Correct typo of Remak at the bottom of Table 21-3

Table 21-3. Correspondence Between Values Set to ELSELRn (n = 00 to 25) Registers and Operation of Link Destination Peripheral Functions at Reception

Bits ELSELRn3 to ELSELRn0 in ELSELRn Register	Link Destination Peripheral Function	Operation When Receiving Event
:	:	:
0010B	Timer input of timer array unit 0 channel 0 Notes 1 and 2	Delay counter, input pulse interval measurement, external event counter
0011B	Timer input of timer array unit 0 channel 0 Notes 1 and 2	
:	:	:
1000B	Timer input of timer array unit 0 channel 2 Notes 1 and 2	Delay counter, input pulse interval measurement, external event counter
1001B	Timer input of timer array unit 0 channel 3 Notes 1 and 2	

Notes 1. To select the timer input of timer array unit 0 channel m as the link destination peripheral function, first set the operating clock for channel m to fCLK using timer clock select register 0 (TPS0), and then set the timer output used for channel m to an event input signal from the ELC using timer input select register 0 (TIS0).

2. Before selecting the timer input of timer array unit 0 channel m as the link destination peripheral function, set the noise filter of the corresponding link destination channel in the timer array unit 0 to OFF (set the TNFEN0m bit to 0) by using the noise filter enable register 1 (NFEN1).

Remark m = ~~0, 3~~ 0 to 3

No.102: Correct typos of interrupt flag in Table 22-2

Table 22-2. Flags Corresponding to Interrupt Request Sources

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	144-pin	100-pin	80-pin	64-pin	48-pin
INTCSI00	~~IICIF00~~ CSIIF00	IF0H	CSIMK00	MK0H	CSIPR000, CSIPR100	PR00H, PR10H	✓	✓	✓	–	–
~~INTRM00~~ INTTM00	TMIF00	IF1L	TMMK00	MK1L	TMPR000, TMPR100	PR01L, PR11K	✓	✓	✓	✓	✓
INTP10	PIF10	IF1H	PMK10	MK1H	~~PPR10, PPR110~~ PPR010, PPR110	PR01H, PR11H	✓	✓	✓	✓	–
INTP11	PIF11	IF2L	PMK11	MK2L	~~PPR11, PPR111~~ PPR011, PPR111	PR02L, PR12L	✓	✓	✓	✓	–
INTCAN0ERR	CAN0ERRIF		~~CAN0ERMK~~ CAN0ERRMK		CAN0ERRPR0, ~~CA0ERRPR1~~ CAN0ERRPR1		✓	✓	✓	✓	✓

No.103: Correct the description of Caution in chapter “23.1”

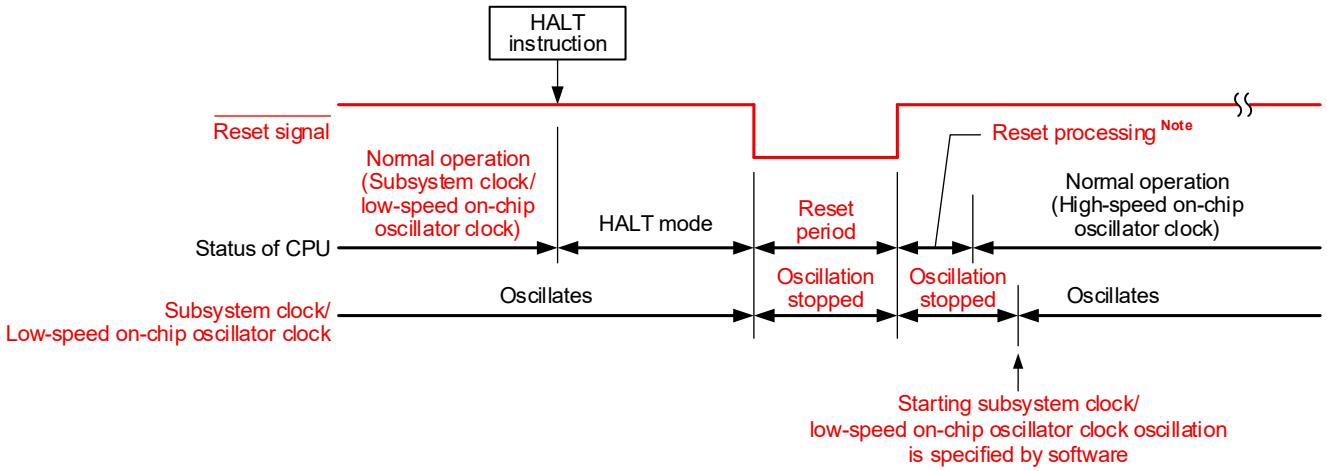
23.1 Functions of Key Interrupt

Caution The pin assignment differs depending on the products. The PIOR50 bit can specify which I/O port is assigned to each KRn function. Inputs to the A/D converter are multiplexed with P70 to P74, P80 to P87 and P90 to P92, to which the function can be assigned. These pins are used as analog input pins in their initial state. Use the PIOR50 bit and the ADPC, PMC7 registers to make the pins operate as digital input pins before using the key interrupt function. For details of the PIOR50 bit and the ADPC, PMC7 registers, refer to 4.3.14 Peripheral I/O redirection register 5 (PIOR5), 12.3.11 A/D port configuration register (ADPC) and 4.3.6 Port mode control register 7, 12 (PMC7, PMC12).

No.104: Correct the information of clock state of sub/low-speed OCO in Figure 24-5

Figure 24-5. HALT Mode Release by Reset

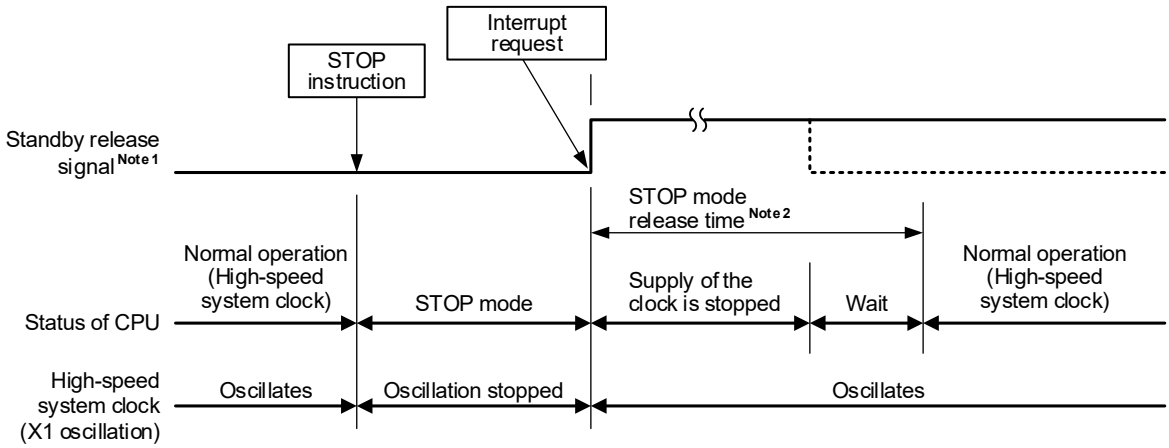
(3) When subsystem clock or low-speed on-chip oscillator clock is used as CPU clock



No.105: Correct typo of OSTS register of Note 2 in Figure 24-6

Figure 24-6. STOP Mode Release by Interrupt Request Generation (1/2)

(1) When high-speed system clock (X1 oscillation) is used as CPU clock



Note 2. STOP mode release time

Supply of the clock is stopped

• When FRQSEL4 = 1 in the user option byte (000C2H/020C2H):

18 μs to "whichever is longer 105 μs and the oscillation stabilization time (set by ~~STS~~ OSTS)"

No.106: Correct typo of option byte address in chapter “24.3.3”

24.3.3 SNOOZE mode

(1) SNOOZE mode setting and operating statuses

In SNOOZE mode transition, wait status to be only following time.

Transition time from STOP mode to SNOOZE mode

- When FRQSEL4 = 1 in the user option byte (~~000C2H/010C2H~~ 000C2H/020C2H): 18 μs to 105 μs
- When FRQSEL4 = 0 in the user option byte (~~000C2H/010C2H~~ 000C2H/020C2H): 18 μs to 65 μs

No.107: Correct the description of Caution and Remark in chapter “26.1”

26.1 Functions of Power-on-reset Circuit

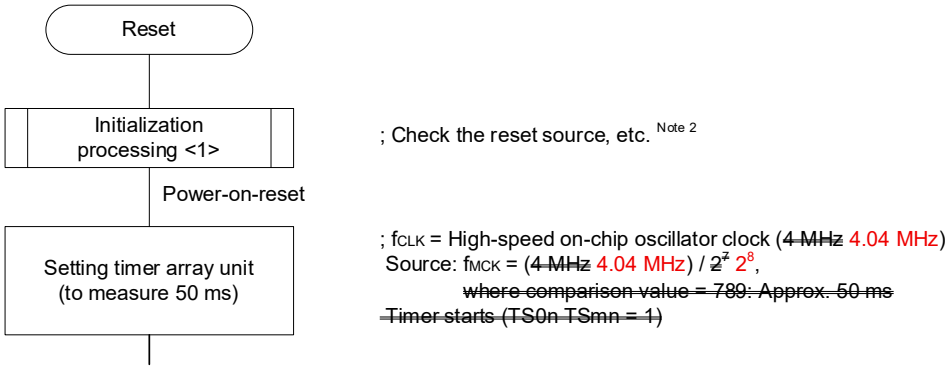
Caution **If an internal reset signal is generated in the POR circuit, the ~~POCRES_0~~ POCRES0 and CLKRF flags of the POR/CLM reset confirmation register (POCRES) and the TRAP, WDCLRF, IAWRF, and LVIRF flags of the reset control flag register (RESF) are cleared (00H).**

Remark This product incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the RESF and POCRES registers for when an internal reset signal is generated by the power-on reset (POR), watchdog timer (WDT), clock monitor, voltage detector (LVD), illegal instruction execution, or illegal-memory access. The RESF register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by the watchdog timer (WDT), voltage detector (LVD), illegal instruction execution, clock monitor, or illegal-memory access. ~~The POCRES register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by the clock monitor.~~ The CLKRF bit of the POCRES register is set to 1 when an internal reset signal is generated by the clock monitor. The POCRES0 bit of the POCRES register is cleared to 0 by the POR reset when it has been set to 1 beforehand.

For details of the POCRES and RESF registers, see **CHAPTER 25 RESET FUNCTION**.

No.108: Correct the information of source clock in Figure 26-3

Figure 26-3. Example of Software Processing After Reset Release (1/2)



No.109: Correct the information of detection level in chapter “27.1”

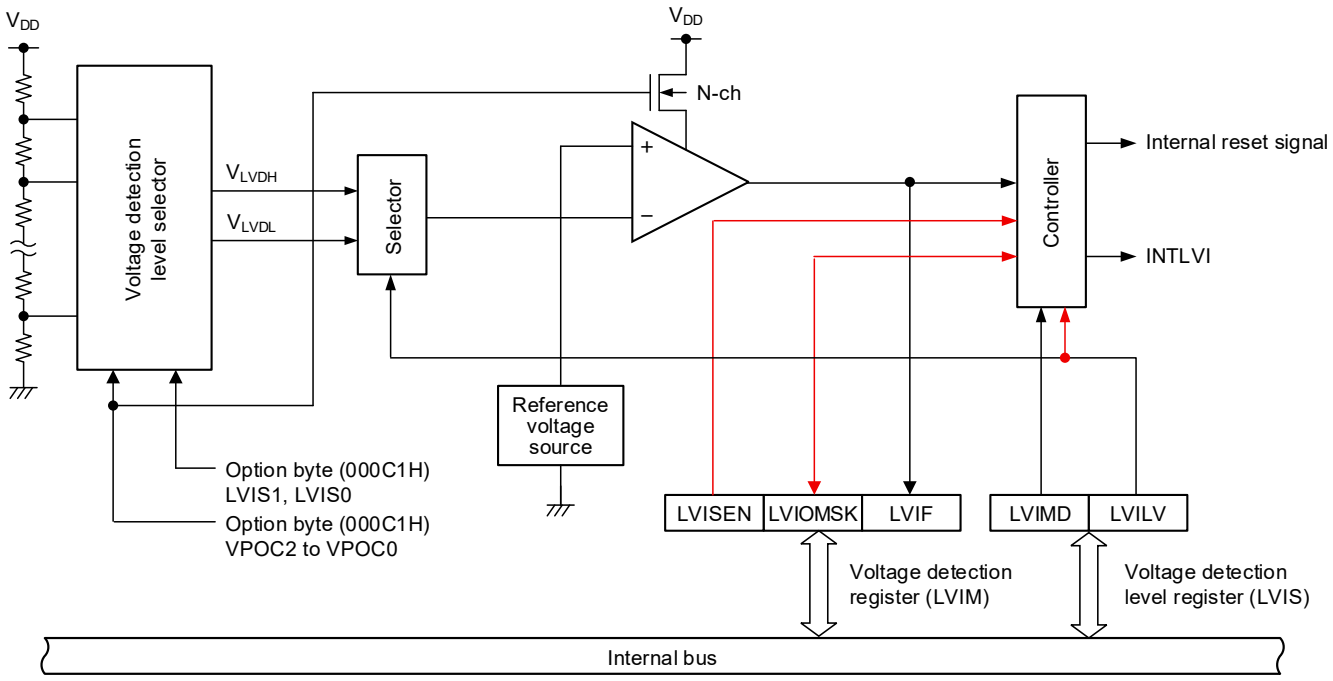
27.1 Functions of Voltage Detector

- The detection level for the power supply detection voltage (V_{LVDH}, V_{LVDL}) can be selected by using the option byte as one of ~~14 levels~~ 6 levels (For details, see **CHAPTER 30 OPTION BYTE**).

No.110: Correct the information of LVD circuit in Figure 27-1

The changes are indicated by red lines.

Figure 27-1. Block Diagram of Voltage Detector



No.111: Correct typo in Table 27-1

Table 27-1. LVD Operation Mode and Detection Voltage Settings for User Option Byte (000C1H/020C1H)

• When used as interrupt & reset mode

Detection voltage			Option byte Setting Value						
VLVDH		VLVDL	LVIMDS1	LVIMDS0	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	Falling edge							
4.42 V	4.32 V	2.75 V	1	0	0	0	1	0	0
4.62 V	4.52 V	2.75 V			0	1	0	0	0
~~3.32 V~~ 3.22 V	3.15 V	2.75 V			0	1	1	0	1
4.74 V	4.64 V							0	0
上記以外			設定禁止						

No.112: Delete the information of IEC61508 in chapters “28.1 and 28.3.2”

IEC61508 is a specification required for the system, so the description will be deleted.

28.1 Overview of Safety Functions

The following safety functions are provided in the RL78/F15 to comply with the ~~IEC60730 and~~ IEC61508 safety standards.

28.3.2 CRC operation function (general-purpose CRC)

~~In order to guarantee safety during operation, the IEC61508 standard mandates the checking of data even while the CPU is operating.~~

In the RL78/F15, a general CRC operation can be executed as a peripheral function while the CPU is operating.

No.113: Correct typo of Figure Title and bit information of ECCDWRVR register in Figure 28-13

Figure 28-13. Format of Write Data Inversion Register (~~ECCWRDR~~ ECCDWRVR)

Address: F0206H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
~~ECCWRVR~~ ECCDWRVR	–	–	–	PRTYRV	ECCRV3	ECCRV2	ECCRV1	ECCRV0

Symbol	7	6	5	4	3	2	1	0
~~ECCWRVR~~ ECCDWRVR	DWRV7	DWRV6	DWRV5	DWRV4	DWRV3	DWRV2	DWRV1	DWRV0

No.114: Add the description of “(3) Cautions for use” in chapter “28.3.5”

28.3.5 Clock monitor

(3) Cautions for use

When entering the STOP mode by stopping the PLL clock during the operation of the clock monitor, set bit 0 (PLLON) in the PLL control register (PLLCTL) before executing the STOP instruction.

Do not use the clock monitor function during on-chip debugging.

No.115: Correct the information of Remark in Figure 30-4

Figure 30-4. Format of On-chip Debug Option Byte (000C3H/020C3H)

Address: 000C3H/020C3H[Note 1]

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	HPIEN[Note 2]	OCDERSD

Remark The value on ~~bits 3 and 2~~ bits 3 to 1 will be written over when the on-chip debug function is in use and thus it will become unstable after the setting. However, be sure to set the default values (0, 1) to bits 3 and 2 at setting.

No.116: Add the description of Caution 4 in chapter “31.8.3”

31.8.3 Procedure for accessing data flash memory

Cautions 3. The high-speed on-chip oscillator should be kept operating during data flash rewrite. If it is kept stopping, the high-speed on-chip oscillator clock should be operated (HIOSTOP = 0). The data flash library should be executed after 30 μs have elapsed.

4. If accessing data flash memory when the f_{SL} (subsystem clock or slow on-chip oscillator) is selected as f_{CLK} (CPU/peripheral hardware clock), take one of the following procedures.:

i) To switch f_{CLK} from f_{SL} to the main system clock, follow these steps (1) to (3).

(1) Confirming the complete switching to main system clock (CLS* = 0).

(2) Read any data flash memory address as a dummy read (don't use the read value).

(3) Waiting until the following time has passed: 5 μs

***: Bit of the system clock control register (CKC)**

ii) Do not read data flash memory when f_{SL} is selected as f_{CLK}.

If data flash content needs to be accessed during f_{SL} is selected as f_{CLK}, store the required data flash content to RAM before setting f_{SL} to f_{CLK}. And read copied content from RAM.

No.117: Correct the information of “RAM Area Used” in Table 32-1

Table 32-1. RAM Area Used and Number of Branches Retained by On-chip Trace

Products	RAM	RAM Area Used	Number of Branches
R5F113PG, R5F113TG	10 KB	− (Do not use the user RAM area)	128
R5F113PH, R5F113TH	16 KB		
R5F113PJ, R5F113TJ	20 KB	~~• 0FB500H-0FB52FH (Hot plug-in/RRM abd DDM by DTC) • 0FB300H-0FB4FFH (On-chip trace)~~ − (Do not use the user RAM area)	
R5F113GK, R5F113LK, R5F113MK, R5F113PK, R5F113TK	26 KB	− (Do not use the user RAM area)	
R5F113GL, R5F113LL, R5F113ML, R5F113PL, R5F113TL	32 KB	• ~~0FB500H-0FB52FH~~ 0F8500H-0F852FH (Hot plug-in/RRM and DMM by DTC) • ~~0FB300H-0FB4FFH~~ 0F8300H-0F84FFH (On-chip trace)	

No.118: Correct typo of reference figure in chapter “32.4.1”

32.4.1 Securement of memory space

The shaded portions in ~~Figure 32-2~~ Figure 32-3 are the areas reserved for placing the debug monitor program, so user programs or data cannot be allocated in these spaces. When using the on-chip debug function, these spaces must be secured so as not to be used by the user program. Moreover, this area must not be rewritten by the user program.

No.119: Correct the information of address in Table 34-1

Figure 32-3. Memory Spaces Where Debug Monitor Programs Are Allocated

Notes 1. Address differs depending on products as follows.

Products (code flash memory capacity)	Address of Note 1
R5F113mG（m = T, P）	1FFFFH
R5F113mH（m = T, P）	2FFFFH
R5F113mJ（m = T, P）	3FFFFH
R5F113mK（m = T, P, M, L, G）	~~47FFFH~~ 5FFFFH
R5F113mL（m = T, P, M, L, G）	7FFFFH

No.120: Correct the information of saddrp in Table 34-1

Table 34-1. Operand Identifiers and Specification Methods

Identifier	Description Method
:	:
saddr saddrp	FFE20H to FFF1FH Immediate data or labels FFE20H to ~~FF1FH~~ FFF1FH Immediate data or labels (even addresses only[Note])
:	:

Note Bit 0 = 0 when an odd address is specified.

No.121: Add the Caution for N-ch open-drain mode in chapters “35.3.1 and 36.3.1”

35.3.1 Pin Characteristics, 36.3.1 Pin Characteristics

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

No.122: Correct the information of conditions for IOL1 in chapter “35.3.1”

35.3.1 Pin Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/4)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Total of all pins (for duty factors ≤ 70% Note 2)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			65.0	mA
			~~2.7 V ≤ V_{DD} < 4.0 V~~ 2.7 V ≤ EV_{DD0} < 4.0 V			50.0	mA

No.123: Correct typo of Note 2 in chapters “35.3.2 and 36.3.2”

35.3.2 Supply Current Characteristics, 36.3.2 Supply Current Characteristics

Notes 1. When the high-speed on-chip oscillator clock and high-speed system clock are stopped.

2. Current flowing only to the watchdog timer (including the operation current of the ~~4.5~~ 15 kHz on-chip oscillator). The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

No.124: Correct typo in the Notes at the bottom of the table in chapter “35.5.1 and 36.5.1”

35.5.1 Serial Array Unit, 36.5.1 Serial Array Unit

(2) During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$ … internal clock output, normal slew rate)

Note 4. t_{KCY1} ≥ ~~4/f_{CLK}~~ 4/f_{MCK} must also be satisfied.

(3) During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$ … internal clock output, special slew rate)

Note 4. t_{KCY1} ≥ ~~4/f_{CLK}~~ 4/f_{MCK} must also be satisfied.

(9) During communication at different potential (3-V supply system) (CSI mode) (master mode, $\overline{SCKp}$ … internal clock output, normal slew rate)

Note 3. t_{KCY1} ≥ ~~4/f_{CLK}~~ 4/f_{MCK} must also be satisfied.

No.125: Correct the information of conditions in chapters “35.5.2 and 36.5.2”

35.5.2 Serial Interface IICA, 36.5.2 Serial Interface IICA

Parameter	Symbol	Conditions	Normal Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: 10 MHz ≤ ~~f_{CLK}~~ f_{MCK}					0	1000	kHz
		Fast mode: 3.5 MHz ≤ ~~f_{CLK}~~ f_{MCK}			0	400			kHz
		Normal mode: 1 MHz ≤ ~~f_{CLK}~~ f_{MCK}	0	100					kHz

No.126: Correct the information of conditions for “Overall error” in chapters “35.6.1 and 36.6.1”

35.6.1 A/D Converter Characteristics, 36.6.1 A/D Converter Characteristics

(1) When AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin: ANI2 to ANI23 (power supply: VDD)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution	4.0V≤VDD≤5.5V		~~1.2~~ ±1.2	±3.0	LSB
		AVREFP = VDD	2.7V≤VDD<4.0V		~~1.2~~ ±1.2	±3.5	LSB

(2) When AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin: ANI24 to ANI30 (power supply: EVDD0)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution	4.0V≤VDD≤5.5V		~~1.2~~ ±1.2	±4.5	LSB
		AVREFP = VDD	2.7V≤VDD<4.0V		~~1.2~~ ±1.2	±5.0	LSB

(3) When AVREF (+) = VDD (ADREFP1 = 0, ADREFP0 = 0), AVREF (-) = VSS (ADREFM = 0), target ANI pin: ANI0 to ANI23, ANI24 to ANI30

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution	4.0V≤VDD≤5.5V		~~1.2~~ ±1.2	±5.0	LSB
		ANI0 to ANI23	2.7V≤VDD<4.0V		~~1.2~~ ±1.2	±5.5	LSB
		10-bit resolution	4.0V≤VDD≤5.5V		~~1.2~~ ±1.2	±6.5	LSB
		ANI24 to ANI30	2.7V≤VDD<4.0V		~~1.2~~ ±1.2	±7.0	LSB

No.127: Correct the information of “target ANI pin” in chapters “35.6.1 and 36.6.1”

35.6.1 A/D Converter Characteristics, 36.6.1 A/D Converter Characteristics

(4) When AVREF (+) = internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin: ~~ANI0 to ANI23, ANI24 to ANI30~~ ANI0, ANI2 to ANI23, ANI24 to ANI30

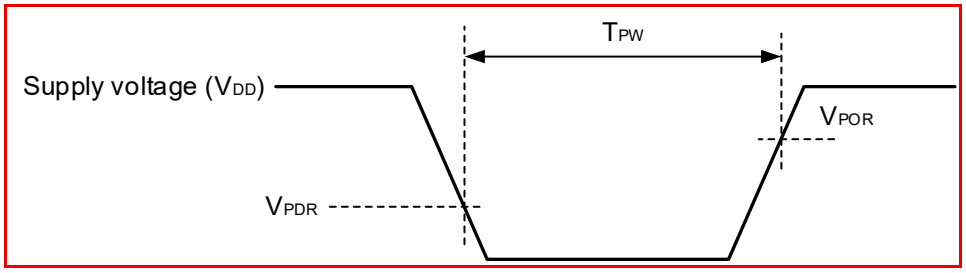
No.128: Add the information of Note and timing figure in chapters “35.6.5 and 36.6.5”

35.6.5 POR Circuit Characteristics, 36.6.5 POR Circuit Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage ~~Note~~ Note 1	VPOR	Power supply rise time	1.48	1.56	1.62	V
	VPDR	Power supply fall time	1.47	1.55	1.61	V
Minimum pulse width Note 2	TPW		300			μs
Detection delay time	TPD				350	μs

Notes 1. This indicates the POR circuit characteristics, and normal operation is not guaranteed under the condition of less than lower limit operation voltage (2.7 V).

2. Minimum time required for a POR reset when VDD exceeds below VPDR.

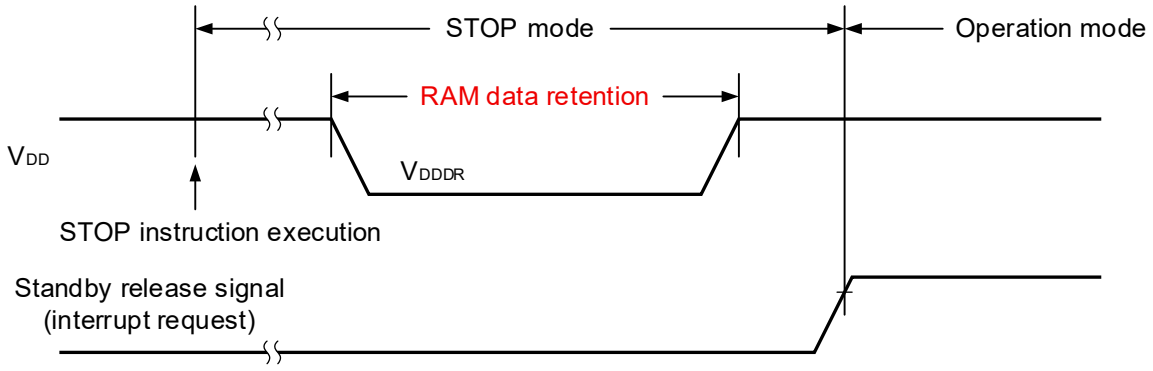


No.129: Correct chapter title, Note at the bottom of table, and timing figure in chapters “35.8 and 36.8”

35.8, 36.8 ~~STOP Mode Memory~~ RAM Data Retention Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47 Note		5.5	V

Note ~~The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.~~
This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



No.130: Correct the information of conditions and Note 1 at the bottom of table in chapters “35.9 and 36.9”

35.9 Flash Memory Programming Characteristics, 36.9 Flash Memory Programming Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years ~~(after rewrite)~~ T_A = +85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 20 years ~~(after rewrite)~~ T_A = +85°C Note 4	10,000			
		Retained for 5 years ~~(after rewrite)~~ T_A = +85°C Note 4	100,000			
Erase time	Terasa	Block erase	5			ms
Write time	Twrwa	1 word write	10			µs

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. ~~The retaining years are until next rewrite after the rewrite.~~ The starting point of the retaining years are after the erase.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. The average temperature for data retention.