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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0146A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice Descriptions of errors in the RL78/F12 User's Manual: Hardware Rev.1.11		Information Category	Technical Notification		
Applicable Product	RL78/F12 Group	Lot No. All lots	Reference Document	RL78/F12 User's Manual: Hardware Rev.1.11 (R01UH0231EJ0111)		

This document describes misstatements found in RL78/F12 User's Manual: Hardware Rev.1.11 (R01UH0231EJ0111).

These corrections will be made for the next revision of the User's Manual: Hardware Rev.1.20 (R01UH0231EJ0120).

Corrections:

(1/2)

No	Corrections	R01UH0231EJ0111	Pages in this document
1	1.2 Ordering Information: Add ordering part number	P.3	P.3
2	1.3.1 20-pin products: Typo in package type	P.4	P.4
3	1.3.2 30-pin products: Typo in package type	P.5	P.4
4	1.3.3 32-pin products: Typos in package type and diagrams	P.6	P.4
5	1.3.4 48-pin products: Typo in package type	P.7, 8	P.5
6	1.3.5 64-pin products: Typos in package type and diagrams	P.9	P.6
7	1.4 Pin Identification: Pins EV_{DD} and EV_{SS} are not listed	P.10	P.7
8	1.5.1 20-pin products: Typo in SCLxx pin direction	P.11	P.7
9	1.5.2 30-pin products: Typo in SCLxx pin direction	P.12	P.7
10	1.5.3 32-pin products: Typo in SCLxx pin direction	P.13	P.8
11	1.5.4 48-pin products: Typo in SCLxx pin direction	P.14	P.9
12	1.5.5 64-pin products: Typos in SCLxx pin direction and pin name	P.15	P.10
13	1.6 Outline of Functions: Unnecessary typo in serial interface	P.17	P.11
14	7.3, Figure 7-5: Add notes on real-time clock (TN-RL*-A058A)	P.336	P.12
15	7.4.1, Figure 7-17: Unnecessary typo in note 4	P.346	P.12
16	7.4.3, Figure 7-19 and Figure 7-20: Add notes on real-time clock (TN-RL*-A123A)	P.348, 349	P.12
17	8.3, Figure 8-4: Typo in the setting value of ITCMP[11:0] bits	P.358	P.13
18	11.4.3, Table 11-4: Add notes on watchdog timer (TN-RL*-A068A)	P.380	P.13
19	24.1, 24.3.2, 24.3.4, 24.3.5: Unnecessary typos in the IEC 61508	P.938, 943, 947	P.14
20	24.3.4, 24.3.4.1: Add notes on RAM guard function (TN-RL*-A071A)	P.947	P.15
21	24.3.6, Figure 24-10: Added notes on invalid memory access detection function (TN-RL*-A072A)	P.949	P.16
22	27.1, Table 27-1: Typos in package type	P.969	P.18
23	27.4.3 Procedure for accessing data flash memory: Add notes (TN-RL*-A096A)	P.977	P.18
24	31.6.2, 32.6.2: Typos in signal (SCLA0, SDAA0) and symbol (t_{BUF}) name	P.1038, 1069	P.19
25	31.7.1, 32.7.1: Typos in A/D characteristics table	P.1039 to 1042, P.1071 to 1074	P.20

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No	Corrections	R01UH0231EJ0111	Pages in this document
26	31.7.2: Typo in temperature sensor conditions	P.1043	P.20
27	31.7.3: Typo in POR circuit conditions	P.1043	P.21
28	31.7.4: Typo in remark	P.1044	P.21
29	32.4.2: Unnecessary typo in the supply current characteristics	P.1060	P.21
30	32.7.4: Typo in remark	P.1076	P.21
31	33.1 20-pin products: Add each code data to the package drawing	P.1079	P.22
32	33.2 30-pin products: Add each code data to the package drawing	P.1080	P.24
33	33.3 32-pin products: Add each code data to the package drawing	P.1081	P.26
34	33.3 32-pin products: Add the 32-pin product new package data	–	P.28
35	33.4 48-pin products: Add each code data to the package drawing	P.1082	P.29
36	33.4 48-pin products: Add each code data to the package drawing	P.1083	P.31
37	33.5 64-pin products: Add each code data to the package drawing	P.1084	P.33

Incorrect: Bold with underline; Correct: Gray hatched

No.1: 1.2 Ordering Information: Add ordering part number

(Incorrect)

• Flash memory version (lead-free product)

Pin count	Package	Data flash	Part Number
20 pins	20-pin plastic SSOP (7.62 mm (300))	Mounted	R5F10968JSP, R5F1096AJSP, R5F1096BJSP, R5F1096CJSP, R5F1096DJSP, R5F1096EJSP
30 pins	30-pin plastic SSOP (7.62 mm (300))	Mounted	R5F109AAJSP, R5F109ABJSP, R5F109ACJSP, R5F109ADJSP, R5F109AEJSP
32 pins	32-pin plastic WQFN fine pitch) (5 × 5)	Mounted	R5F109BAJNA, R5F109BBJNA, R5F109BCJNA, 5F109BDJNA, R5F109BEJNA
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	Mounted	R5F109GAJFB, R5F109GBJFB, R5F109GCJFB, R5F109GDJFB, R5F109GEJFB
	48-pin plastic WQFN (7 × 7) Note	Mounted	R5F109GAJNA, R5F109GBJNA, R5F109GCJNA, R5F109GDJNA, R5F109GEJNA
64 pins	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	R5F109LAJFB, R5F109LBJFB, R5F109LCJFB, R5F109LDJFB, R5F109LEJFB

Note Contact Renesas local sales office or sales representative for further details on this package.

(Correct)

• Flash memory version (lead-free product)

Pin count	Package	Device	Part Number
20 pins	20-pin plastic LSSOP (7.62 mm (300))	Version J	R5F10968JSP, R5F10968CJSP, R5F1096AJSP, R5F1096ACJSP, R5F1096BJSP, R5F1096BCJSP, R5F1096CJSP, R5F1096CCJSP, R5F1096DJSP, R5F1096DCJSP, R5F1096EJSP, R5F1096ECJSP
		Version K	R5F10968KSP, R5F10968CKSP, R5F1096AKSP, R5F1096ACKSP, R5F1096BKSP, R5F1096BCKSP, R5F1096CKSP, R5F1096CCKSP, R5F1096DKSP, R5F1096DCKSP, R5F1096EKSP, R5F1096ECKSP
30 pins	30-pin plastic LSSOP (7.62 mm (300))	Version J	R5F109AAJSP, R5F109AACJSP, R5F109ABJSP, R5F109ABCJSP, R5F109ACJSP, R5F109ACCJSP, R5F109ADJSP, R5F109ADCJSP, R5F109AEJSP, R5F109AECJSP
		Version K	R5F109AAKSP, R5F109AACKSP, R5F109ABKSP, R5F109ABCKSP, R5F109ACKSP, R5F109ACCKSP, R5F109ADKSP, R5F109ADCKSP, R5F109AEKSP, R5F109AECKSP
32 pins	32-pin plastic HWQFN (fine pitch) (5 × 5)	Version J	R5F109BAJNA, R5F109BACJNA, R5F109BBJNA, R5F109BBCJNA, R5F109BCJNA, R5F109BCCJNA, R5F109BDJNA, R5F109BDCJNA, R5F109BEJNA, R5F109BECJNA
		Version K	R5F109BAKNA, R5F109BACKNA, R5F109BBKNA, R5F109BBCKNA, R5F109BCKNA, R5F109BCCKNA, R5F109BDKNA, R5F109BDCKNA, R5F109BEKNA, R5F109BECKN
48 pins	48-pin plastic LFQFP (fine pitch) (7 × 7)	Version J	R5F109GACJFB, R5F109GBCJFB, R5F109GCCJFB, R5F109GDCJFB, R5F109GECJFB
		Version K	R5F109GACKFB, R5F109GBCKFB, R5F109GCCKFB, R5F109GDCKFB, R5F109GECKFB
	48-pin plastic HWQFN (7 × 7) Note	Version J	R5F109GAJNA, R5F109GBJNA, R5F109GCJNA, R5F109GDJNA, R5F109GEJNA
		Version K	R5F109GAKNA, R5F109GBKNA, R5F109GCKNA, R5F109GDKNA, R5F109GEKNA
64 pins	64-pin plastic LFQFP (fine pitch) (10 × 10)	Version J	R5F109LACJFB, R5F109LBCJFB, R5F109LCCJFB, R5F109LDCJFB, R5F109LECJFB
		Version K	R5F109LACKFB, R5F109LBCKFB, R5F109LCCKFB, R5F109LDCKFB, R5F109LECKFB

Note Contact Renesas local sales office or sales representative for further details on this package.

No.2: 1.3.1 20-pin products

(Incorrect)

• 20-pin plastic **SSOP** (7.62 mm (300))

(Correct)

• 20-pin plastic LSSOP (7.62 mm (300))

No.3: 1.3.2 30-pin products

(Incorrect)

• 30-pin plastic **SSOP** (7.62 mm (300))

(Correct)

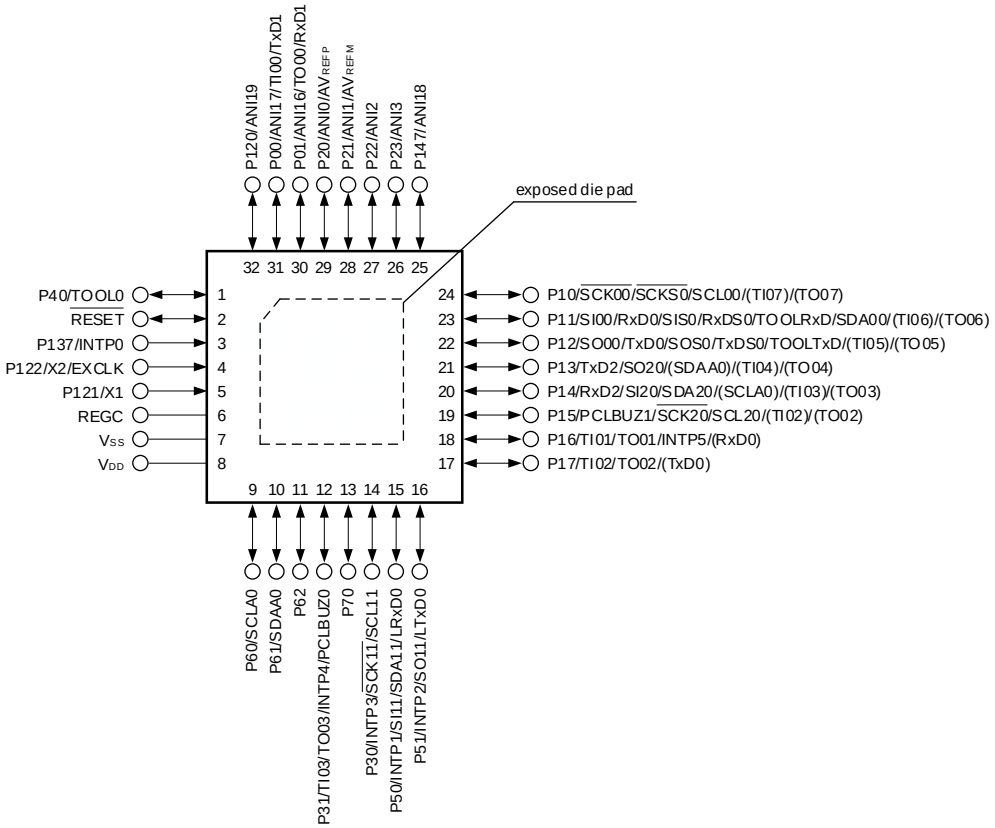
• 30-pin plastic LSSOP (7.62 mm (300))

No.4: 1.3.3 32-pin products

(Incorrect)

• 32-pin plastic **WQFN** (fine pitch) (5 × 5)

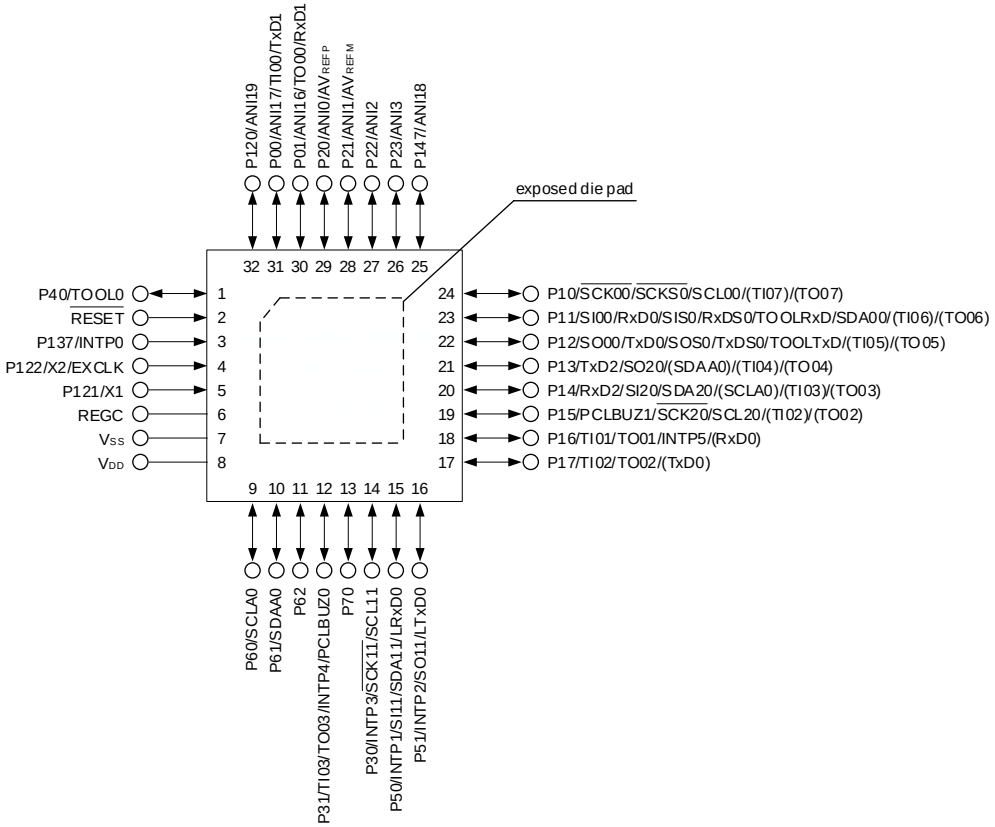
Direction of the arrow on RESET pin (**bidirectional**)



(Correct)

• 32-pin plastic HWQFN (fine pitch) (5 × 5)

Direction of the arrow on RESET pin (input direction)



No.5: 1.3.4 48-pin products

(Incorrect)

• 48-pin plastic **LQFP** (fine pitch) (7 × 7)
• 48-pin plastic **WQFN** (7 × 7)

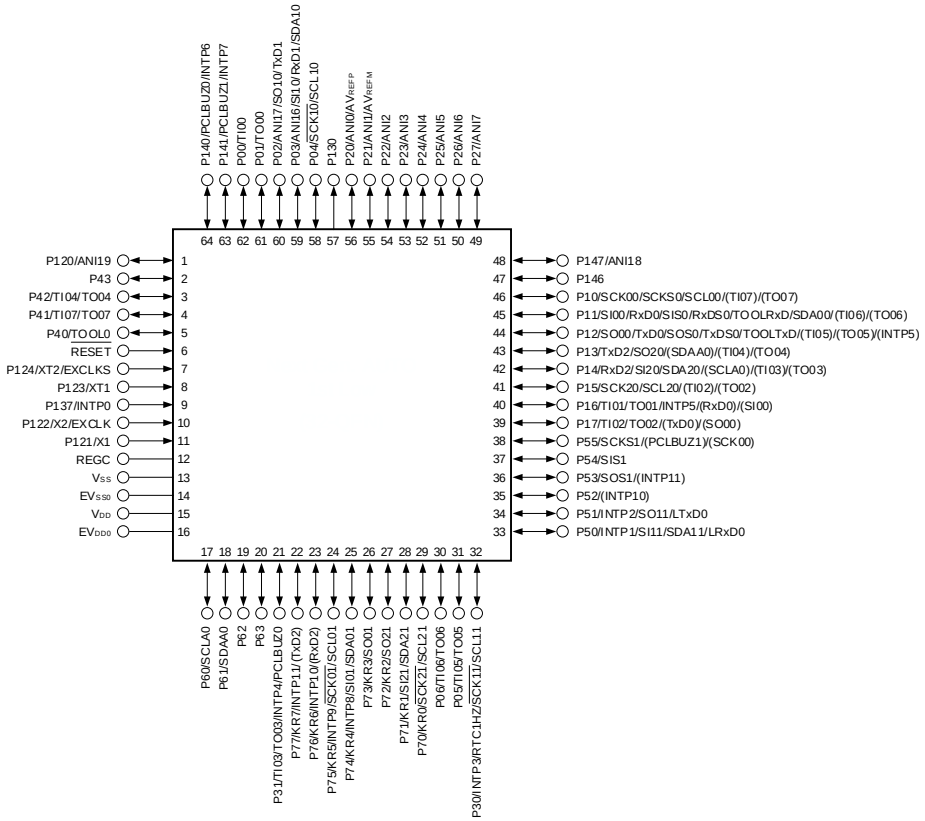
(Correct)

• 48-pin plastic LFQFP (fine pitch) (7 × 7)
• 48-pin plastic HWQFN (7 × 7)

No.6: 1.3.5 64-pin products

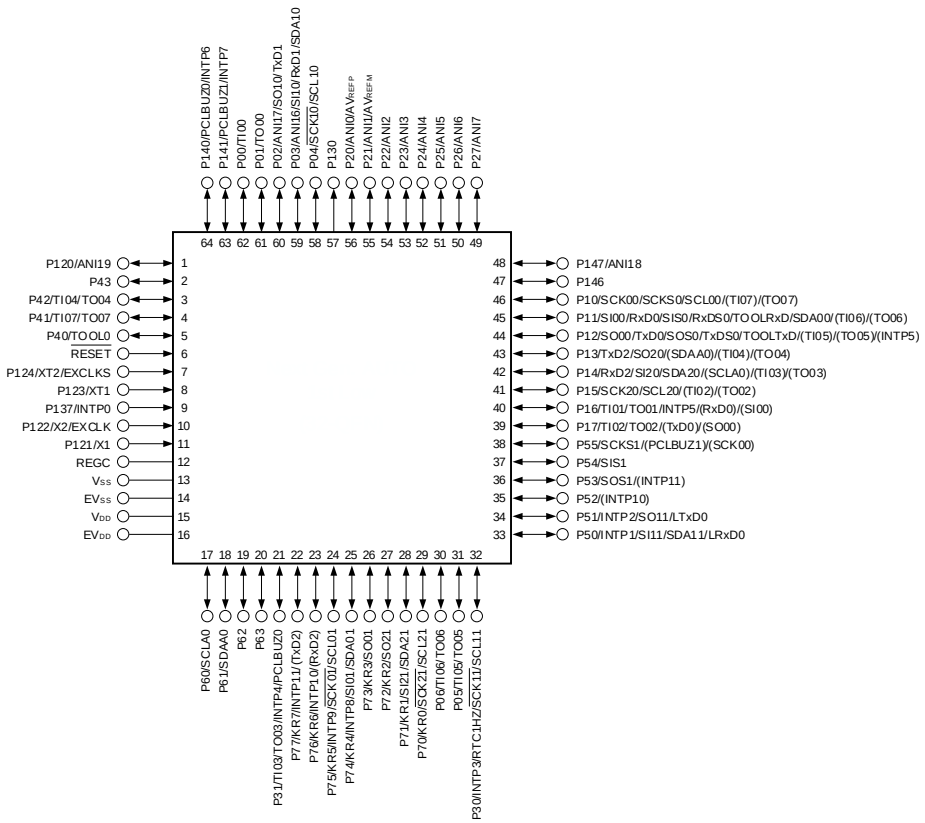
(Incorrect)

• 64-pin plastic **LQFP** (fine pitch) (10 × 10)
Pin Name: 14 pin: **EVSS0**, 16 pin: **EVDD0**



(Correct)

• 64-pin plastic LFQFP (fine pitch) (10 × 10)
Pin Name: 14 pin: EVSS, 16 pin: EVDD



No.7: 1.4 Pin Identification

(Incorrect)

VDD:	Power supply
VSS:	Ground

(Correct) Added description of pins EVDD and EVSS.

EVDD, VDD:	Power supply
EVSS, VSS:	Ground

No.8: 1.5.1 20-pin products

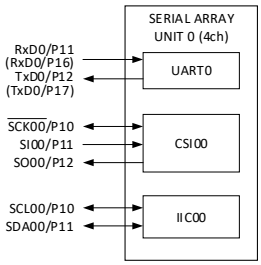
(Incorrect)

Direction of the arrow on SCL00/P10 pin in the Figure (**bidirectional**)

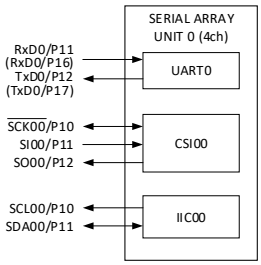
(Correct) Corrected the block diagram.

Direction of the arrow on SCL00/P10 pin in the Figure (output direction)

(Incorrect)



(Correct)



No.9: 1.5.2 30-pin products

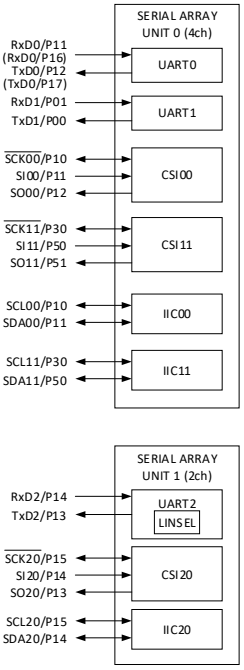
(Incorrect)

Direction of the arrow on pins SCL00/P10 and SCL11/P30, and SCL20/P15 pin in the Figure (**bidirectional**)

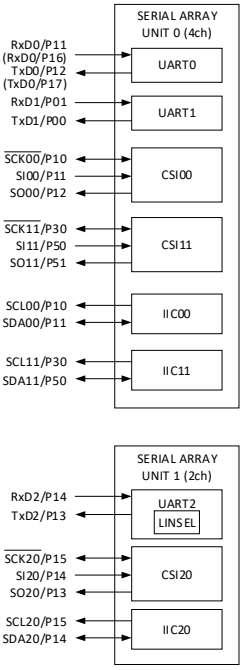
(Correct) Corrected the block diagram.

Direction of the arrow on pins SCL00/P10 and SCL11/P30, and SCL20/P15 pin in the Figure (output direction)

(Incorrect)



(Correct)



No.10: 1.5.3 32-pin products

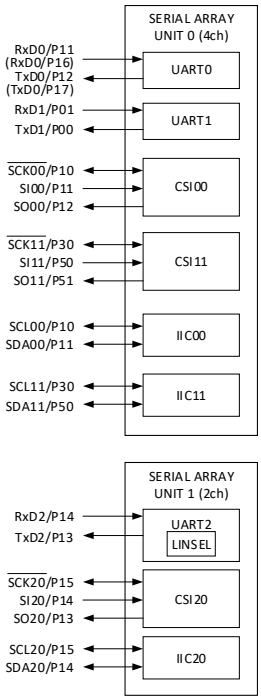
(Incorrect)

Direction of the arrow on pins SCL00/P10 and SCL11/P30, and SCL20/P15 pin in the Figure (**bidirectional**)

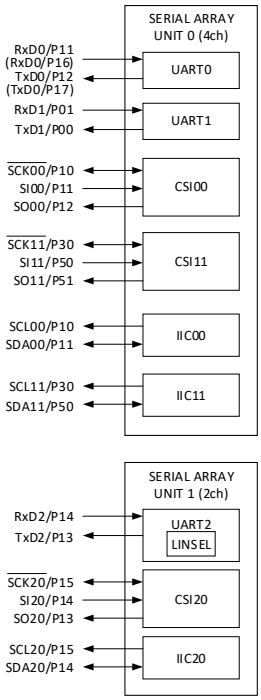
(Correct) Corrected the block diagram.

Direction of the arrow on pins SCL00/P10 and SCL11/P30, and SCL20/P15 pin in the Figure (output direction)

(Incorrect)



(Correct)



No.11: 1.5.4 48-pin products

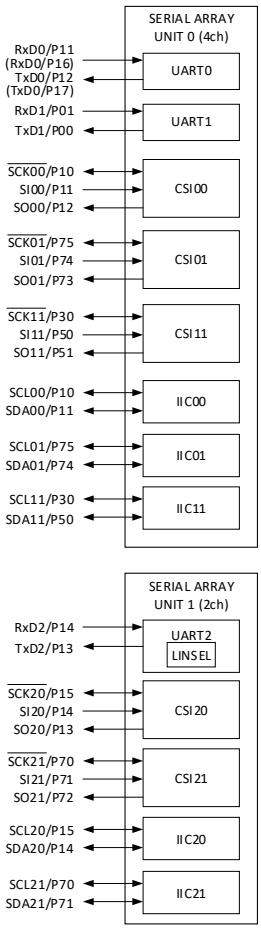
(Incorrect)

Direction of the arrow on pins SCL00/P10, SCL01/P75 and SCL11/P30, and pins SCL20/P15 and SCL21/P70 in the Figure (**bidirectional**)

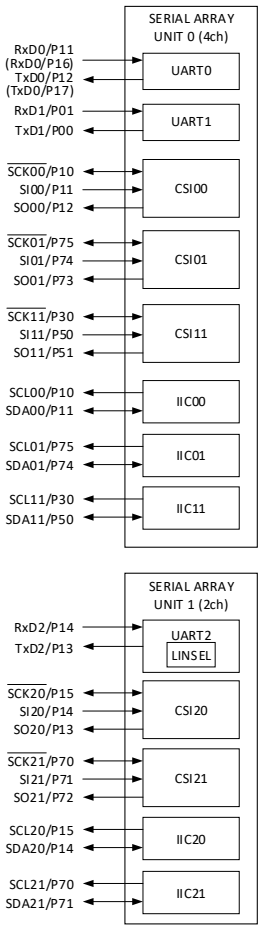
(Correct) Corrected the block diagram.

Direction of the arrow on pins SCL00/P10, SCL01/P75 and SCL11/P30, and pins SCL20/P15 and SCL21/P70 in the Figure (output direction)

(Incorrect)



(Correct)



No.12: 1.5.5 64-pin products

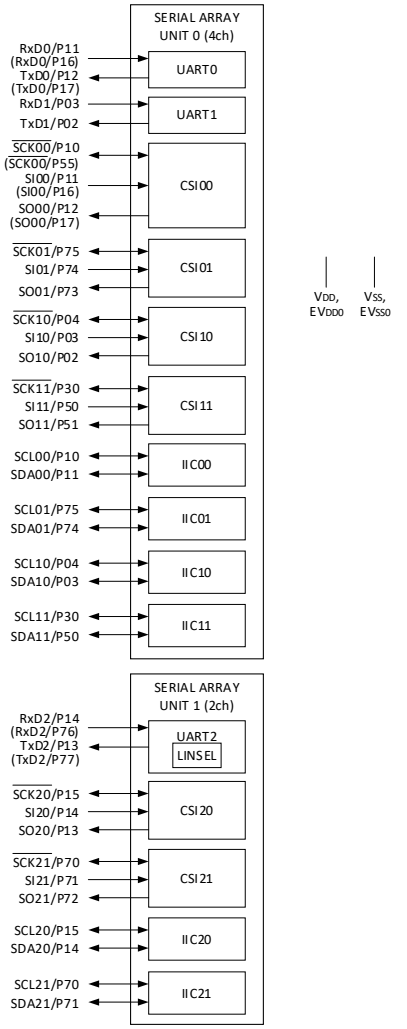
(Incorrect)

Direction of the arrow on pins SCL00/P10, SCL01/P75, SCL10/P04 and SCL11/P30, and pins SCL20/P15 and SCL21/P70 in the Figure (**bidirectional**). Corrected typos (**EV_{DD0}, EV_{SS0}**)

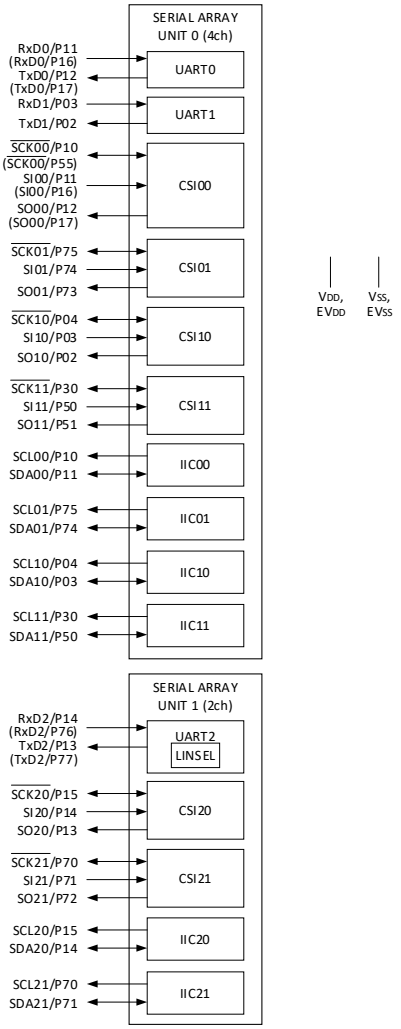
(Correct) Corrected the block diagram.

Direction of the arrow on pins SCL00/P10, SCL01/P75, SCL10/P04 and SCL11/P30, and pins SCL20/P15 and SCL21/P70 in the Figure (output direction). Corrected typos (EV_{DD}, EV_{SS})

(Incorrect)



(Correct)



No.13: 1.6 Outline of Functions

(Incorrect)

(2/2)

Item	20-pin	30-pin	32-pin	48-pin	64-pin
	R5F1096x	R5F109Ax	R5F109Bx	R5F109Gx	R5F109Lx
Serial interface	[20-pin, **24-pin**, **25-pin** products] • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel • LIN-UART: 1 channel [30-pin, 32-pin products] • CSI: 2 channels/UART: 2 channels/simplified I^2C: 2 channels • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI (7 to 16 bits): 1 channel/UART (7 to 9, 16 bits): 1 channel • LIN-UART: 1 channel [48-pin products] • CSI: 3 channels/UART: 2 channels/simplified I^2C: 3 channels • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI (7 to 16 bits): 1 channel/UART (7 to 9, 16 bits): 1 channel • LIN-UART: 1 channel [64-pin products] • CSI: 4 channels/UART: 2 channels/simplified I^2C: 4 channels • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI (7 to 16 bits): 2 channels/UART (7 to 9, 16 bits): 1 channel • LIN-UART: 1 channel				
I^2C bus	–	1 channel	1 channel	1 channel	

(Correct) Deleted unnecessary information.

(2/2)

Item	20-pin	30-pin	32-pin	48-pin	64-pin
	R5F1096x	R5F109Ax	R5F109Bx	R5F109Gx	R5F109Lx
Serial interface	[20-pin products] • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel • LIN-UART: 1 channel [30-pin, 32-pin products] • CSI: 2 channels/UART: 2 channels/simplified I^2C: 2 channels • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI (7 to 16 bits): 1 channel/UART (7 to 9, 16 bits): 1 channel • LIN-UART: 1 channel [48-pin products] • CSI: 3 channels/UART: 2 channels/simplified I^2C: 3 channels • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI (7 to 16 bits): 1 channel/UART (7 to 9, 16 bits): 1 channel • LIN-UART: 1 channel [64-pin products] • CSI: 4 channels/UART: 2 channels/simplified I^2C: 4 channels • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels • CSI (7 to 16 bits): 2 channels/UART (7 to 9, 16 bits): 1 channel • LIN-UART: 1 channel				
I^2C bus	–	1 channel	1 channel	1 channel	

No.14: 7.3 Registers Controlling Real-time Clock, Figure 7-5 RTCC1 register

(Incorrect)

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value.

This bit controls the operation of the counter.
Be sure to write “1” to it to read or write the counter value.
As the counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0.
When RWAIT = 1, it takes up to 1 clock (fRTC) until the counter value can be read or written (RWST = 1).
When the counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

(Correct) Added notes on real-time clock.

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value.

This bit controls the operation of the counter.
Be sure to write “1” to it to read or write the counter value.
As the counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0.
When RWAIT = 1, it takes up to 1 clock (fRTC) until the counter value can be read or written (RWST = 1). Notes1,2
When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.
When the counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.
However, when it wrote a value to second count register, it will not keep the overflow event.

Notes 1. When setting RWAIT=1 during 1 operating clock (fRTC), after setting RTCE=1, it may take two clock time of the operation clock (fRTC), until RWST bit is set to "1".
2. When setting RWAIT=1 during 1 operating clock (fRTC), after returning from a stand-by (HALT mode, STOP mode and SNOOZE mode), it may take two clock time of the operation clock (fRTC), until RWST bit is set to "1".

No.15: 7.4.1 Starting operation of real-time clock, Figure 7-17

Note 4 at the bottom of the figure

(Incorrect)

Notes 1. First set the RTCEN bit to 1, while oscillation of the input clock (fRTC) is stable.
4. Set RWAIT to 0, after completion of reading or writing the counter.

(Correct) Deleted unnecessary information.

Notes 1. First set the RTCEN bit to 1, while oscillation of the input clock (fRTC) is stable.
Deleted Note 4 (because the subject is not specified in the figure).

No.16: 7.4.3 Reading/writing real-time clock, Figure 7-19 and Figure 7-20

Caution at the bottom of the figure

(Incorrect)

Caution Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

(Correct) Added notes on real-time clock.

Caution Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.
When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

No.17: 8.3 Registers Controlling Interval Timer, Figure 8-4 ITMC register

(Incorrect)

ITCMP11 to ITCMP0	Specification of the interval timer compare value
001H	These bits generate an interrupt at the fixed cycle (count clock cycles x (ITCMP setting + 1)).
• • •	
~~FFFH1~~	
Example interrupt cycles when 001H or FFFH is specified for ITCMP11 to ITCMP0 • ITCMP11 to ITCMP0 = 001H, count clock: when f_{SUB} = 32.768 kHz 1/32.768 [kHz] × (1 + 1) = 0.06103515625 [ms] ≅ 61.03 [μs] • ITCMP11 to ITCMP0 = FFFH, count clock: when f_{SUB} = 32.768 kHz 1/32.768 [kHz] × (4095 + 1) = 125 [ms]	

(Correct) Corrected the typo in the setting value of ITCMP[11:0] bits.

ITCMP11 to ITCMP0	Specification of the interval timer compare value
001H	These bits generate an interrupt at the fixed cycle (count clock cycles x (ITCMP setting + 1)).
• • •	
FFFH	
Example interrupt cycles when 001H or FFFH is specified for ITCMP11 to ITCMP0 • ITCMP11 to ITCMP0 = 001H, count clock: when f_{SUB} = 32.768 kHz 1/32.768 [kHz] × (1 + 1) = 0.06103515625 [ms] ≅ 61.03 [μs] • ITCMP11 to ITCMP0 = FFFH, count clock: when f_{SUB} = 32.768 kHz 1/32.768 [kHz] × (4095 + 1) = 125 [ms]	

No.18: 11.4.3 Setting window open period of watchdog timer, Table 11-4

(Incorrect)

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	Setting prohibited
0	1	50%
1	0	75%
1	1	100%

(Correct) Added notes on watchdog timer.

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	Setting prohibited
0	1	50%
1	0	75% **Note**
1	1	100%

Note When the window open period is set to 75%, clearing the counter of the watchdog timer (writing ACH to WDTE) must proceed outside the corresponding period from among those listed below, over which clearing of the counter is prohibited (for example, confirming that the interval timer interrupt request flag (WDTIIF) of the watchdog timer is set).

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time (f_{IL} = 17.25 kHz (MAX.))	Period over which clearing the counter is prohibited when the window open period is set to 75%
0	0	0	$2^6/f_{IL}$ (3.71 ms)	1.85 ms to 2.51 ms
0	0	1	$2^7/f_{IL}$ (7.42 ms)	3.71 ms to 5.02 ms
0	1	0	$2^8/f_{IL}$ (14.84 ms)	7.42 ms to 10.04 ms
0	1	1	$2^9/f_{IL}$ (29.68 ms)	14.84 ms to 20.08 ms
1	0	0	$2^{11}/f_{IL}$ (118.72 ms)	56.36 ms to 80.32 ms
1	0	1	$2^{13}/f_{IL}$ (474.89 ms)	237.44 ms to 321.26 ms
1	1	0	$2^{14}/f_{IL}$ (949.79 ms)	474.89 ms to 642.51 ms
1	1	1	$2^{16}/f_{IL}$ (3799.18 ms)	1899,59 ms to 2570.04 ms

No.19: 24.1, 24.3.2, 24.3.4, 24.3.5 IEC 61508 unnecessary descriptions

(Incorrect)

24.1 Overview of Safety Functions

The RL78/F12 is provided with the following safety functions to meet the **IEC 60730 and IEC 61508** safety standards.
The functions are intended to detect failures through microcomputer's self-diagnosis and to stop the system safely.

24.3.2 CRC Operation Function (General-Purpose CRC)

The IEC 61508 standard requires safety to be guaranteed during operation and thus the means for data verification during CPU operation is necessary.

With the general-purpose CRC operation function, the CRC operation is possible as a peripheral function during CPU operation.

24.3.4 RAM Guard Function

The IEC 61508 standard requires safety to be guaranteed during operation and thus it is necessary to protect significant data stored in RAM when the CPU freezes.

The RAM guard function protects data in the specified space.
Setting this function disables writing to RAM in the specified space but enables reading normally.

24.3.5 SFR Guard Function

The IEC 61508 standard requires safety to be guaranteed during operation and thus it is necessary to prevent significant SFRs from being erroneously rewritten when the CPU freezes.

The SFR guard function protects data in the registers used to control the port function, interrupt function, clock control function, voltage detection circuits, and RAM parity error detection function.
Setting this function disables writing to guarded SFRs but enables reading normally.

(Correct)

24.1 Overview of Safety Functions

The RL78/F12 is provided with the following safety functions to meet the IEC 60730 safety standards.
The functions are intended to detect failures through microcomputer's self-diagnosis and to stop the system safely.

24.3.2 CRC Operation Function (General-Purpose CRC)

With the general-purpose CRC operation function, the CRC operation is possible as a peripheral function during CPU operation.

24.3.4 RAM Guard Function

The RAM guard function protects data in the specified space.
Setting this function disables writing to RAM in the specified space but enables reading normally.

24.3.5 SFR Guard Function

The SFR guard function protects data in the registers used to control the port function, interrupt function, clock control function, voltage detection circuits, and RAM parity error detection function.
Setting this function disables writing to guarded SFRs but enables reading normally.

No.20: 24.3.4, Figure 24-8, Add notes on RAM guard function

(Incorrect)

24.3.4 RAM Guard Function

The RAM guard function protects data in the specified space.

Setting this function disables writing to RAM in the specified space but enables reading normally.

GRAM1	GRAM0	RAM guard space Note
0	0	Disabled. RAM can be written to.
0	1	The 128 bytes starting at the lower RAM address
1	0	The 256 bytes starting at the lower RAM address
1	1	The 512 bytes starting at the lower RAM address

Note The RAM start address differs depending on the size of the RAM provided with the product.

(Correct)

24.3.4 RAM Guard Function

The RAM guard function protects data in the specified space.

Setting this function disables writing to RAM in the specified space but enables reading normally.

Caution: RAM guard function is not available on RAM capacities 1.5KB products

RAM capacities 1.5KB products: R5F1096B, R5F109AB, R5F109BB, R5F109GB and R5F109LB

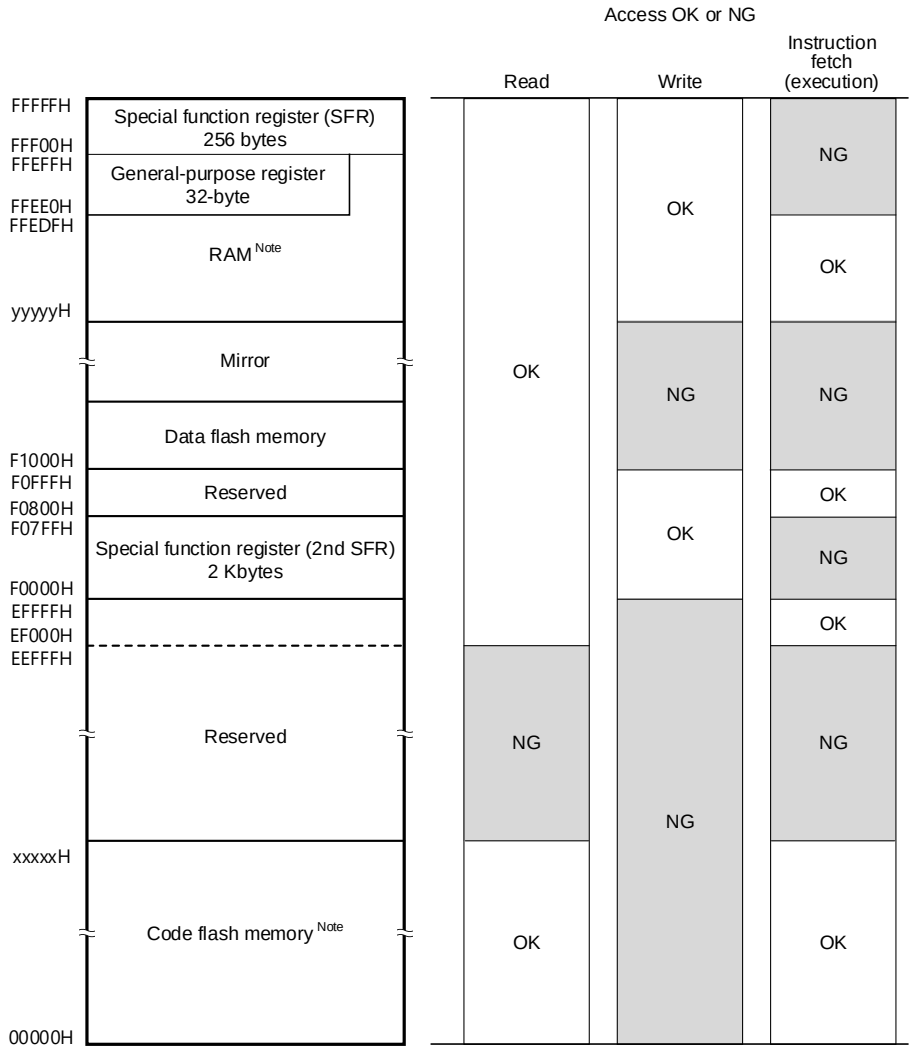
GRAM1	GRAM0	RAM guard space Note
0	0	Disabled. RAM can be written to.
0	1	The 128 bytes starting at the lower RAM address
1	0	The 256 bytes starting at the lower RAM address
1	1	The 512 bytes starting at the lower RAM address

Note The RAM start address differs depending on the size of the RAM provided with the product.

RAM guard function is not available on RAM capacities 1.5KB products.

No.21: 24.3.6 Invalid Memory Access Detection Function, Figure 24-10

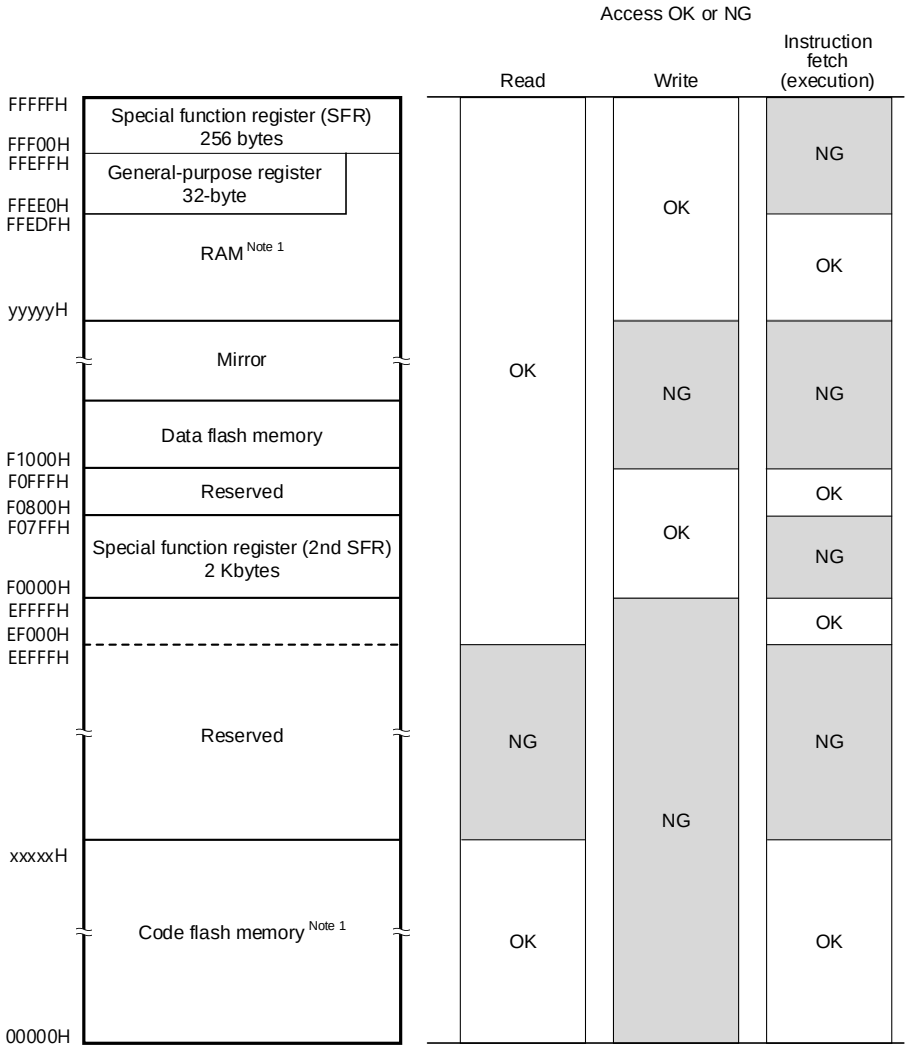
(Incorrect)



Note The addresses of the RAM and code flash memory are shown below according to the product type.

Product Type	Code Flash Memory (00000H to xxxxxH)	RAM (yyyyyH to FFFFFH)
R5F109xA	8192 × 8 bits (00000H to 01FFFH)	512 × 8 bits
R5F109xA (x = 6, A, B, G, L)	16384 × 8 bits (00000H to 03FFFH)	1024 × 8 bits
R5F109xB (x = 6, A, B, G, L)	24576 × 8 bits (00000H to 05FFFH)	1536 × 8 bits
R5F109xC (x = 6, A, B, G, L)	32768 × 8 bits (00000H to 07FFFH)	2048 × 8 bits (FF700H to FFEFFH)
R5F109xD (x = 6, A, B, G, L)	49152 × 8 bits (00000H to 0BFFFH)	2048 × 8 bits (FF300H to FFEFFH)
R5F109xE (x = 6, A, B, G, L)	65536 × 8 bits (00000H to 0FFFFH)	2048 × 8 bits (FEF00H to FFEFFH)

(Correct) Added notes on invalid memory access detection function.



Notes 1. The addresses of the RAM and code flash memory are shown below according to the product type.

Product Type	Code Flash Memory (00000H to xxxxxH)	RAM (yyyyyH to FFFFFH)
R5F10968	8192 × 8 bits (00000H-01FFFH) Note 2	512 × 8 bits (FFD00H-FFEFFH)
R5F109xA (x = 6, A, B, G, L)	16384 × 8 bits (00000H-03FFFH) Note 2	1024 × 8 bits (FFB00H-FFEFFH)
R5F109xB (x = 6, A, B, G, L)	24576 × 8 bits (00000H-05FFFH) Note 2	1536 × 8 bits (FF900H-FFEFFH) Note 3
R5F109xC (x = 6, A, B, G, L)	32768 × 8 bits (00000H-07FFFH) Note 2	2048 × 8 bits (FF700H-FFEFFH)
R5F109xD (x = 6, A, B, G, L)	49152 × 8 bits (00000H-0BFFFH) Note 2	2048 × 8 bits (FF300H-FFEFFH)
R5F109xE (x = 6, A, B, G, L)	65536 × 8 bits (00000H-0FFFFH)	2048 × 8 bits (FEF00H-FFEFFH)

2. Fetching of an instruction (for execution) by illegal to a location in the area from xxxxxH-0FFFFH leads to the generation of a reset due the execution of an illegal instruction rather than being handled as illegal memory access. In case of reading a reset does not generate and “FFH” is read.

3. Fetching of an instruction (for execution) by illegal to a location in the area from FF700H-FF8FFH, a reset does not generate by invalid memory access detection but it may generate by RAM parity error. In case of writing, it does not generate by invalid memory access detection.

No.22: 27.1 Writing to Flash Memory by Using Flash Memory Programmer, Table 27-1

(Incorrect)

Pin Configuration of Dedicated Flash Memory Programmer				Pin Name	Pin No.				
Signal Name		I/O	Pin Function		20-pin	30-pin	32-pin	48-pin	64-pin
PG-FP5, FL-PR5	E1 on-chip debugging emulator				~~SSOP~~	~~SSOP~~	~~WQFN (5×5)~~	~~LQFP (7×7), WQFN (7×7)~~	~~LQFP (10×10)~~
–	TOOL0	I/O	Transmit/receive signal	TOOL0/P40	3	5	1	39	5
SI/RxD	–	I/O	Transmit/receive signal						

(Correct) Corrected the description of the package name.

Pin Configuration of Dedicated Flash Memory Programmer				Pin Name	Pin No.				
Signal Name		I/O	Pin Function		20-pin	30-pin	32-pin	48-pin	64-pin
PG-FP5, FL-PR5	E1 on-chip debugging emulator				LSSOP	LSSOP	HWQFN	LFQFP, HWQFN	LFQFP
–	TOOL0	I/O	Transmit/receive signal	TOOL0/P40	3	5	1	39	5
SI/RxD	–	I/O	Transmit/receive signal						

No.23: 27.4.3 Procedure for accessing data flash memory

(Incorrect)

Cautions 1. Accessing the data flash memory is not possible during the setup time.

:

4. The data flash should be read in either of following ways.

- Use the flash library provided by Renesas (EEL (Pack01) version V1.13 or later).
- Stop the DMA transfer before reading.

(Correct) Added notes on data flash memory access.

Cautions 1. Accessing the data flash memory is not possible during the setup time.

:

4. The data flash should be read in either of following ways.

- Use the flash library provided by Renesas (EEL (Pack01) version V1.13 or later).
- Stop the DMA transfer before reading.

5. If accessing data flash memory when the f_{SUB} (subsystem clock) is selected as f_{CLK} (CPU/peripheral hardware clock), take one of the following procedures.:

i) To switch f_{CLK} from f_{SUB} to the main system clock, follow these steps (1) to (3).

(1) Confirming the complete switching to main system clock (CLS* = 0).

(2) Read any data flash memory address as a dummy read (don't use the read value).

(3) Waiting until the following time has been passed:

HS (high-speed main) mode: 5 μs

LS (low-speed main) mode: 1 μs

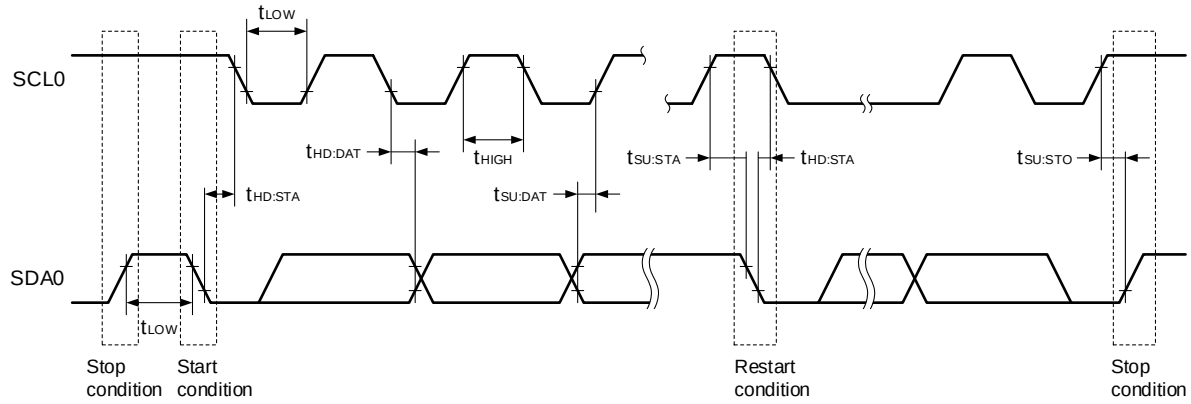
*: Bit of the system clock control register (CKC)

ii) Do not read data flash memory when f_{SUB} is selected as f_{CLK}.

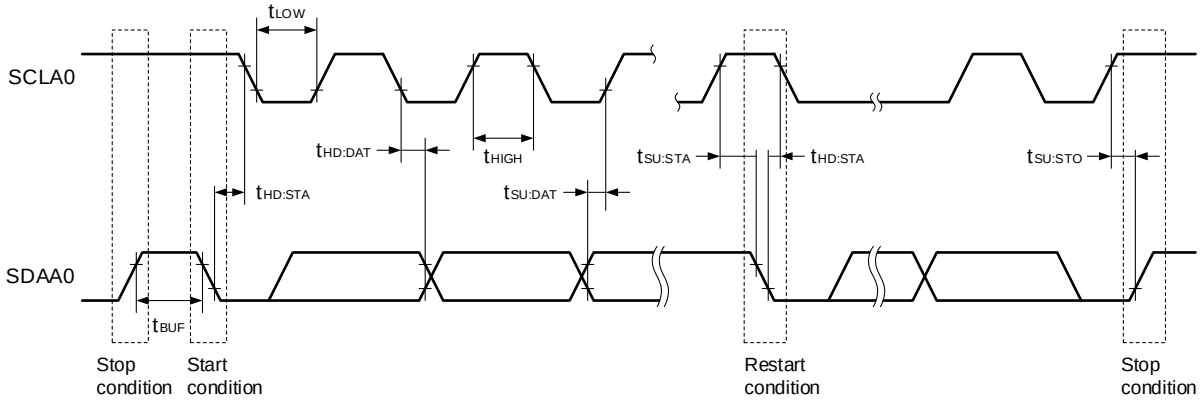
If data flash content needs to be accessed during f_{SUB} is selected as f_{CLK}, store the required data flash content to RAM before setting f_{SUB} to f_{CLK}. And read copied content from RAM.

No.24: 31.6.2, 32.6.2 Serial interface IICA, IICA serial transfer timing

(Incorrect)



(Correct) Corrected typos in signal (SCLA0, SDAA0) and symbol (tBUF) names.



No.25: 31.7.1, 32.7.1 A/D converter characteristics, Characteristics table

(Incorrect)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V		~~1.2~~	±3.0	LSB
			1.8 V ≤ V_{DD} < 4.0 V		~~1.2~~	±3.5	LSB

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} AV_{REFM} = V_{SS}	4.0 V ≤ V_{DD} ≤ 5.5 V		~~1.2~~	±4.5	LSB
			1.8 V ≤ V_{DD} < 4.0 V		~~1.2~~	±5.0	LSB

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	ANI0-ANI7		~~1.2~~	±5.0	LSB
			1.8 V ≤ V_{DD} < 4.0 V	ANI0-ANI7		~~1.2~~	±5.5	LSB

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	ANI16-ANI19		~~1.2~~	±6.5	LSB
			1.8 V ≤ V_{DD} < 4.0 V	ANI16-ANI19		~~1.2~~	±7.0	LSB
Analog input voltage	V_{AIN}	ANI16-ANI19			V_{SS}		~~EV_{DD0}~~	V

(Correct) Corrected the description in the A/D characteristics table.

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±3.0	LSB
			1.8 V ≤ V_{DD} < 4.0 V		±1.2	±3.5	LSB

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} AV_{REFM} = V_{SS}	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±4.5	LSB
			1.8 V ≤ V_{DD} < 4.0 V		±1.2	±5.0	LSB

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	ANI0-ANI7		±1.2	±5.0	LSB
			1.8 V ≤ V_{DD} < 4.0 V	ANI0-ANI7		±1.2	±5.5	LSB

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Overall error Note 1	AINL	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	ANI16-ANI19		±1.2	±6.5	LSB
			1.8 V ≤ V_{DD} < 4.0 V	ANI16-ANI19		±1.2	±7.0	LSB
Analog input voltage	V_{AIN}	ANI16-ANI19			V_{SS}		V_{DD}	V

No.26: 31.7.2 Temperature sensor characteristics, Description of conditions

(Incorrect)

(T_A = −40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = **EV_{SS0} = EV_{SS1}** = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V

(Correct) Corrected typo.

(T_A = −40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V

No.27: 31.7.3 POR circuit characteristics, Description of conditions

(Incorrect)

(T_A = −40 to +85°C, V_{SS} = **EVss** = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.46	1.51	1.59	V

(Incorrect) Corrected typo.

(T_A = −40 to +85°C, V_{SS} = EVss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.46	1.51	1.59	V

No.28: 31.7.4 LVD circuit characteristics, Remark at the bottom of the characteristics table.

(Incorrect)

Remark $V_{LVI(n-1)}$ > V_{LVIn}: **n = 1 to 13**

(Incorrect) Corrected typo.

Remark $V_{LVI(n-1)}$ > V_{LVIn}: n = 1 to 11

No.29: 32.4.2 Supply current characteristics, Description in the table

(Incorrect)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current **Note 1**	I_{DD2} **Note 2**	HALT mode	High-speed operation **Note 7**	f_{IH} = 24 MHz **Note 3**		0.48	5.38	mA
				f_{IH} = 16 MHz **Note 3**		0.40	3.90	mA
				f_{IH} = 8 MHz **Note 3**		**TBD**	**TBD**	mA
				f_{MX} = 20 MHz **Note 4**		0.43	1.88	mA
				f_{MX} = 10 MHz **Note 4**		0.28	1.02	mA
				f_{MX} = 8 MHz **Note 4**		**TBD**	**TBD**	mA

(Incorrect) Deleted unnecessary information.

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current **Note 1**	I_{DD2} **Note 2**	HALT mode	High-speed operation **Note 7**	f_{IH} = 24 MHz **Note 3**		0.48	5.38	mA
				f_{IH} = 16 MHz **Note 3**		0.40	3.90	mA
				f_{MX} = 20 MHz **Note 4**		0.43	1.88	mA
				f_{MX} = 10 MHz **Note 4**		0.28	1.02	mA

No.30: 32.7.4 LVD circuit characteristics, Remark at the bottom of the characteristics table.

(Incorrect)

Remark $V_{LVI(n-1)}$ > V_{LVIn}: **n = 1 to 13**

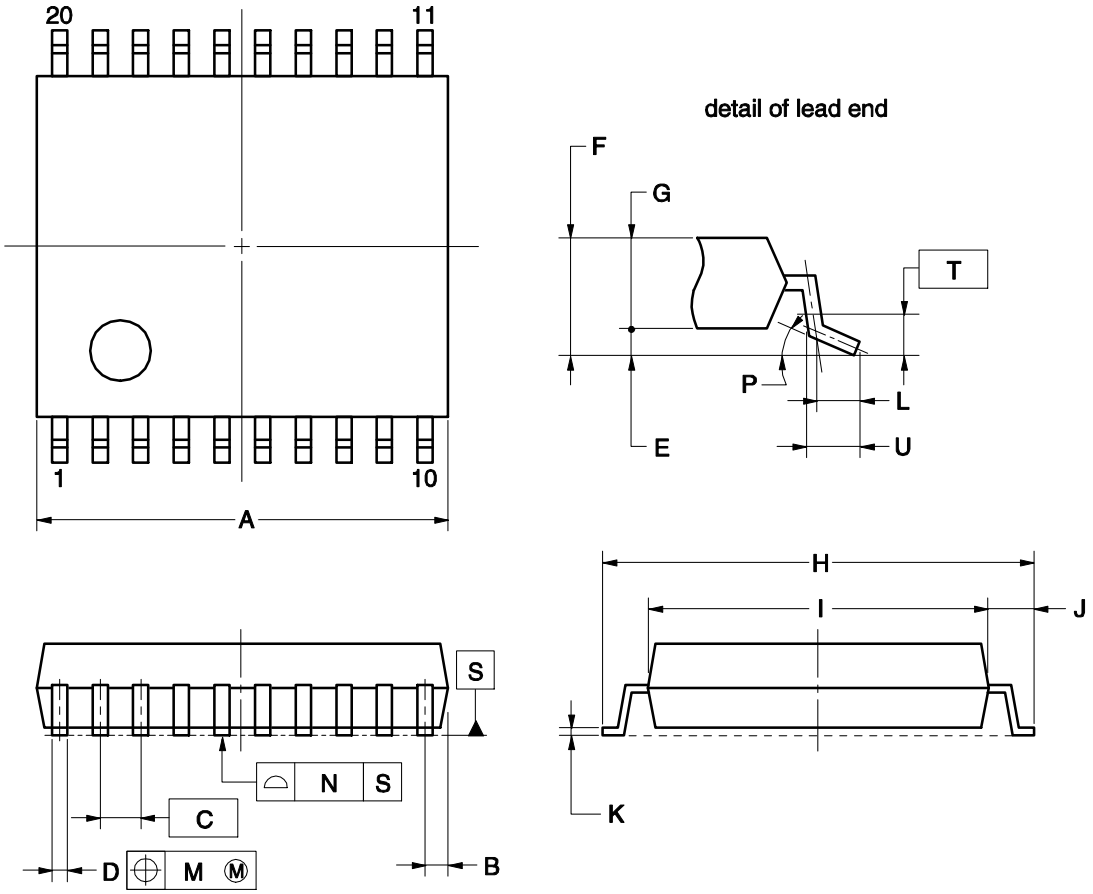
(Correct) Corrected typo.

Remark $V_{LVI(n-1)}$ > V_{LVIn}: n = 1 to 5

No.31: 33.1 20-pin products (LSSOP)

(Incorrect)

20-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

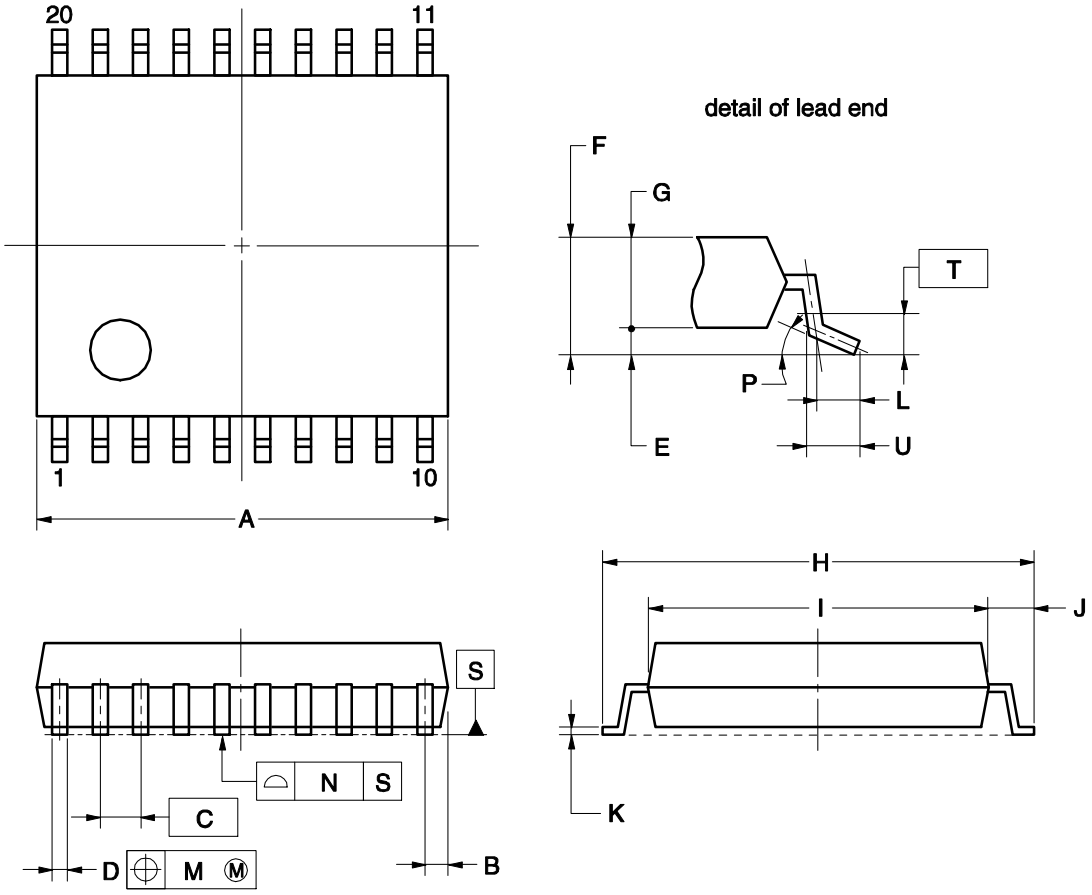
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.15
B	0.475 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3°^{+5°}_{-3°}$
T	0.25
U	0.6±0.15

S20MC-65-5A4-2

(Correct) Added each code data to the package diagram.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12



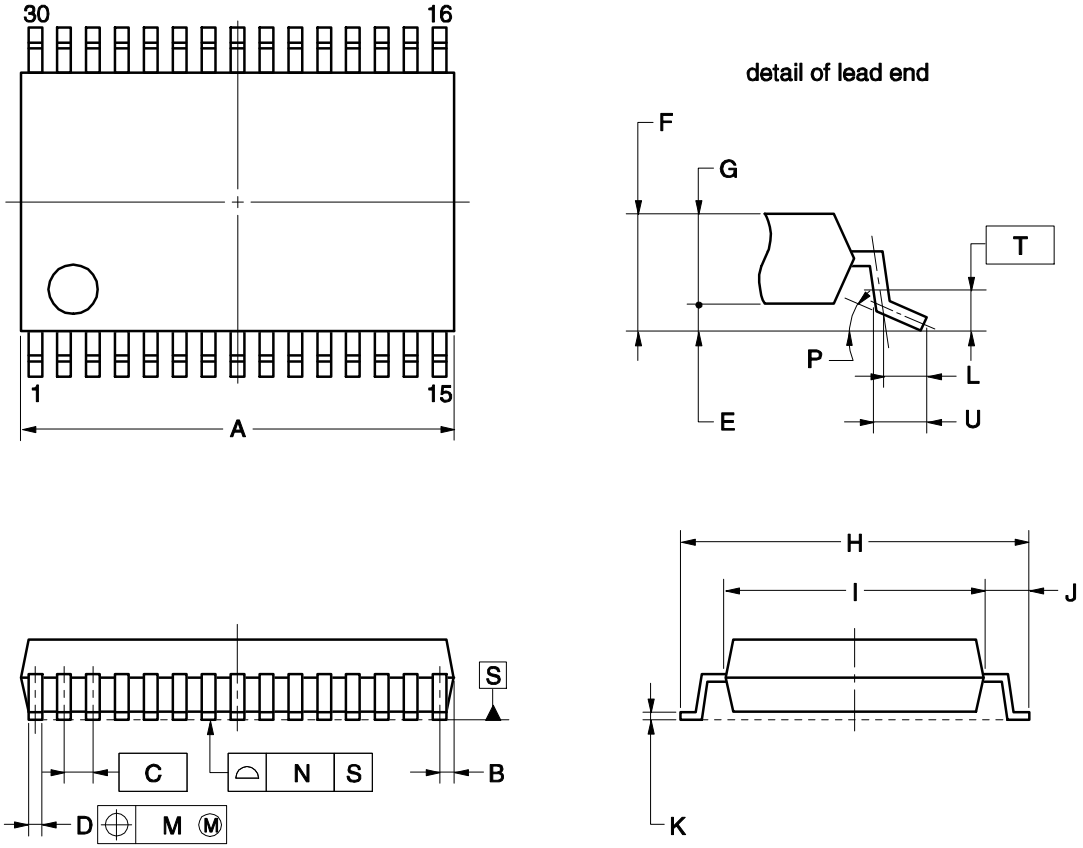
NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.15
B	0.475 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3°^{+5°}_{-3°}$
T	0.25
U	0.6±0.15

No.32: 33.2 30-pin products (LSSOP)

(Incorrect)

30-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

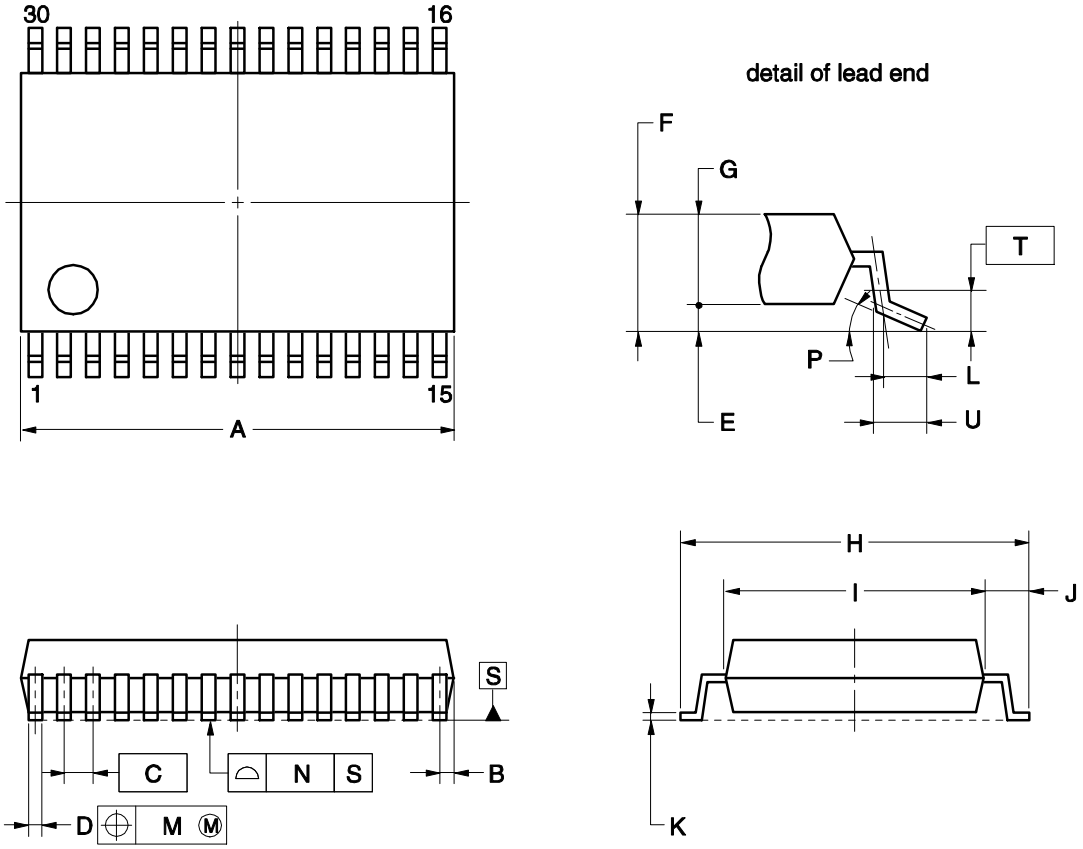
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3°^{+5°}_{-3°}$
T	0.25
U	0.6±0.15

S30MC-65-5A4-2

(Correct) Added each code data to the package diagram.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



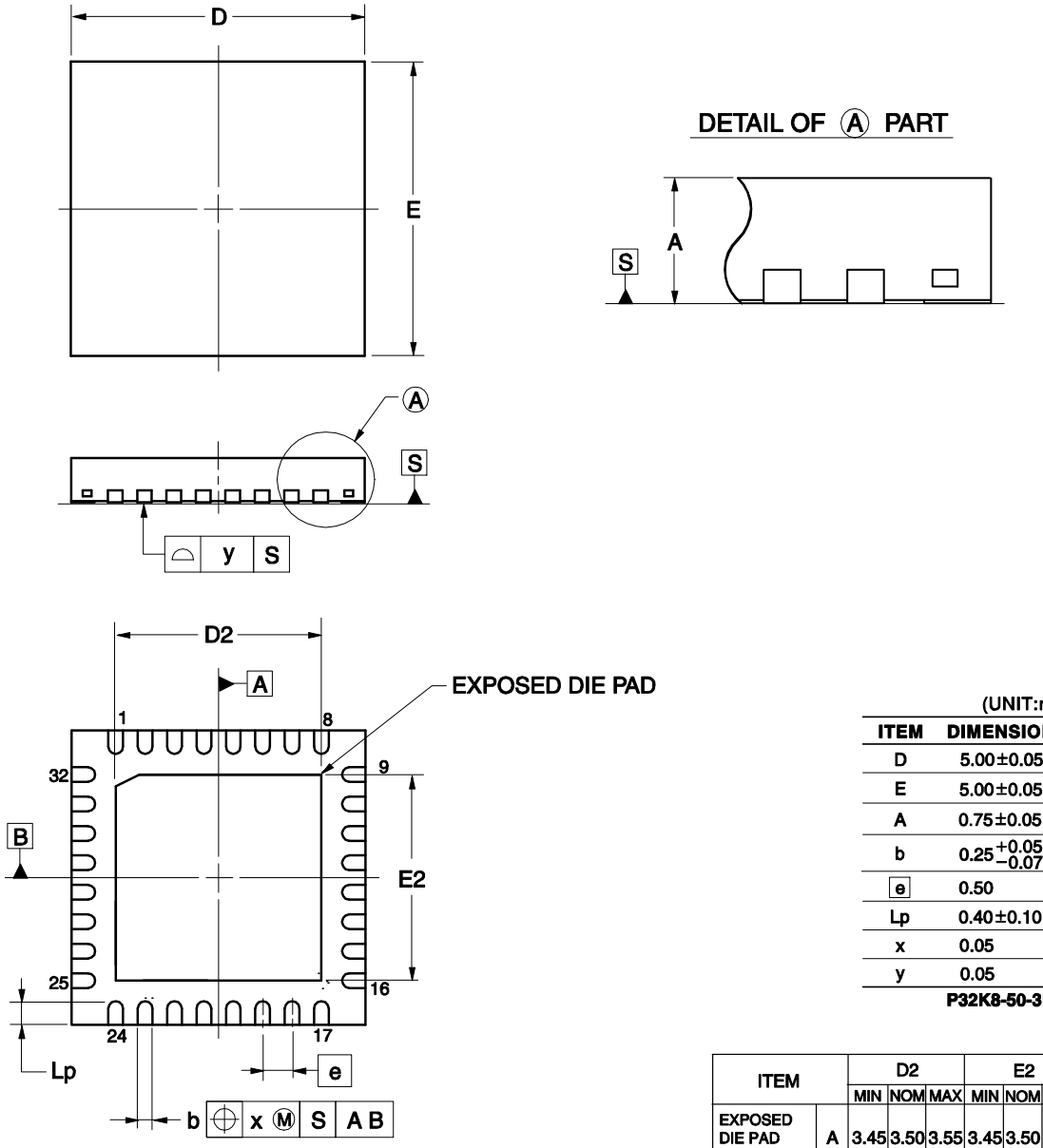
NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3°^{+5°}_{-3°}$
T	0.25
U	0.6±0.15

No.33: 33.3 32-pin products (HWQFN [1])

(Incorrect)

32-PIN PLASTIC WQFN(5x5)



(UNIT:mm)

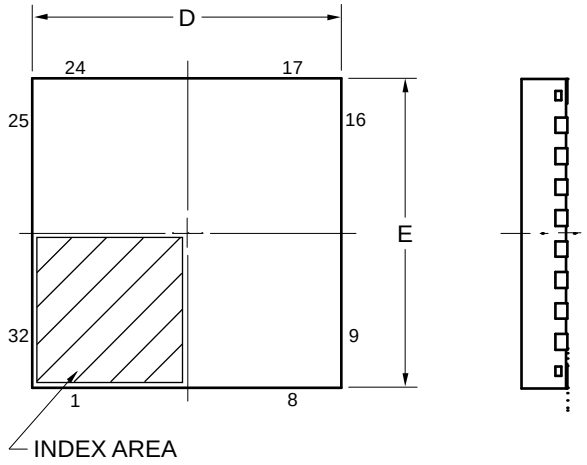
ITEM	DIMENSIONS
D	5.00±0.05
E	5.00±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

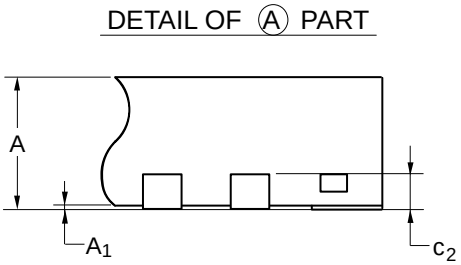
P32K8-50-3B4-2

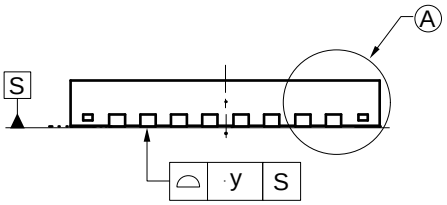
ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	3.45	3.50	3.55	3.45	3.50	3.55

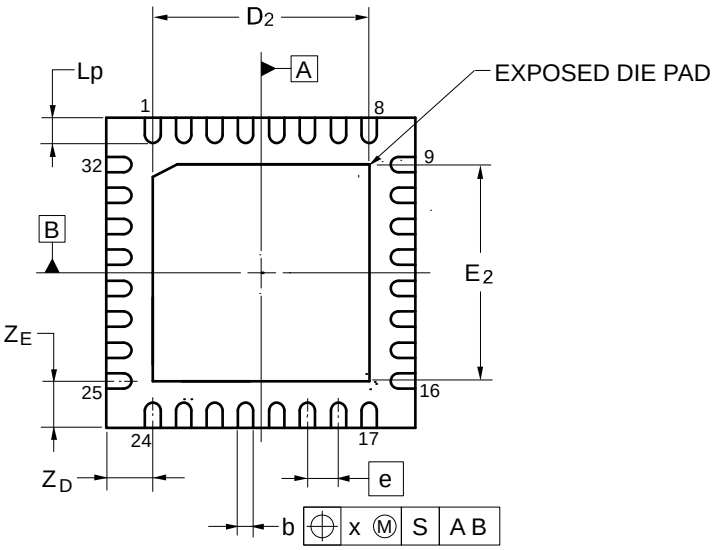
(Correct) Added each code data to the diagram and corrected the description in the parameter table.

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06







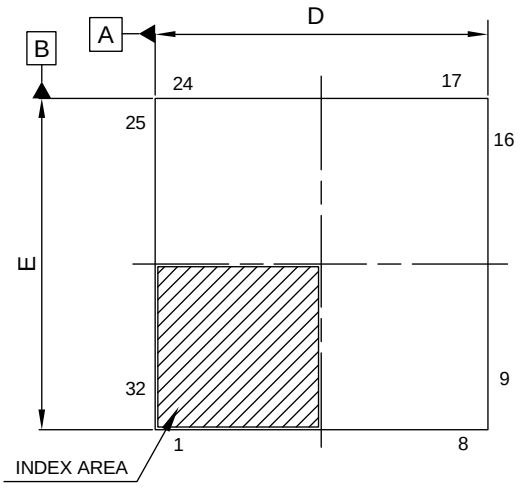


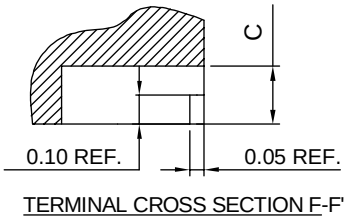
Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	3.50	—
E_2	—	3.50	—

No.34: 33.3 32-pin products (HWQFN [2])

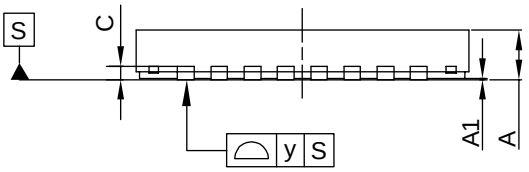
(Correct) Added the 32-pin product package data.

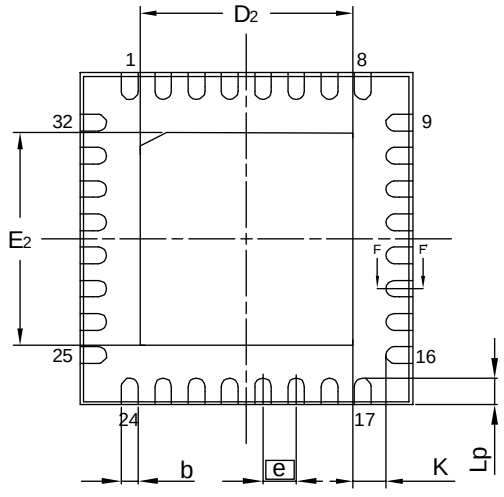
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KH-A	0.06





TERMINAL CROSS SECTION F-F'



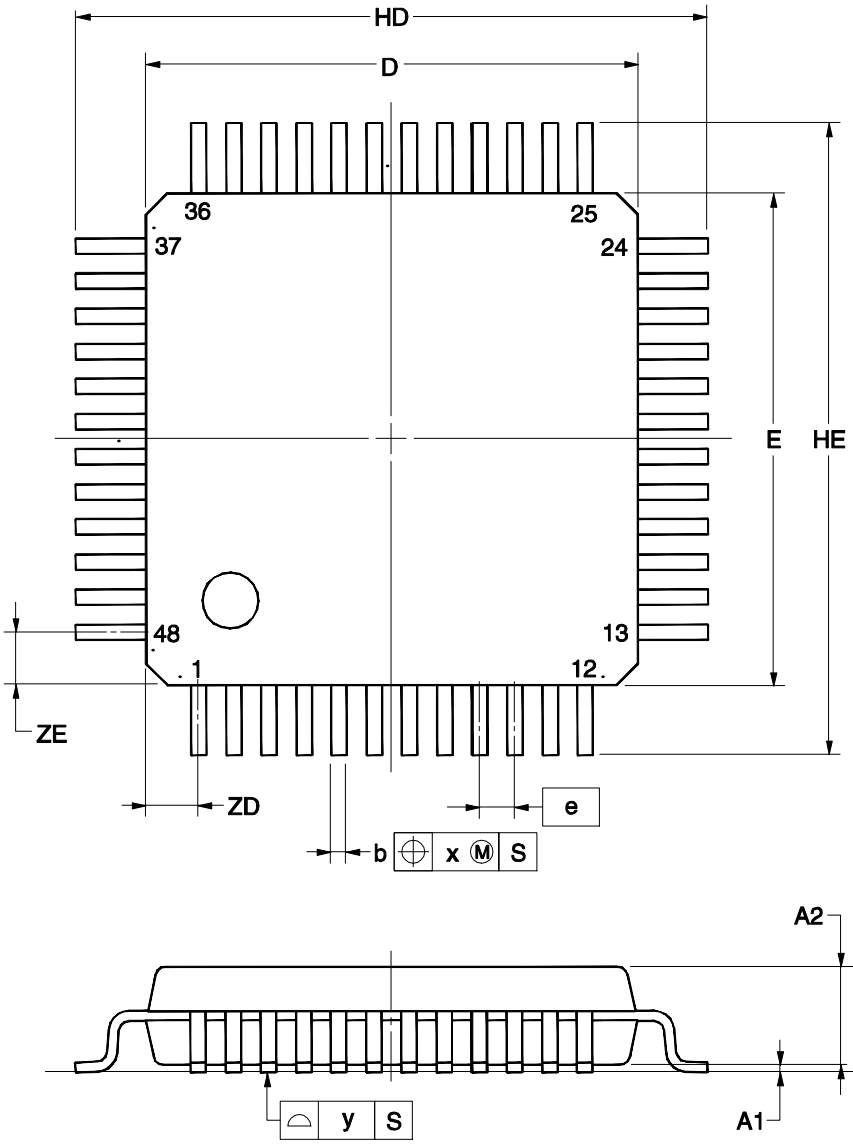


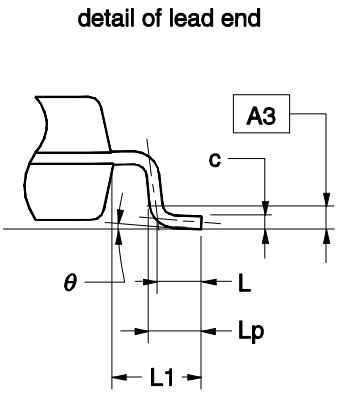
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	4.85	5.00	5.15
E	4.85	5.00	5.15
A	—	—	0.80
A_1	0.00	—	0.05
b	0.18	0.25	0.30
e		0.50 BSC	
Lp	0.35	0.40	0.45
y	—	—	0.08
c	—	0.20	—
K	0.20	—	—
D_2	—	3.20	—
E_2	—	3.20	—

No.35: 33.4 48-pin products (LFQFP)

(Incorrect)

48-PIN PLASTIC LQFP (FINE PITCH)(7x7)





(UNIT:mm)

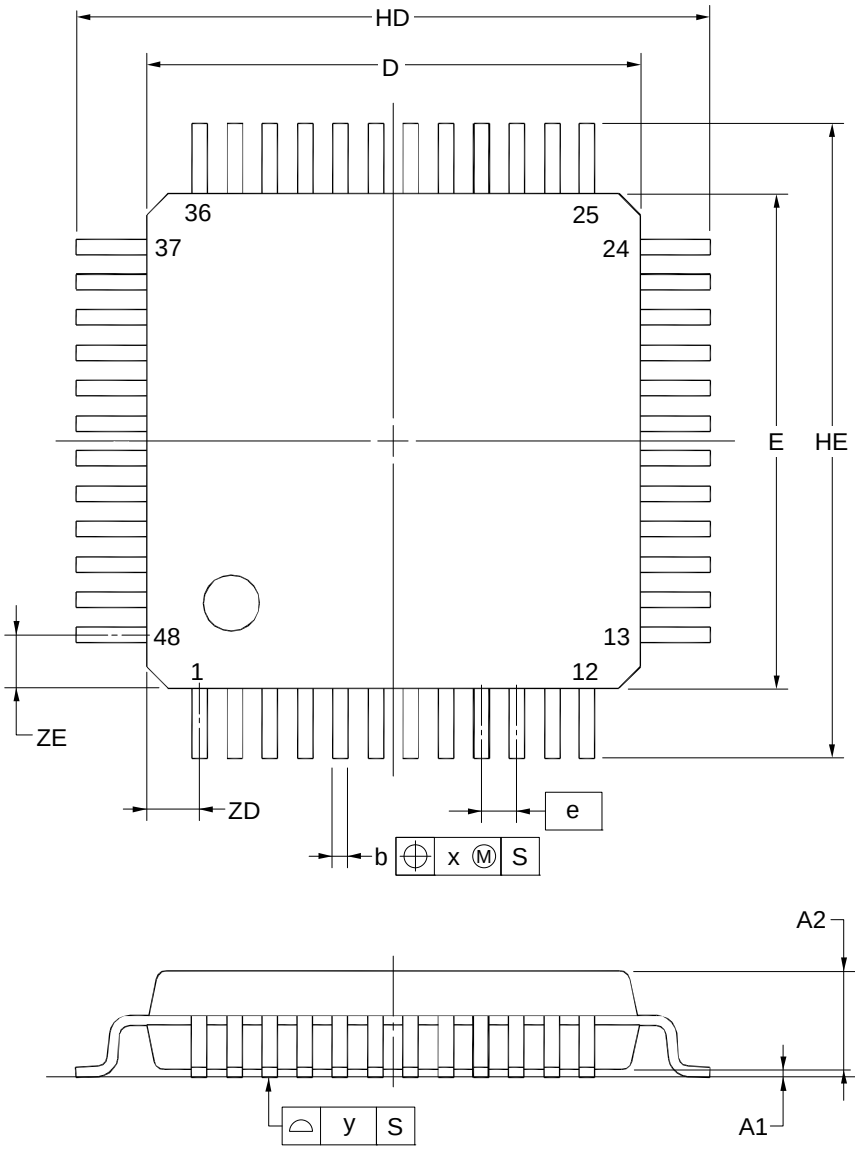
ITEM	DIMENSIONS
D	7.00±0.20•
E	7.00±0.20•
HD	9.00±0.20•
HE	9.00±0.20•
A	1.60 MAX.•
A1	0.10±0.05•
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08•
y	0.08•
ZD	0.75•
ZE	0.75

P48GA-50-8EU

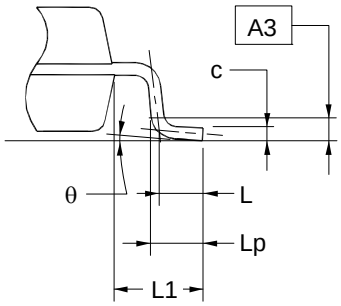
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

(Correct) Added each code data to the package diagram.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



detail of lead end



(UNIT:mm)

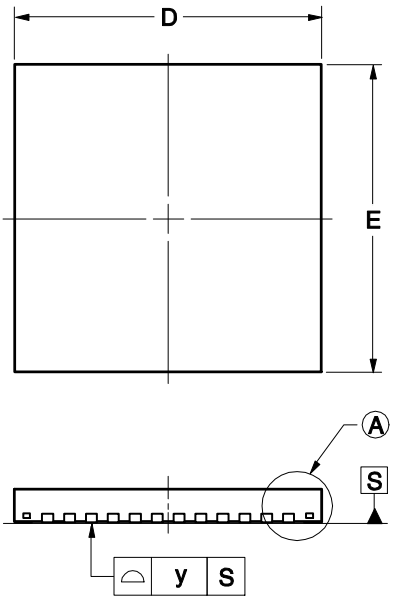
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

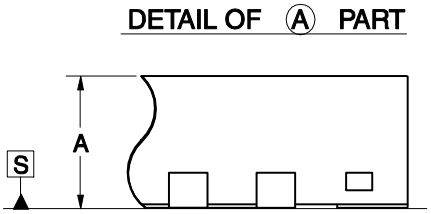
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

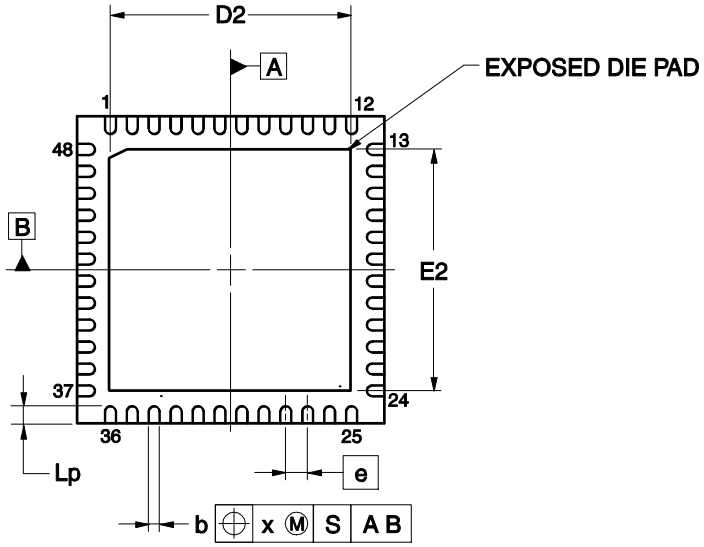
No.36: 33.4 48-pin products (HWQFN)

(Incorrect)

48-PIN PLASTIC WQFN(7x7)







(UNIT:mm)

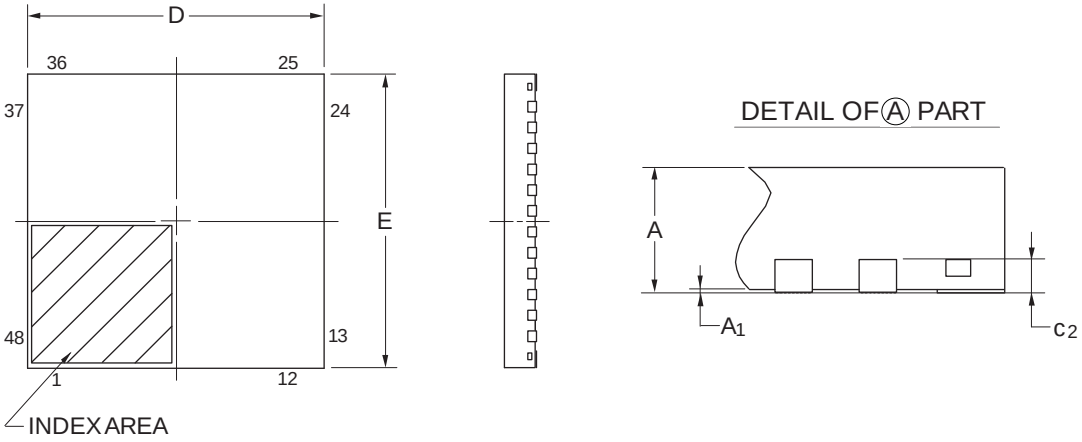
ITEM	DIMENSIONS
D	7.00±0.05
E	7.00±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

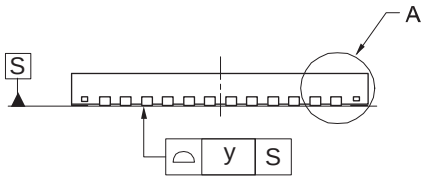
P48K8-50-5B4-3

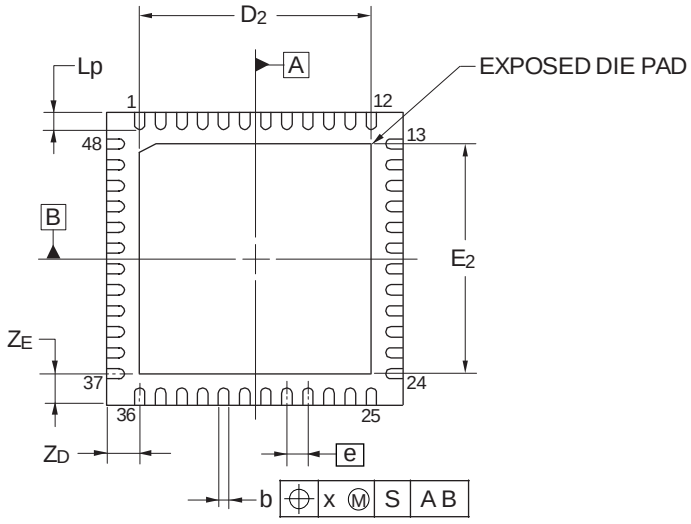
ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

(Correct) Added each code data to the diagram and corrected the description in the parameter table.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-7	0.13





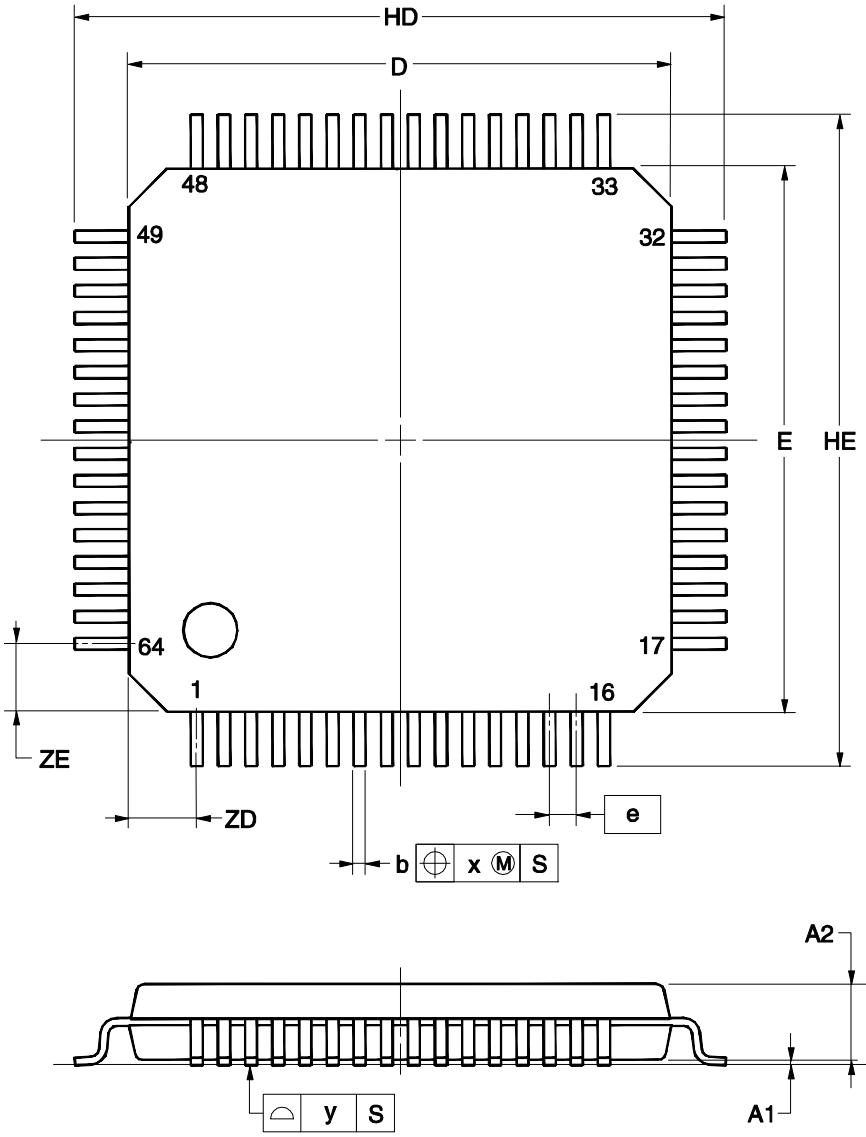


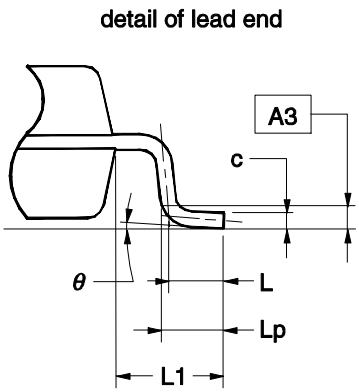
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2		5.50	—

No.37: 33.5 64-pin products

(Incorrect)

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)





(UNIT:mm)

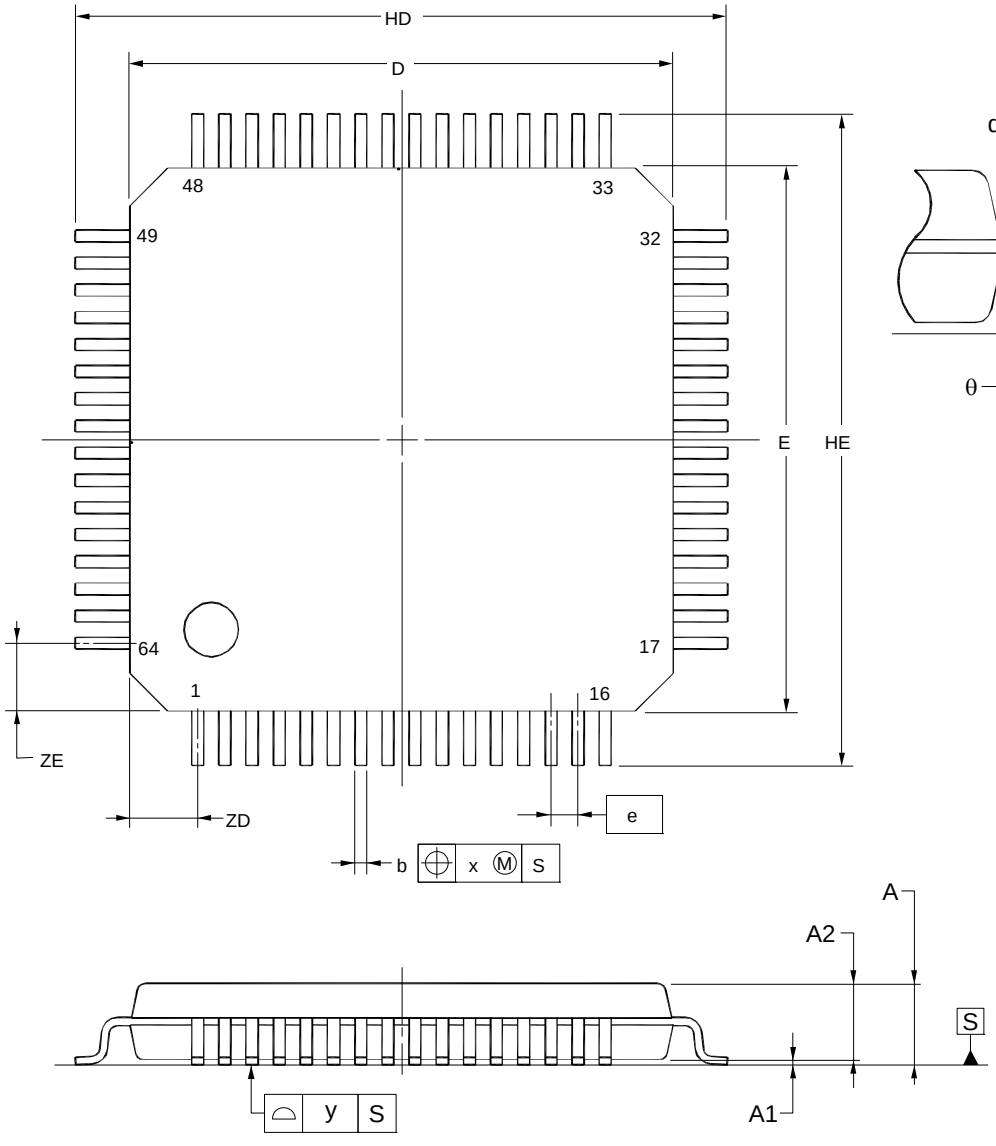
ITEM	DIMENSIONS
D	10.00±0.20•
E	10.00±0.20•
HD	12.00±0.20•
HE	12.00±0.20•
A	1.60 MAX.•
A1	0.10±0.05•
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08•
y	0.08•
ZD	1.25•
ZE	1.25

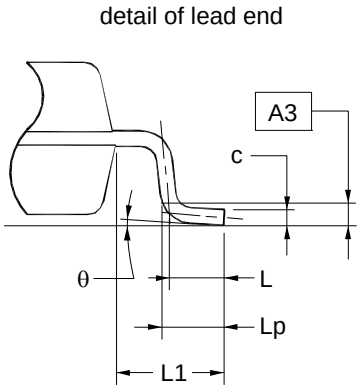
P64GB-50-UEU-1

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

(Correct) Added each code data to the package diagram.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU	0.35





(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.