To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
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Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

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Customer Support Dept.
April 1, 2003

HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	9th, March, 1998	No.	TN-PSC-332A/E
THEME	The correction of HD64572 SCA-II User's Manual.		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents	☐ Limitation on Use ■ Correction	
PRODUCT NAME	HD64572FL33 , HD64572AFL33	Lot No.etc.	All lots
REFERENCE DOCUMENTS	———	Effective Date	forever
		From	Now

There are some misprint in HD64572 SCA-II User's Manual,please make correct it described as below.

1. Section 1 Overview

1.5 Protocol Support

1.5.1 Asynchronous Mode ··· page 10

(Current)

Item	Description
Stop bits	1,1.5, or 2

(Corrected)

Item	Description
Stop bits	1 or 2

1.7.2 Transmission Formats ··· page 25

(Current)

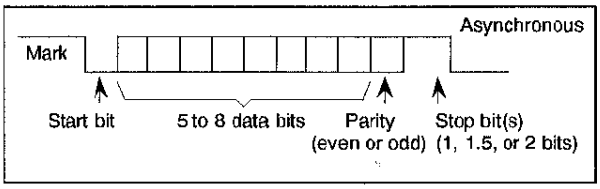


Figure1-8 Examples of Transmission Formats

(Corrected)

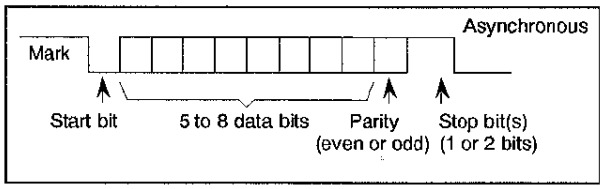


Figure1-8 Examples of Transmission Formats

2. Section 5 Multiprotocol Serial Communication Interface(MSCI)

5.1 Overview

5.1.1 Features and Functions ··· page 152

・Asynchronous mode

(Current)

-Selectable stop bit length(1,1.5,or 2 bits)

(Corrected)

-Selectable stop bit length(1 or 2 bits)

5.2 Registers

5.2.1 MSCI Mode Register 0(MD0) ··· page156

Bit	7	6	5	4	3	2	1	0
Asynchronous	PRTCL2	PRTCL1	PRTCL0	AUTO	-*1	-*1	STOP1	STOP0
Byte synchronous					CRCC1	CRCC0	CRC1	CRC0
Bit synchronous								
Transparent				-*1	-*1	-*1	-*1	-*1
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(Current)

Stop bit length(asynchronous mode)

0	0	1 bit
1	0	1.5 bits
0	1	2 bits
1	1	Reserved*2

(Corrected)

Stop bit length(asynchronous mode)

0	0	1 bit
0	1	Reserved*2
1	0	2 bits
1	1	Reserved*2

Bits 1 and 0 - Stop Bit Length (STOP1 , STOP0) ··· page159

• Asynchronous mode

(Current)

STOP1	STOP0	Description
0	0	Stop bit length = 1
	1	Stop bit length = 1.5
1	0	Stop bit length = 2
	1	Reserved

(Corrected)

STOP1	STOP0	Description
0	0	Stop bit length = 1
	1	Reserved
1	0	Stop bit length = 2
	1	Reserved

5.3 Operation ··· page 271

5.3.1 Asynchronous Mode

(Current)

The data transmission ends with 1, 1.5, or 2 stop bits.

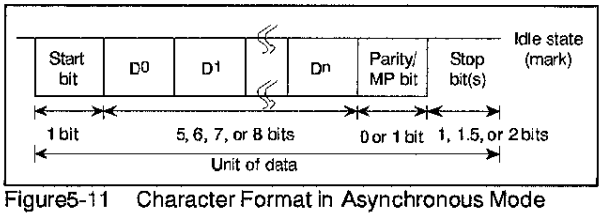


Figure5-11 Character Format in Asynchronous Mode

(Corrected)

The data transmission ends with 1 or 2 stop bits.

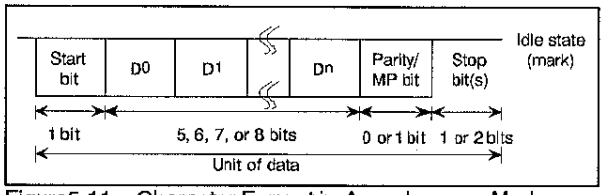


Figure5-11 Character Format in Asynchronous Mode

Transmission Operation ··· page 274 , 275

(Current)

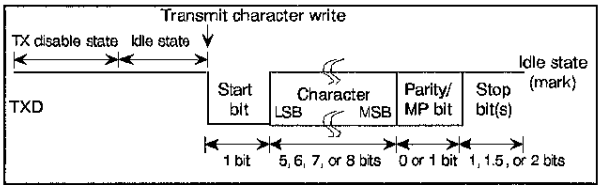


Figure5-14 State Transition Diagram for Transmission in Asynchronous Mode

(Corrected)

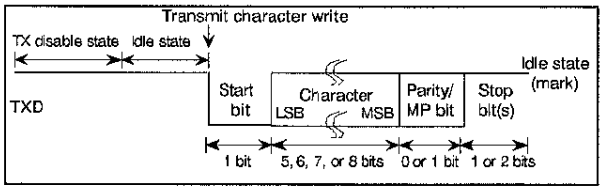


Figure5-14 State Transition Diagram for Transmission in Asynchronous Mode

A stop bit length of 1, 1.5, or 2 can be specified in 1/16, 1/32, or 1/64 clock mode. In 1/1 clock mode, only a stop bit length of 1 or 2 is available; if 1.5 is specified, 2 stop bits will be used.

A stop bit length of 1 or 2 can be specified in 1/16, 1/32, or 1/64 clock mode.

Error Checking ··· page 283

- Framing error

(Current)

A space detected where a stop bit should be causes a framing error. Even if the stop bit length is 1.5 or 2 bits, only the first bit is checked.

(Corrected)

A space detected where a stop bit should be causes a framing error. Even if the stop bit length is 2 bits, only the first bit is checked.

3. Section9 Electrical Characterics

9.3 AC Characteristics

9.3.1 Bus Timing

Table9-3 Slave Mode Bus Timing CPU Modes 0 and 1

(Current)

No.	Item	Symbol	Min	Typ	Max	Unit
6	$\overline{RD}$ active hold time	t_{RDH}	1	-	-	ns
7	$\overline{RD}$ inactive set-up time	t_{RDS2}	12	-	-	ns
9	$\overline{DS}$ hold time	t_{DSH}	1	-	-	ns
10	WAIT low delay time	t_{WTD1}	-	-	20	ns
11	WAIT active delay time	t_{WTD2}	-	-	20	ns
13	Read data valid delay time	t_{DBD1}	-	-	20	ns
14	Read data invalid delay time	t_{DBD2}	-	-	20	ns
17	$\overline{WR}$ active hold time	t_{WRH}	0	-	-	ns
18	$\overline{WR}$ inactive set-up time	t_{WRS2}	10	-	-	ns

(Corrected)

No.	Item	Symbol	Min	Typ	Max	Unit
6	$\overline{RD}$ active hold time	t_{RDH}	2	-	-	ns
7	$\overline{RD}$ inactive set-up time	t_{RDS2}	13	-	-	ns
9	$\overline{DS}$ hold time	t_{DSH}	2	-	-	ns
10	WAIT active delay time	t_{WTD1}	-	-	20	ns
11	WAIT inactive delay time	t_{WTD2}	-	-	20	ns
13	Read data valid delay time	t_{DBD1}	-	-	22	ns
14	Read data invalid delay time	t_{DBD2}	-	-	24	ns
17	$\overline{WR}$ active hold time	t_{WRH}	2	-	-	ns
18	$\overline{WR}$ inactive set-up time	t_{WRS2}	13	-	-	ns

Table9-4 Slave Mode Bus Timing CPU Modes 2 and 3

(Current)

No.	Item	Symbol	Min	Typ	Max	Unit
26	R/$\overline{W}$ active hold time	t_{RWH}	1	-	-	ns
29	$\overline{DS}$ inactive set-up time	t_{DSS2}	14	-	-	ns
30	WAIT High delay time	t_{WTD1}	-	-	20	ns
31	WAIT active delay time	t_{WTD2}	-	-	20	ns
33	Read data valid delay time	t_{DBD1}	-	-	20	ns
34	Read data invalid delay time	t_{DBD2}	-	-	20	ns

(Corrected)

No.	Item	Symbol	Min	Typ	Max	Unit
26	R/$\overline{W}$ active hold time	t_{RWH}	2	-	-	ns
29	$\overline{DS}$ inactive set-up time	t_{DSS2}	16	-	-	ns
30	WAIT active delay time	t_{WTD1}	-	-	20	ns
31	WAIT inactive delay time	t_{WTD2}	-	-	20	ns
33	Read data valid delay time	t_{DBD1}	-	-	22	ns
34	Read data invalid delay time	t_{DBD2}	-	-	24	ns

Table9-7 Interrupt Timing in CPU Modes 0 and 1 ··· page478

(Current)

No.	Item	Symbol	Min	Typ	Max	Unit
107	Vecter data valid delay time	t_{IDBD1}	-	-	20	ns

(Corrected)

No.	Item	Symbol	Min	Typ	Max	Unit
107	Vecter data valid delay time	t_{IDBD1}	-	-	22	ns

Table9-8 Interrupt Timing in CPU Modes 2 and 3 ··· page478

(Current)

No.	Item	Symbol	Min	Typ	Max	Unit
117	Vecter data valid delay time	t_{IDBD1}	-	-	20	ns

Test Conditions : Figure9-10, Figure9-11

(Corrected)

No.	Item	Symbol	Min	Typ	Max	Unit
117	Vecter data valid delay time	t_{IDBD1}	-	-	22	ns

Test Conditions : Figure9-11

Table9-9 Bus Arbitration Timing in CPU Modes 0 and 1 ··· page479

(Current)

No.	Item	Symbol	Min	Typ	Max	Unit
208	Address output delay time	t_{AD}	-	-	20	ns

(Corrected)

No.	Item	Symbol	Min	Typ	Max	Unit
208	Address output delay time	t_{AD}	-	-	22	ns

Table9-10 Bus Arbitration Timing in CPU Modes 2 and 3 ··· page480

(Current)

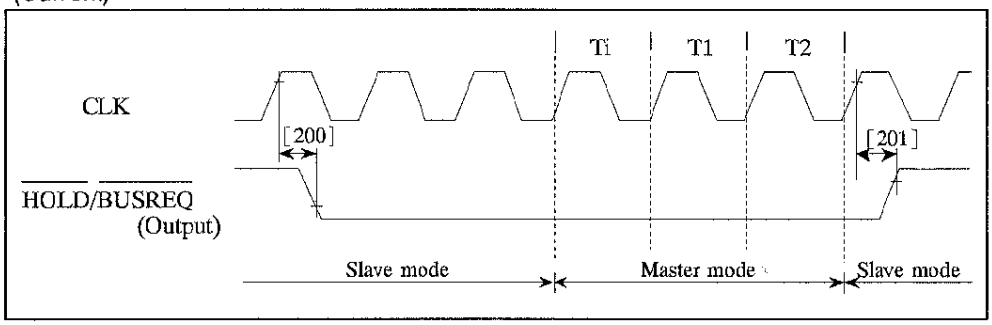
No.	Item	Symbol	Min	Typ	Max	Unit
226	Address output delay time	t_{AD}	-	-	20	ns

(Corrected)

No.	Item	Symbol	Min	Typ	Max	Unit
226	Address output delay time	t_{AD}	-	-	22	ns

Figure9-12 Bus Arbitration Timing (CPU Modes 0 , 1) ··· page 493

(Current)



(Corrected)

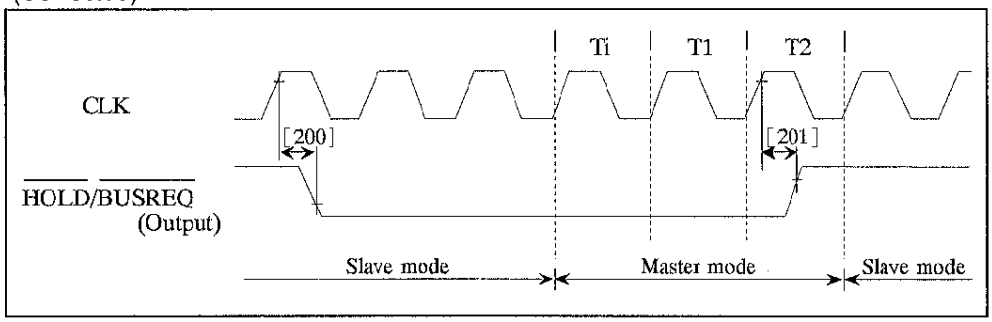
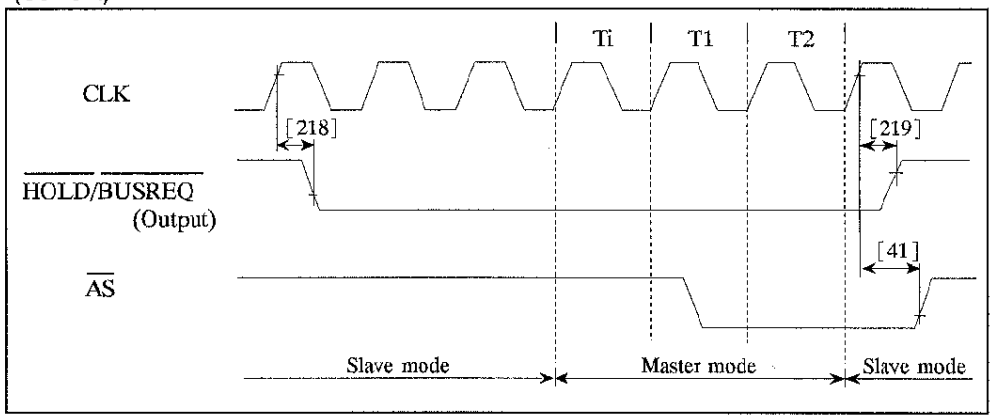


Figure9-13 Bus Arbitration Timing (CPU Modes 2 , 3) ··· page 494

(Current)



(Corrected)