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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0125A/E	Rev.	1.00
Title	Correction of GPT		Information Category	Technical Notification		
Applicable Product	Each Group of RA4E1, RA4E2, RA4M2, RA4M3, RA4T1, RA6E1, RA6E2, RA6M4, RA6M5, RA6T2, RA6T3, RA8D1, RA8E1, RA8M1, RA8T1, RA8E2	Lot No. All	Reference Document	Refer the table 1		

Table 1 Reference Document List

No	Reference Document Name	Rev	Document Control Number
1	RA4E1 Group User's Manual Hardware	1.20	R01UH0929EJ0120
2	RA4E2 Group User's Manual Hardware	1.30	R01UH0996EJ0130
3	RA4M2 Group User's Manual Hardware	1.30	R01UH0892EJ0130
4	RA4M3 Group User's Manual Hardware	1.40	R01UH0893EJ0140
5	RA4T1 Group User's Manual Hardware	1.20	R01UH0999EJ0120
6	RA6E1 Group User's Manual Hardware	1.20	R01UH0930EJ0120
7	RA6E2 Group User's Manual Hardware	1.30	R01UH0988EJ0130
8	RA6M4 Group User's Manual Hardware	1.40	R01UH0890EJ0140
9	RA6M5 Group User's Manual Hardware	1.30	R01UH0891EJ0130
10	RA6T2 Group User's Manual Hardware	1.40	R01UH0951EJ0140
11	RA6T3 Group User's Manual Hardware	1.20	R01UH0998EJ0120
12	RA8D1 Group User's Manual Hardware	1.10	R01UH0995EJ0110
13	RA8E1 Group User's Manual Hardware	1.00	R01UH1129EJ0100
14	RA8M1 Group User's Manual Hardware	1.10	R01UH0994EJ0110
15	RA8T1 Group User's Manual Hardware	1.10	R01UH1016EJ0110
16	RA8E2 Group User's Manual Hardware	1.00	R01UH1130EJ0100

1. The changes to the RA4E1 microcontroller group are as follows.

1.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 470

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD[2:0] bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), set the MD[2:0] bits to the initial value (000b).

1.2 21.3.4 Automatic Dead Time Setting Function

＜Current description＞ page 516

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 1, 2, 4, 5, m = A, B). The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated.

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20.

The adjusted value for the negative waveform is set for GTCCRB automatically.

The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

＜Changed description＞

Dead time for the changing point of a negative waveform is set in the GTDVU register.

Values for automatic dead time setting can be read from GTCCRB. Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited.

~~In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 1, 2, 4, 5, m = A, B).~~

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20. The adjusted value for the negative waveform is set for GTCCRB automatically. The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

In saw-wave one-shot pulse mode, if the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.

The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated. In triangle-wave mode, it also can be done at the next count clock from the current crest.

2. The changes to the RA4E2 microcontroller group are as follows.

2.1 20.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 482

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with the MD[2] bit set to 0, and counting in triangle-wave mode is performed with the MD[2] bit set to 1.

The MD[2:0] bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD[2:0] bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with the MD[2] bit set to 0, and counting in triangle-wave mode is performed with the MD[2] bit set to 1.

The MD[2:0] bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD[2:0] bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, upcounting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD[2:0] bits to the initial value (000b).

3. The changes to the RA4M2 microcontroller group are as follows.

3.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 489

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD[2:0] bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), set the MD[2:0] bits to the initial value (000b).

3.2 21.3.4 Automatic Dead Time Setting Function

＜Current description＞ page 538

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 0 to 7, m = A, B). The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated.

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20.

The adjusted value for the negative waveform is set for GTCCRB automatically.

The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

＜Changed description＞

Dead time for the changing point of a negative waveform is set in the GTDVU register.

Values for automatic dead time setting can be read from GTCCRB. Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited.

~~In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 0 to 7, m = A, B).~~

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20. The adjusted value for the negative waveform is set for GTCCRB automatically. The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

In saw-wave one-shot pulse mode, if the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.

The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated. In triangle-wave mode, it also can be done at the next count clock from the current crest.

4. The changes to the RA4M3 microcontroller group are as follows.

4.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 505

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD[2:0] bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), set the MD[2:0] bits to the initial value (000b).

4.2 21.3.4 Automatic Dead Time Setting Function

＜Current description＞ page 554

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 0 to 7, m = A, B). The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated.

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20.

The adjusted value for the negative waveform is set for GTCCRB automatically.

The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

＜Changed description＞

Dead time for the changing point of a negative waveform is set in the GTDVU register.

Values for automatic dead time setting can be read from GTCCRB. Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited.

~~In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 0 to 7, m = A, B).~~

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20. The adjusted value for the negative waveform is set for GTCCRB automatically. The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

In saw-wave one-shot pulse mode, if the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.

The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated. In triangle-wave mode, it also can be done at the next count clock from the current crest.

5. The changes to the RA4T1 microcontroller group are as follows.

5.1 20.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 473

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with the MD[2] bit set to 0, and counting in triangle-wave mode is performed with the MD[2] bit set to 1.

The MD[2:0] bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD[2:0] bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with the MD[2] bit set to 0, and counting in triangle-wave mode is performed with the MD[2] bit set to 1.

The MD[2:0] bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD[2:0] bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, upcounting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD[2:0] bits to the initial value (000b).

6. The changes to the RA6E1 microcontroller group are as follows.

6.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 503

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD[2:0] bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), set the MD[2:0] bits to the initial value (000b).

6.2 21.3.4 Automatic Dead Time Setting Function

＜Current description＞ page 549

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 1, 2, 4 to 7, m = A, B). The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated.

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20.

The adjusted value for the negative waveform is set for GTCCRB automatically.

The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

＜Changed description＞

Dead time for the changing point of a negative waveform is set in the GTDVU register.

Values for automatic dead time setting can be read from GTCCRB. Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited.

~~In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 1, 2, 4 to 7, m = A, B).~~

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20. The adjusted value for the negative waveform is set for GTCCRB automatically. The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

In saw-wave one-shot pulse mode, if the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.

The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated. In triangle-wave mode, it also can be done at the next count clock from the current crest.

7. The changes to the RA6E2 microcontroller group are as follows.

7.1 20.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 490

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with the MD[2] bit set to 0, and counting in triangle-wave mode is performed with the MD[2] bit set to 1.

The MD[2:0] bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD[2:0] bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with the MD[2] bit set to 0, and counting in triangle-wave mode is performed with the MD[2] bit set to 1.

The MD[2:0] bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD[2:0] bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, upcounting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD[2:0] bits to the initial value (000b).

8. The changes to the RA6M4 microcontroller group are as follows.

8.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 569

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD[2:0] bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), set the MD[2:0] bits to the initial value (000b).

8.2 21.3.4 Automatic Dead Time Setting Function

＜Current description＞ page 618

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 0 to 9, m = A, B). The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated.

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20.

The adjusted value for the negative waveform is set for GTCCRB automatically.

The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

＜Changed description＞

Dead time for the changing point of a negative waveform is set in the GTDVU register.

Values for automatic dead time setting can be read from GTCCRB. Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited.

~~In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 0 to 9, m = A, B).~~

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20. The adjusted value for the negative waveform is set for GTCCRB automatically. The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

In saw-wave one-shot pulse mode, if the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.

The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated. In triangle-wave mode, it also can be done at the next count clock from the current crest.

9. The changes to the RA6M5 microcontroller group are as follows.

9.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 593

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD[2:0] bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), set the MD[2:0] bits to the initial value (000b).

9.2 21.3.4 Automatic Dead Time Setting Function

＜Current description＞ page 642

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 0 to 9, m = A, B). The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated.

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20.

The adjusted value for the negative waveform is set for GTCCRB automatically.

The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

＜Changed description＞

Dead time for the changing point of a negative waveform is set in the GTDVU register.

Values for automatic dead time setting can be read from GTCCRB. Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited.

~~In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 0 to 9, m = A, B).~~

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20. The adjusted value for the negative waveform is set for GTCCRB automatically. The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

In saw-wave one-shot pulse mode, if the order of the change point becomes inconsistent by adjustment of the waveform change point due to occurrence of dead time errors, or if the change point exceeds the count period even after the adjustment, the complementary relation between the positive- and negative-phases cannot be guaranteed.

The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated. In triangle-wave mode, it also can be done at the next count clock from the current crest.

10. The changes to the RA6T2 microcontroller group are as follows.

10.1 21.2.10 GTICASR : General PWM Timer Input Capture Source Select Register A

＜Current description＞ page 491

Bit	Symbol	Function	R/W
24	ASOC	Other channel Source GTCCRA Input Capture Enable 0: Disables GTCCRA input capture by other channel factor 1: Enables GTCCRA input capture by other channel factor	R/W

＜Changed description＞

Bit	Symbol	Function	R/W
24	ASOC	Other channel Source GTCCRA Input Capture Enable 0: Disables GTCCRA input capture by other channel factors 1: Enables GTCCRA input capture by other channel factors	R/W

10.2 21.2.10 GTICASR : General PWM Timer Input Capture Source Select Register A

＜Current description＞ page 493

ASOC bit (Other channel Source GTCCRA Input Capture Enable)

Select enable or disable for an input capture to the GTCCRA register by other channel factor.

Input capture of other channel factors is not subject to input capture factors to other channels set by the ICAFA and ICBFA bits of the GTICCR register.

＜Changed description＞

ASOC bit (Other channel Source GTCCRA Input Capture Enable)

Select enable or disable for an input capture to the GTCCRA register by other channel factors of inter channel cooperation which is set in the GTICCR register of other channels. Input capture of other channel factors which enabled by this bit is not subject to input capture factors to other channels set by the ICAFA and ICBFA bits of the GTICCR register.

10.3 21.2.11 GTICBSR : General PWM Timer Input Capture Source Select Register B

＜Current description＞ page 495

Bit	Symbol	Function	R/W
24	BSOC	Other channel Source GTCCRB Input Capture Enable 0: Disables GTCCRB input capture by other channel factor 1: Enables GTCCRB input capture by other channel factor	R/W

＜Changed description＞

Bit	Symbol	Function	R/W
24	BSOC	Other channel Source GTCCRB Input Capture Enable 0: Disables GTCCRB input capture by other channel factors 1: Enables GTCCRB input capture by other channel factors	R/W

10.4 21.2.11 GTICBSR : General PWM Timer Input Capture Source Select Register B

＜Current description＞ page 496

BSOC bit (Other channel Source GTCCRB Input Capture Enable)

Select enable or disable for an input capture to the GTCCRB register by other channel factor.

Input capture of other channel factors is not subject to input capture factors to other channels set by the ICAFB and ICBFB bits of the GTICCR register.

＜Changed description＞

BSOC bit (Other channel Source GTCCRB Input Capture Enable)

Select enable or disable for an input capture to the GTCCRB register by other channel factors of inter channel cooperation which is set in the GTICCR register of other channels. Input capture of other channel factors which enabled by this bit is not subject to input capture factors to other channels set by the ICAFB and ICBFB bits of the GTICCR register.

10.5 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 499

MD[3:0] bits (Mode Select)

(omission)

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD bits are ignored, where counting in saw-wave or triangle-wave or complementary PWM modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[3:0] bits (Mode Select)

(omission)

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD bits are ignored, where counting in saw-wave or triangle-wave or complementary PWM modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD bits to the initial value (0000b).

10.6 Table 21.18 GTPR buffer transfer timing in complementary PWM mode

＜Current description＞ page 571

Table 21.18 GTPR buffer transfer timing in complementary PWM mode

	Complementary PWM mode 1	Complementary PWM mode 2	Complementary PWM mode 3, 4
GTPDBR ↓ Temporary register P	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)	After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2)

＜Changed description＞

Table 21.18 GTPR buffer transfer timing in complementary PWM mode

	Complementary PWM mode 1	Complementary PWM mode 2	Complementary PWM mode 3, 4
GTPDBR ↓ Temporary register P	(1) Counting in process After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2) (2) Counting stopped After one GTCLK cycle from GTPDBR register write	(1) Counting in process After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2) (2) Counting stopped After one GTCLK cycle from GTPDBR register write	(1) Counting in process After one GTCLK cycle from GTCCRD register write of slave channel 2 (GPT32n+2) (2) Counting stopped After one GTCLK cycle from GTPDBR register write

10.7 Figure 21.22 Example of GTPR double buffer operation with complementary PWM mode 1

Change the values of the GPT32n.GTPDB register, GPT32n.Temporary register P, GPT32n.GTPB register, and GPT32n.GTPR register in the figure as follows.

0x0000 0300 → 0x0000 3000

0x0000 0500 → 0x0000 5000

0x0000 0700 → 0x0000 7000

0x0000 0900 → 0x0000 9000

0x0000 0B00 → 0x0000 B000

＜Current description＞ page 573

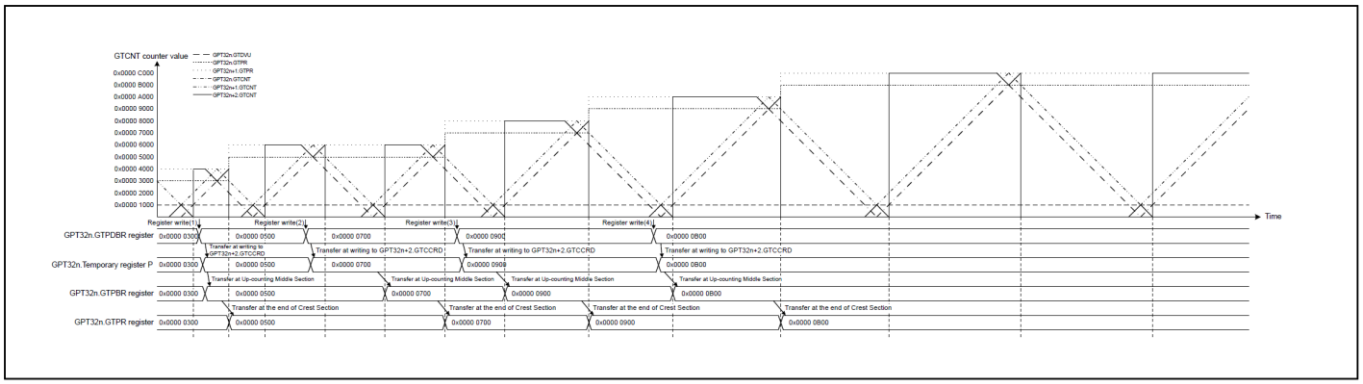

Figure 21.22 Example of GTPR double buffer operation with complementary PWM mode 1

＜Changed description＞

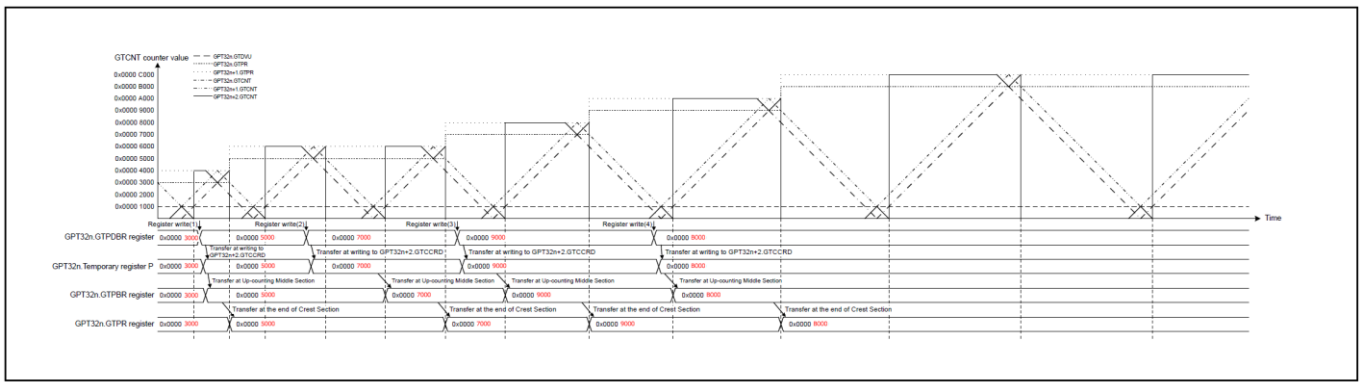

Figure 21.22 Example of GTPR double buffer operation with complementary PWM mode 1

10.8 Figure 21.23 Example of GTPR double buffer operation with complementary PWM mode 2

Change the values of the GPT32n.GTPDB register, GPT32n.Temporary register P, GPT32n.GTPB register, and GPT32n.GTPR register in the figure as follows.

0x0000 0300 → 0x0000 3000

0x0000 0500 → 0x0000 5000

0x0000 0700 → 0x0000 7000

0x0000 0900 → 0x0000 9000

0x0000 0B00 → 0x0000 B000

＜Current description＞ page 573

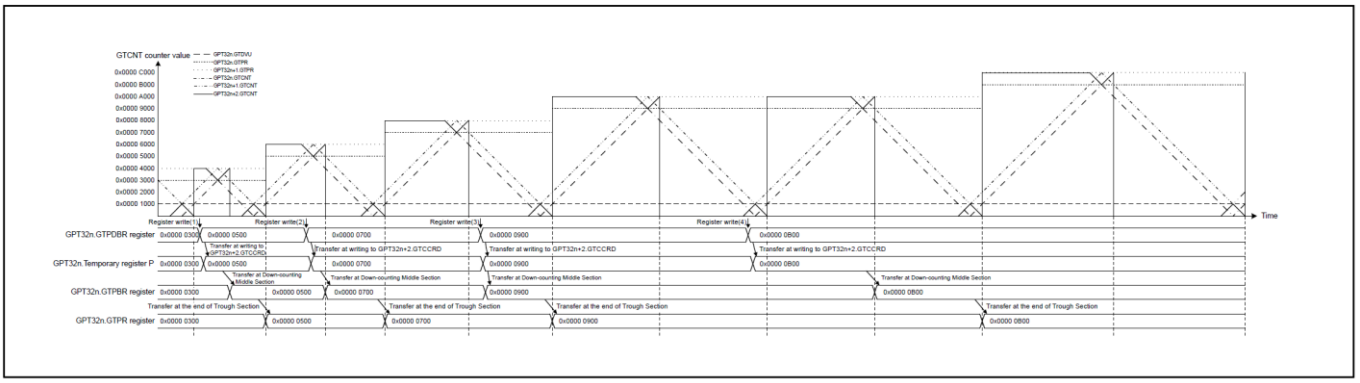

Figure 21.23 Example of GTPR double buffer operation with complementary PWM mode 2

＜Changed description＞

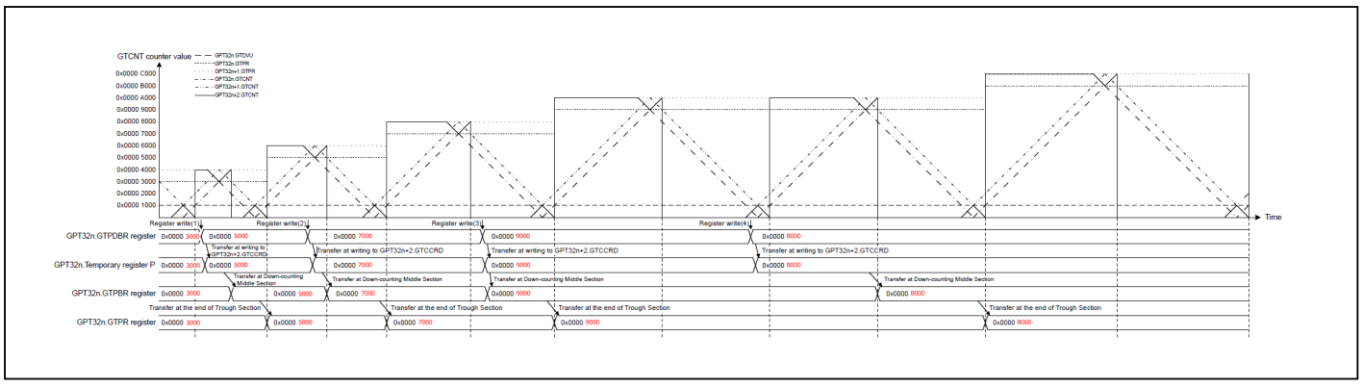

Figure 21.23 Example of GTPR double buffer operation with complementary PWM mode 2

10.9 Figure 21.24 Example of GTPR double buffer operation with complementary PWM mode 3, 4

Change the values of the GPT32n.GTPDB register, GPT32n.Temporary register P, GPT32n.GTPB register, and GPT32n.GTPR register in the figure as follows.

0x0000 0300 → 0x0000 3000

0x0000 0500 → 0x0000 5000

0x0000 0700 → 0x0000 7000

0x0000 0900 → 0x0000 9000

0x0000 0B00 → 0x0000 B000

＜Current description＞ page 574

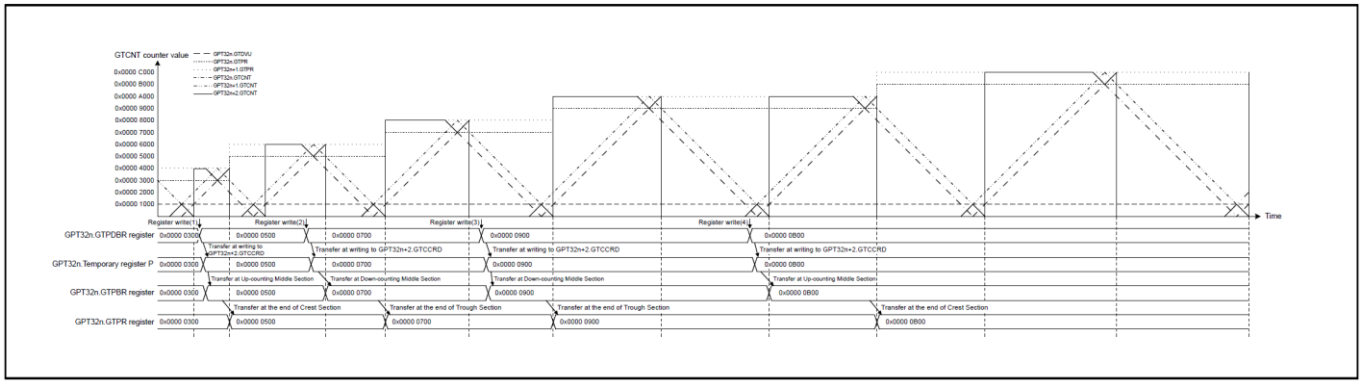

Figure 21.24 Example of GTPR double buffer operation with complementary PWM mode 3, 4

＜Changed description＞

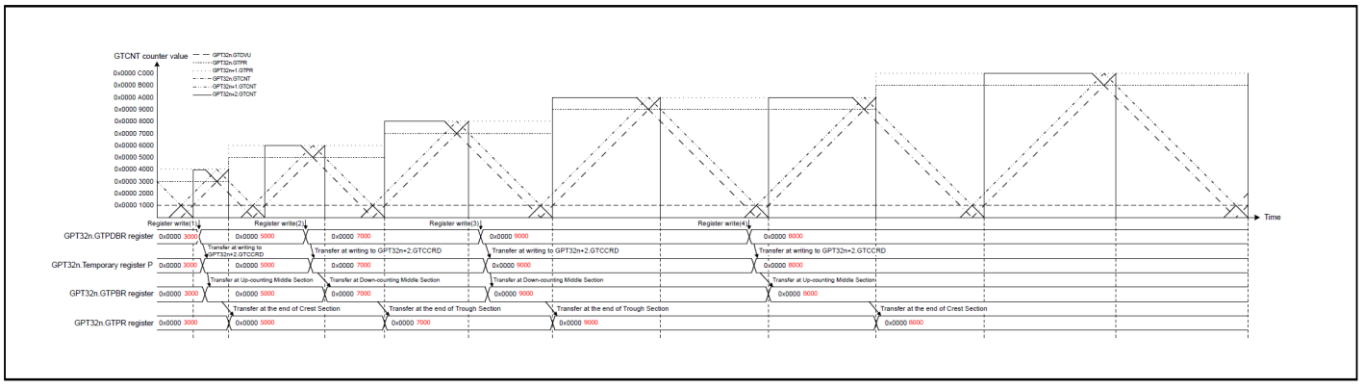

Figure 21.24 Example of GTPR double buffer operation with complementary PWM mode 3, 4

10.10 Table 21.35 Example for Setting Complementary PWM Mode 1,2,3 (1 of 2)

＜Current description＞ page 623

Table 21.35 Example for Setting Complementary PWM Mode 1,2,3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[3:0] bits of GTP32n channel.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of GPT32n channel.
3	Set cycle	Set the cycle in GTPR of GPT32n channel.

＜Changed description＞

Table 21.35 Example for Setting Complementary PWM Mode 1,2,3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[3:0] bits of GTP32n channel.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of GPT32n channel.
3	Set cycle	Set the cycle in GTPR, GTPBR and GTPDBR of GPT32n channel.

10.11 Table 21.40 Example for Setting Complementary PWM Mode 4 (1 of 2)

＜Current description＞ page 638

Table 21.40 Example for Setting Complementary PWM Mode 4 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode (1111b) with GTCR.MD[3:0] of GTP32n channel.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of GPT32n channel.
3	Set cycle	Set the cycle in GTPR of GPT32n channel.
4	Set GTIOCnm /GTIOCn+1m / GTIOCn+2m pin function	Set the function of the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
5	Enable GTIOCnm / GTIOCn+1m /GTIOCn+2m pin output	Set to enable the output from the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with the OAE and OBE bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
6	Set buffer operation	Set buffer operation with the GTBER2.CP3DB bit of the GPT32n, GPT32n+1, and GPT32n+2 channels.
7	Set compare match value	Set the output pin changing point during up-counting after count start in the GTCCRA register of the GPT32n, GPT32n+1, and GPT32n+2 channels.

＜Changed description＞

Table 21.40 Example for Setting Complementary PWM Mode 4 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode (1111b) with GTCR.MD[3:0] of GTP32n channel.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0] bits of GPT32n channel.
3	Set cycle	Set the cycle in GTPR, GTPBR and GTPDBR of GPT32n channel.
4	Set GTIOCnm /GTIOCn+1m /GTIOCn+2m pin function	Set the function of the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with GTIOA[4:0] and GTIOB[4:0] bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
5	Enable GTIOCnm /GTIOCn+1m /GTIOCn+2m pin output	Set to enable the output from the GTIOCnm, GTIOCn+1m, and GTIOCn+2m pins with the OAE and OBE bits in the GTIOR register of the GPT32n, GPT32n+1, and GPT32n+2 channels.
6	Set buffer operation	Set buffer operation with the GTBER2.CP3DB bit of the GPT32n, GPT32n+1, and GPT32n+2 channels.
7	Set compare match value	Set the output pin changing point during up-counting after count start in the GTCCRA register of the GPT32n, GPT32n+1, and GPT32n+2 channels.

10.12 21.10 Usage Notes

＜Current description＞

(There is no description in 21.10 Usage Notes.)

＜Changed description＞

21.10.12. Setting Range of the GTPBR and GTPDBR register in complementary PWM mode (GPT32n (n = 4~9))

In complementary PWM modes 1, 3, and 4, if GTPR buffer transfer occurs at the end of the crest section, set the GTPBR and GTPDBR value to the restricted range(GTPBR≧GTPR-GTDVU, GTPDBR≧GTPR-GTDVU) so that the GTPR value after the buffer transfer is not less than the GTCNT counter value of the master channel at the end of the crest section. When GTPR buffer transfer occurs at the end of the trough section or clearing counter, there is no restriction on the setting range of GTPBR and GTPDBR.

11. The changes to the RA6T3 microcontroller group are as follows.

11.1 20.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 484

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with the MD[2] bit set to 0, and counting in triangle-wave mode is performed with the MD[2] bit set to 1.

The MD[2:0] bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD[2:0] bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with the MD[2] bit set to 0, and counting in triangle-wave mode is performed with the MD[2] bit set to 1.

The MD[2:0] bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD[2:0] bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, upcounting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD[2:0] bits to the initial value (000b).

12. The changes to the RA8D1 microcontroller group are as follows.

12.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 716

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit.The MD bits must be set while the GTCNT operation is stopped.During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD bits must be set while the GTCNT operation is stopped.

During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD[2:0] bits to the initial value (000b).

13. The changes to the RA8E1 microcontroller group are as follows.

13.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 571

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit.The MD bits must be set while the GTCNT operation is stopped.During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD[2:0] bits to the initial value (000b).

14. The changes to the RA8M1 microcontroller group are as follows.

14.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 688

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit.The MD bits must be set while the GTCNT operation is stopped.During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD[2:0] bits to the initial value (000b).

15. The changes to the RA8T1 microcontroller group are as follows.

15.1 20.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 649

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit.The MD bits must be set while the GTCNT operation is stopped.During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD[2:0] bits to the initial value (000b).

16. The changes to the RA8E2 microcontroller group are as follows.

16.1 21.2.12 GTCR : General PWM Timer Control Register

＜Current description＞ page 659

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit.The MD bits must be set while the GTCNT operation is stopped.During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed.

＜Changed description＞

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode.

Only the MD[2] bit is valid at input capture. Counting in saw-wave mode is performed with 0 for the MD[2] bit, and counting in triangle-wave mode is performed with 1 for the MD[2] bit. The MD bits must be set while the GTCNT operation is stopped. During the event count operation (when at least one bit among the bits for the GTUPSR and GTDNSR registers is set to 1), ~~setting of the MD bits are ignored, where counting in saw-wave or triangle-wave modes is not performed. Instead, up-counting or down-counting by a source set by the GTUPSR and GTDNSR registers is performed~~ set the MD[2:0] bits to the initial value (000b).

- That's all -