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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation
https://www.renesas.com/jp/ja/support/contact/

Product Category	MPU & MCU	Document No.	TN-RA*-A0124B/E	Rev.	2.00
Title	Correction of flash cache errors		Information Category	Technical Notification	
Applicable Product	RA4E2 group, RA4M1 group, RA4T1 group, RA4W1 group, RA6E1 group, RA6E2 group, RA6M1 group, RA6M2 group, RA6M3 group, RA6M4 group, RA6M5 group, RA6T1 group, RA6T2 group, RA6T3 group, RA8D1 group, RA8M1 group, and RA8T1 group	Lot No. All	Reference Document	Refer the table 1	

Table 1 Reference Document List

No	Reference Document Name	Rev	Document Control Number	Chapter
1	RA4E2 Group User's Manual Hardware	1.30	R01UH0996EJ0130	41.5.1
2	RA4M1 Group User's Manual Hardware	1.10	R01UH0887EJ0110	44.3.1
3	RA4T1 Group User's Manual Hardware	1.20	R01UH0999EJ0120	38.5.1
4	RA4W1 Group User's Manual Hardware	1.00	R01UH0883EU0100	43.3.1
5	RA6E1 Group User's Manual Hardware	1.20	R01UH0930EJ0120	44.5.1
6	RA6E2 Group User's Manual Hardware	1.30	R01UH0988EJ0130	42.5.1
7	RA6M1 Group User's Manual Hardware	1.20	R01UH0884EJ0120	50.4.1
8	RA6M2 Group User's Manual Hardware	1.20	R01UH0885EJ0120	53.4.1
9	RA6M3 Group User's Manual Hardware	1.20	R01UH0886EJ0120	55.4.1
10	RA6M4 Group User's Manual Hardware	1.40	R01UH0890EJ0140	47.5.1
11	RA6M5 Group User's Manual Hardware	1.30	R01UH0891EJ0130	50.5.1
12	RA6T1 Group User's Manual Hardware	1.20	R01UH0897EU0120	41.4.1
13	RA6T2 Group User's Manual Hardware	1.40	R01UH0951EJ0140	43.5.1
14	RA6T3 Group User's Manual Hardware	1.20	R01UH0998EJ0120	39.5.1
15	RA8D1 Group User's Manual Hardware	1.10	R01UH0995EJ0110	52.5.1
16	RA8M1 Group User's Manual Hardware	1.10	R01UH0994EJ0110	52.5.1
17	RA8T1 Group User's Manual Hardware	1.10	R01UH1016EJ0110	46.5.1

1. The changes to the RA4E2 microcontroller group are as follows.

<Current description>

41.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 41.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from EDMAC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

＜Changed description＞

41.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 41.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from DMAC/DTC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

2. The changes for the RA4M1 group are shown below.

<Current description>

44.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for prefetch access of CPU instruction fetches.

Table 44.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative	Fully associative	-
	●64 bits/entry (64-bit aligned data) ●8 entries/ways.	●64 bits/entry (64-bit aligned data) ●1 entry.	●64 bits/entry (64-bit aligned data) ●2 entries ●Next address of previous CPU instruction.
Access cycle	Cache hit: 0 waits Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

<Changed description>

44.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for prefetch access of CPU instruction fetches.

Table 44.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from DMAC/DTC	CPU instruction fetches
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative	Fully associative	-
	●64 bits/entry (64-bit aligned data) ●8 entries/ways.	●64 bits/entry (64-bit aligned data) ●1 entry.	●64 bits/entry (64-bit aligned data) ●2 entries ●Next address of previous CPU instruction.
Access cycle	Cache hit: 0 waits Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

3. The changes for the RA4T1 group are shown below.

<Current description>

38.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 38.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from EDMAC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

38.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 38.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from DMAC/DTC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

4. The changes for the RA4W1 group are shown below.

<Current description>

43.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetch
- FCACHE2, for CPU operand access and DMA
- FLPF, for prefetch access of CPU instruction fetch.

Table 43.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative	Fully associative	-
	●64 bits/entry (64-bit aligned data) ●8 entries/ways.	●64 bits/entry (64-bit aligned data) ●1 entry.	●64 bits/entry (64-bit aligned data) ●2 entries ●Next address of previous CPU instruction.
Access cycle	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

<Changed description>

43.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetch
- FCACHE2, for CPU operand access and access from DMA/DTC
- FLPF, for prefetch access of CPU instruction fetch.

Table 43.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from DMAC/DTC	CPU instruction fetches
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative	Fully associative	-
	●64 bits/entry (64-bit aligned data) ●8 entries/ways.	●64 bits/entry (64-bit aligned data) ●1 entry.	●64 bits/entry (64-bit aligned data) ●2 entries ●Next address of previous CPU instruction.
Access cycle	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

5. The changes for the RA6E1 group are shown below.

<Current description>

44.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 44.8 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from EDMAC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

44.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access ~~and access from EDMAC~~
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 44.8 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access ~~and Access from EDMAC~~
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

6. The changes for the RA6E2 group are shown below.

<Current description>

42.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 42.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from EDMAC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

42.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 42.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from DMAC/DTC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

7. The changes for the RA6M1 group are shown below.

<Current description>

50.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 50.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	●8-way set associative ●128 bits/entry (128-bit aligned data) ●2 entries/way	●Fully associative ●128 bits/entry (128-bit aligned data) ●1 entry for FCACHE2	●Fully associative ●128 bits/entry (128-bit aligned data) ●2 entries
Access cycles	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register

<Changed description>

50.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches.

Table 50.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from DMAC/DTC	CPU instruction fetches
Capacity	256 bytes	16 bytes	32 bytes
Associativity	●8-way set associative ●128 bits/entry (128-bit aligned data) ●2 entries/way	●Fully associative ●128 bits/entry (128-bit aligned data) ●1 entry for FCACHE2	●Fully associative ●128 bits/entry (128-bit aligned data) ●2 entries
Access cycles	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register

8. The changes for the RA6M2 group are shown below.

<Current description>

53.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 53.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 000F FFFFh	0000 0000h - 000F FFFFh	0000 0000h - 000F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	●8-way set associative ●128 bits/entry (128-bit aligned data) ●2 entries/way	●Fully associative ●128 bits/entry (128-bit aligned data) ●1 entry for FCACHE2	●Fully associative ●128 bits/entry (128-bit aligned data) ●2 entries
Access cycles	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register

<Changed description>

53.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC and EDMAC
- FLPF, for the prefetch access in CPU instruction fetches.

Table 53.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 000F FFFFh	0000 0000h - 000F FFFFh	0000 0000h - 000F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from DMAC/DTC and EDMAC	CPU instruction fetches
Capacity	256 bytes	16 bytes	32 bytes
Associativity	●8-way set associative ●128 bits/entry (128-bit aligned data) ●2 entries/way	●Fully associative ●128 bits/entry (128-bit aligned data) ●1 entry for FCACHE2	●Fully associative ●128 bits/entry (128-bit aligned data) ●2 entries
Access cycles	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register

9. RA6M3 The changes for the RA6M3 group are shown below.

<Current description>

55.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 55.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch Buffer (FLPF)
Cache target region	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	●8-way set associative ●128 bits/entry (128-bit aligned data) ●2 entries/way	●Fully associative ●128 bits/entry (128-bit aligned data) ●1 entry for FCACHE2	●Fully associative ●128 bits/entry (128-bit aligned data) ●2 entries
Access cycles	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register

<Changed description>

55.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC, EDMAC, and graphic IP
- FLPF, for the prefetch access in CPU instruction fetches.

Table 55.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch Buffer (FLPF)
Cache target region	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from DMAC/DTC, EDMAC, and Graphic IP	CPU instruction fetches
Capacity	256 bytes	16 bytes	32 bytes
Associativity	●8-way set associative ●128 bits/entry (128-bit aligned data) ●2 entries/way	●Fully associative ●128 bits/entry (128-bit aligned data) ●1 entry for FCACHE2	●Fully associative ●128 bits/entry (128-bit aligned data) ●2 entries
Access cycles	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 waits ●Cache miss: Number of waits set in Flash Wait Cycle Register

10. The changes for the RA6M4 group are shown below.

<Current description>

47.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 47.8 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from EDMAC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

47.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access ~~and access from EDMAC~~
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 47.8 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access ~~and Access from EDMAC~~
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

11. The changes for the RA6M5 group are shown below.

<Current description>

50.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 50.8 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from EDMAC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

50.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access ~~and access from EDMAC~~
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 50.8 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access ~~and Access from EDMAC~~
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

12. The changes for the RA6T1 group are shown below.

<Current description>

41.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 41.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	●8-way set associative ●128 bits/entry (128-bit aligned data) ●2 entries/way	●Fully associative ●128 bits/entry (128-bit aligned data) ●1 entry for FCACHE2	●Fully associative ●128 bits/entry (128-bit aligned data) ●2 entries
Access cycles	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register

<Changed description>

41.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches.

Table 41.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from DMAC/DTC	CPU instruction fetches
Capacity	256 bytes	16 bytes	32 bytes
Associativity	●8-way set associative ●128 bits/entry (128-bit aligned data) ●2 entries/way	●Fully associative ●128 bits/entry (128-bit aligned data) ●1 entry for FCACHE2	●Fully associative ●128 bits/entry (128-bit aligned data) ●2 entries
Access cycles	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register	●Cache hit: 0 wait ●Cache miss: Number of waits set in Flash Wait Cycle Register

13. The changes for the RA6T2 group are shown below.

<Current description>

43.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 43.7 Flash Cache 2 (FCACHE2)

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

43.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 43.7 Flash Cache 2 (FCACHE2)

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and access from DMAC/DTC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

14. The changes for the RA6T3 group are shown below.

<Current description>

39.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 39.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from EDMAC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

39.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 39.7 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from DMAC/DTC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

15. The changes for the RA8D1 group are shown below.

<Current description>

52.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 52.11 Flash Cache 2 (FCACHE2) overview

Cache Target Region	Secure alias : 0x0200_0000 - 0x021F_7FFF Non-secure alias : 0x1200_0000 - 0x121F_7FFF
Target Bus Master	CPU Operand Access and Access from other than CPU
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

52.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 52.11 Flash Cache 2 (FCACHE2) overview

Cache Target Region	Secure alias : 0x0200_0000 - 0x021F_7FFF Non-secure alias : 0x1200_0000 - 0x121F_7FFF
Target Bus Master	CPU Operand Access and Access from DMAC/DTC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

16.1 The changes for the RA8M1 group are shown below.

<Current description>

52.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 52.11 Flash Cache 2 (FCACHE2) overview

Cache Target Region	Secure alias : 0x0200_0000 - 0x021F_7FFF Non-secure alias : 0x1200_0000 - 0x121F_7FFF
Target Bus Master	CPU Operand Access and Access from other than CPU
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

52.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 52.11 Flash Cache 2 (FCACHE2) overview

Cache Target Region	Secure alias : 0x0200_0000 - 0x021F_7FFF Non-secure alias : 0x1200_0000 - 0x121F_7FFF
Target Bus Master	CPU Operand Access and Access from DMAC/DTC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

17. The changes for the RA8T1 group are shown below.

<Current description>

46.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 46.11 Flash Cache 2 (FCACHE2) overview

Cache Target Region	Secure alias : 0x0200_0000 - 0x021F_7FFF Non-secure alias : 0x1200_0000 - 0x121F_7FFF
Target Bus Master	CPU Operand Access and Access from other than CPU
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

<Changed description>

46.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from DMAC/DTC
- FLPF, for the prefetch access in CPU instruction fetches

(Omitted)

Table 46.11 Flash Cache 2 (FCACHE2) overview

Cache Target Region	Secure alias : 0x0200_0000 - 0x021F_7FFF Non-secure alias : 0x1200_0000 - 0x121F_7FFF
Target Bus Master	CPU Operand Access and Access from DMAC/DTC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register