Date: Jul. 12, 2022

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A0927A/E	Rev.	1.00
Title	Correction of Errors in User's Manual		Information Category	Technical Notification		
Applicable Product	SH7214 and SH7216 Group Products SH7239 and SH7237 Group Products	Lot No. All lots	Reference Document	SH7214 Group, SH7216 Group User's Manual: Hardware Rev.4.00 (R01UH0230EJ0400) SH7239 Group, SH7237 Group User's Manual: Hardware Rev.2.00 (R01UH0086EJ0200)		

This update is to inform you of corrections to errors in the user's manuals of the above applicable products.

The table below lists the correspondences in the products.

Item	Description	Section No.	Section	Applied To: SH7214 Group, SH7216 Group	Applied To: SH7239 Group, SH7237 Group
1	Modification of the selection of operating modes	3	MCU Operating Modes	Table 3.1	Not applicable
2	Modification of the output pins for reset-synchronized PWM mode	11	MTU2	Table 11.52	Table 11.52
3	Modification of the register settings for complementary PWM mode	11	MTU2	Table 11.55	Table 11.55
4	Modification in "(g) PWM Cycle Setting"	11	MTU2	11.4.8	11.4.8
5	Modification of the example of PWM cycle updating	11	MTU2	Figure 11.42	Figure 11.42
6	Modification of the SCI interrupt sources and DTC	16	SCI	16.5	16.5
7	Modification of the ICCR2 BBSY and SCP bits and addition of the note	19	IIC3	19.3.2	Not applicable
8	Addition of the note for the master transmit operation	19	IIC3	19.4.2	Not applicable
9	Addition of the note for the slave transmit operation	19	IIC3	19.4.4	Not applicable
10	Modification in Slave Receive Mode Operation Timing (2)	19	IIC3	Figure 19.12	Not applicable
11	Modification of the example of data transfer using DTC	19	IIC3	19.6	Not applicable
12	Modification of the example of data transfer using DTC	19	IIC3	Table 19.5	Not applicable
13	Modification of the list of pin functions in each operating mode	22	PFC	Table 22.7	Not applicable
14	Modification of the FCU modes/states and acceptable commands	27/23	ROM	Table 27.13	Table 23.12
15	Modification of the SUSRDY bit in FSTATR0	27/23	ROM	27.3.7	23.3.7
16	Modification of the system configuration in USB boot mode	27	ROM	Figure 27.9	Not applicable
17	Modification of the package dimensions	-	Appendix	Figure C.1	Not applicable

<Corrections>

1. The description is modified as follows in Table 3.1 Selection of Operating Modes in "3.1 Selection of Operating Modes" of "3. MCU Operating Modes".

<<Only for SH7214 Group and SH7216 Group>>

[Before change]

	Pin Setting					
Mode No.	FWE	MD1	MD0	Mode Name	On-Chip ROM	Bus Width of CS0 Space
Mode 7*1*2	1	1	1	USB boot mode	Active	–
Mode 7*1*3	1	1	1	User program mode	Active	–

[After change]

	Pin Setting					
Mode No.	FWE	MD1	MD0	Mode Name	On-Chip ROM	Bus Width of CS0 Space
Mode 7*1*2	1	1	1	USB boot mode	Active	Set by CS0BCR in BSC
Mode 7*1*3	1	1	1	User program mode	Active	–

2. The description is modified as follows in Table 11.52 Output Pins for Reset-Synchronized PWM Mode in "11.4.7 Reset-Synchronized PWM Mode" of "11. Multi-Function Timer Pulse Unit 2 (MTU2)".

[Before change]

Channel	Output Pin	Description
3	TIOC3B	PWM output pin 1
	TIOC3D	PWM output pin 1' (negative-phase waveform of PWM output 1)
4	TIOC4A	PWM output pin 2
	TIOC4C	PWM output pin 2' (negative-phase waveform of PWM output 2)
	TIOC4B	PWM output pin 3
	TIOC4D	PWM output pin 3' (negative-phase waveform of PWM output 3)

[After change]

Channel	Output Pin	Description
3	TIOC3A	Toggle output synchronized with PWM period (or I/O port)
	TIOC3B	PWM OUTPUT PIN 1
	TIOC3D	PWM output pin 1' (negative-phase waveform of PWM output 1)
4	TIOC4A	PWM output pin 2
	TIOC4C	PWM output pin 2' (negative-phase waveform of PWM output 2)
	TIOC4B	PWM output pin 3
	TIOC4D	PWM output pin 3' (negative-phase waveform of PWM output 3)

3. The description is modified as follows in Table 11.55 Register Settings for Complementary PWM Mode in "11.4.8 Complementary PWM Mode" of "11. Multi-Function Timer Pulse Unit 2 (MTU2)".

[Before change]

Channel	Counter/Register	Description	Read/Write from CPU
	Temporary register 3 (TEMP3)	PWM output 3/TGRB_4 temporary register	Not readable/writable

[After change]

Channel	Counter/Register	Description	Read/Write from CPU
	Temporary register 3 (TEMP3)	PWM output 3/TGRB_4 temporary register	Not readable/writable
	Temporary register 4 (TEMP4)	TGRA_3 temporary register	Not readable/writable
	Temporary register 5 (TEMP5)	TCDR temporary register	Not readable/writable

4. The description is modified as follows in "(g) PWM Cycle Setting" in "11.4.8 Complementary PWM Mode" of "11. Multi-Function Timer Pulse Unit 2 (MTU2)".

[Before change]

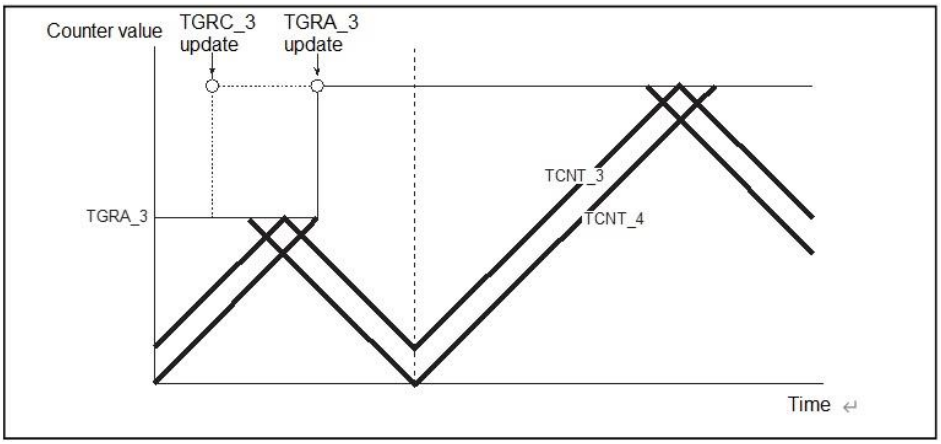
The values set in TGRC_3 and TCBR are transferred simultaneously to TGRA_3 and TCDR in accordance with the transfer timing selected with bits MD3 to MD0 in the timer mode register (TMDR).

[After change]

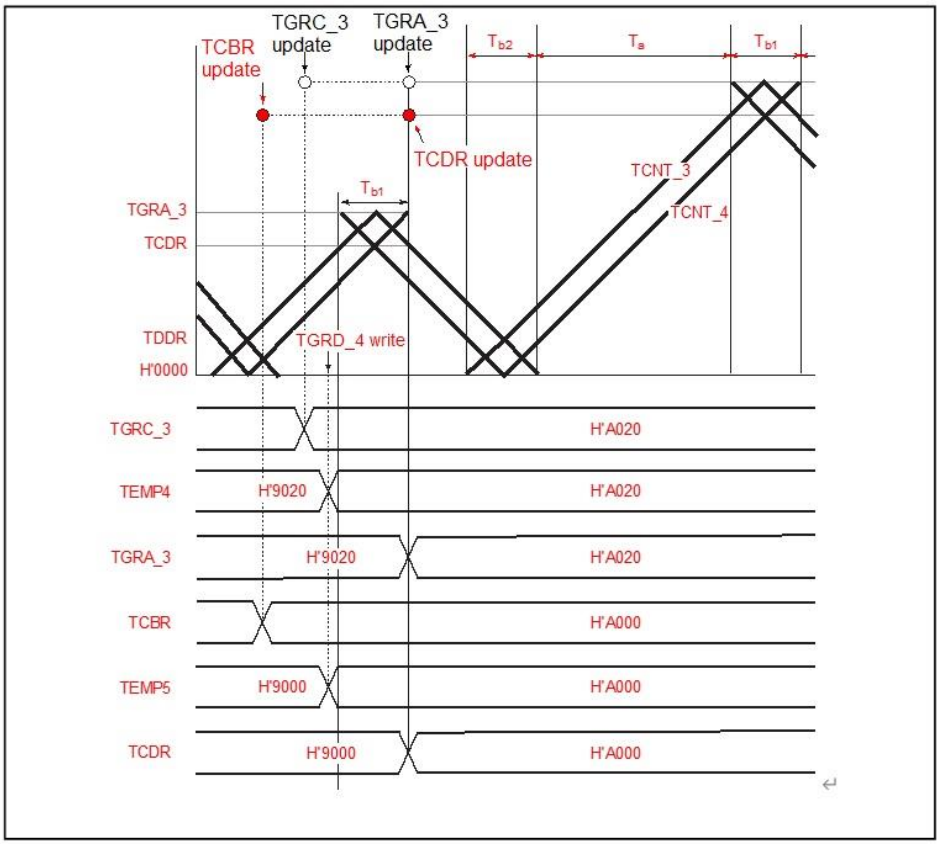
After writing to TGRD_4 and enabling the transfer, the values set in TGRC_3 and TCBR are transferred simultaneously to TGRA_3 and TCDR in accordance with the transfer timing selected with bits MD3 to MD0 in the timer mode register (TMDR).

5. The modification is made as follows in Figure 11.42 Example of PWM Cycle Updating in "11.4.8 Complementary PWM Mode" of "11. Multi-Function Timer Pulse Unit 2 (MTU2)".

[Before change]



[After change]



6. The description is modified as follows in "16.5 SCI Interrupt Sources and DTC" of "16. Serial Communication Interface (SCI)".

[Before change]

When the TDRE flag in the serial status register (SCSSR) is set to 1, a TDR empty interrupt request is generated. This request can be used to activate the data transfer controller (DTC) to transfer data. The TDRE flag is automatically cleared to 0 when data is written to the transmit data register (SCTDR) through the DTC.

When the RDRF flag in SCSSR is set to 1, an RDR full interrupt request is generated. This request can be used to activate the DTC to transfer data. The RDRF flag is automatically cleared to 0 when data is read from the receive data register (SCRDR) through the DTC.

[After change]

When the TDRE flag in the serial status register (SCSSR) is set to 1, a TXI interrupt request is generated. This request can be used to activate the data transfer controller (DTC) to transfer data.

At the data transfer through the DTC activation, when the DISEL bit of DTC is 0 and the transfer counter value is other than 0, the TDRE flag is automatically cleared to 0 when data is written to the transmit data register (SCTDR), and the TXI interrupt request to the CPU is not generated. However, when the DISEL bit is 0 and the transfer counter is 0 or the DISEL bit is 1, the TDRE flag is not cleared to 0 even if data is written to SCTDR. After writing data to SCTDR, the TXI interrupt request to the CPU is generated.

When the RDRF flag in SCSSR is set to 1, an RXI interrupt request is generated. This request can be used to activate the DTC to transfer data. At the data transfer through the DTC activation, when the DISEL bit of DTC is 0 and the transfer counter value is other than 0, the RDRF flag is automatically cleared to 0 when data is read from the receive data register (SCRDR), and the RXI interrupt request to the CPU is not generated. However, when the DISEL bit is 0 and the transfer counter is 0 or the DISEL bit is 1, the RDRF flag is not cleared to 0 even if data is read from SCRDR. After reading data from SCRDR, the RXI interrupt request to the CPU is generated.

7. The BBSY and SCP bits are modified as follows and the following note is added in "19.3.2 I^2C Bus Control Register 2 (ICCR2)" of "19. I^2C Bus Interface 3 (IIC3)".

<<Only for SH7214 Group and SH7216 Group>>

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
7	BBSY	0	R/W	Bus Busy Enables to confirm whether the I2C bus is occupied or released and to issue start/stop conditions in master mode. With the clocked synchronous serial format, this bit is always read as 0. With the I2C bus format, this bit is set to 1 when the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. This bit is cleared to 0 when the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. Write 1 to BBSY and 0 to SCP to issue a start condition. Follow this procedure when also re-transmitting a start condition. Write 0 in BBSY and 0 in SCP to issue a stop condition.
6	SCP	1	R/W	Start/Stop Issue Condition Disable Controls the issue of start/stop conditions in master mode. To issue a start condition, write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, write 0 in BBSY and 0 in SCP. This bit is always read as 1. Even if 1 is written to this bit, the data will not be stored.
~	~	~	~	~
1	IICRST	0	R/W	IIC Control Part Reset Resets the control part except for I^2C registers. If this bit is set to 1 when hang-up occurs because of communication failure during I^2C bus operation, some IIC3 registers and the control part can be reset.

[After change]

Bit	Bit Name	Initial Value	R/W	Description
7	BBSY	0	R/W	Bus Busy Enables to confirm whether the I2C bus is occupied or released and to issue start/stop conditions in master mode. With the clocked synchronous serial format, this bit is always read as 0. With the I2C bus format, this bit is set to 1 when the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. This bit is cleared to 0 when the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. Write 1 to BBSY and 0 to SCP at the same time to issue a start condition. Follow this procedure when also re-transmitting a start condition. Write 0 in BBSY and 0 in SCP at the same time to issue a stop condition.
6	SCP	1	R/W	Start/Stop Issue Condition Disable Controls the issue of start/stop conditions in master mode. To issue a start condition, write 1 in BBSY and 0 in SCP at the same time. A retransmit start condition is issued in the same way. To issue a stop condition, write 0 in BBSY and 0 in SCP at the same time. This bit is always read as 1. Even if 1 is written to this bit, the data will not be stored.
1	IICRST*	0	R/W	IIC Control Part Reset Resets the control part except for I^2C registers. If this bit is set to 1 when hang-up occurs because of communication failure during I^2C bus operation, some IIC3 registers and the control part can be reset.

Note: * Writing 1 to the IICRST bit in ICCR2 causes the following state.

During a reset due to the IICRST bit being set to 1, serial data transmission is terminated. However, the functions to detect start and stop conditions and arbitration lost operates. After the reset, perform the initial setting because the IICR1, IICR2, and ICSR states might be updated depending on the signals input on the SCL and SDA pins.

8. The following note is added to "19.4.2 Master Transmit Operation" of "19. I^2C Bus Interface 3 (IIC3)".

<<Only for SH7214 Group and SH7216 Group>>

[After change]

Note: When *NACKF = 1 is detected, be sure to clear the NACKF bit during the transfer termination processing. Next transmission/reception cannot be performed until it is cleared.

9. The following note is added to "19.4.4 Slave Transmit Operation" of "19. I^2C Bus Interface 3 (IIC3)".

<<Only for SH7214 Group and SH7216 Group>>

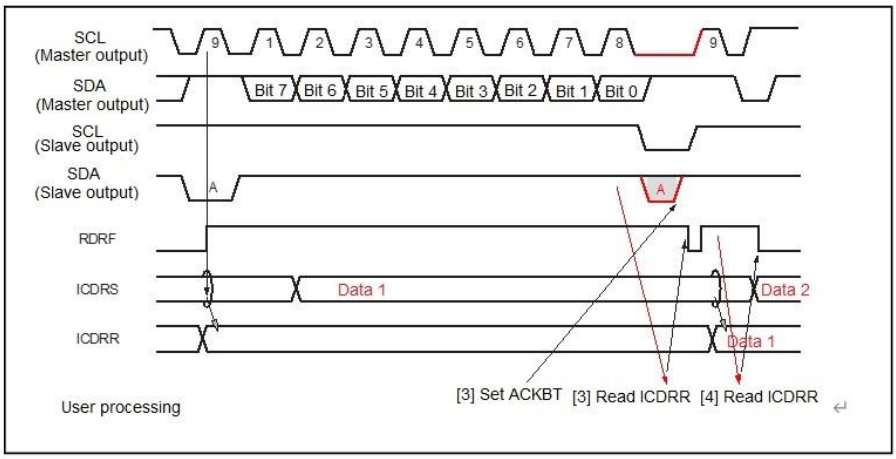
[After change]

Note: When *NACKF = 1 is detected, be sure to clear the NACKF bit during the transfer termination processing. Next transmission/reception cannot be performed until it is cleared.

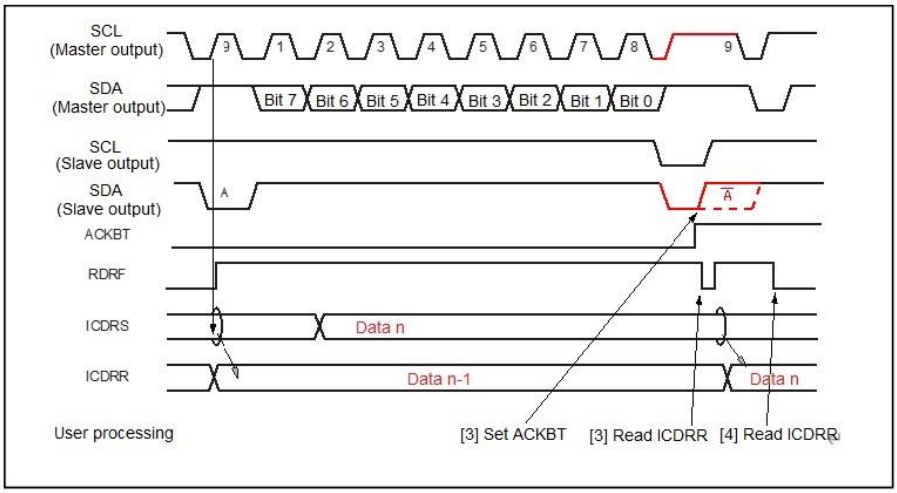
10. The description is modified as follows in Figure 19.12 Slave Receive Mode Operation Timing (2) in "19.4.5 Slave Receive Operation" of "19. I²C Bus Interface 3 (IIC3)".

<<Only for SH7214 Group and SH7216 Group>>

[Before change]



[After change]



11. The description is modified as follows in "19.6 Data Transfer Using DTC" of "19. I²C Bus Interface 3 (IIC3)".

<<Only for SH7214 Group and SH7216 Group>>

[Before change]

19.6 Data Transfer Using DTC

In the I²C bus format, the slave device and transfer direction are selected through the slave address and R/$\overline{W}$ bit, and data reception is confirmed and the last frame is indicated through the acknowledge bit. Therefore, when the DTC is used to transfer data continuously, the DTC processing should be done in combination with the CPU processing activated by interrupts.

Table 19.5 shows an example of I2C data transfer using the DTC. This example assumes that the transfer data count is determined in advance in slave mode.

[After change]

19.6 Data Transfer Using DMAC/DTC

In the I²C bus format, the slave device and transfer direction are selected through the slave address and R/$\overline{W}$ bit, and data reception is confirmed and the last frame is indicated through the acknowledge bit. Therefore, when the DMAC/DTC is used to transfer data continuously, the DMAC/DTC processing should be done in combination with the CPU processing activated by interrupts.

Table 19.5 shows an example of I2C data transfer using the DMAC/DTC. This example assumes that the transfer data count is determined in advance in slave mode.

12. The description is modified as follows in Table 19.5 Example of Data Transfer Using DTC in "19.6 Data Transfer Using DTC" of "19. I^2C Bus Interface 3 (IIC3)".

<<Only for SH7214 Group and SH7216 Group>>

[Before change]

Table 19.5 Example of Data Transfer Using DTC

Item	Master Transmit Mode	Master Receive Mode	Slave Transmit Mode	Slave Receive Mode
Slave address + R/$\overline{W}$ bit transmit/receive	Transmitted by DTC (ICDR writing)	Transmitted by CPU (ICDR writing)	Received by CPU (ICDR reading)	Received by CPU (ICDR reading)
Dummy data read	–	Processed by CPU (ICDR writing)	–	–
Main data transmit/receive	Transmitted by DTC (ICDR writing)	Received by DTC (ICDR reading)	Transmitted by DTC (ICDR writing)	Received by DTC (ICDR reading)
Last frame processing	Not necessary	Received by CPU (ICDR reading)	Not necessary	Received by CPU (ICDR reading)
DTC transfer data frame count setting	Transmission: Actual data count + 1 (+1 is required for the slave address + R/$\overline{W}$ bit transfer)	Reception; Actual data count	Transmission; Actual data count	Reception; Actual data count

[After change]

Table 19.5 Example of Data Transfer Using DMAC/DTC

Item	Master Transmit Mode	Master Receive Mode	Slave Transmit Mode	Slave Receive Mode
Slave address + R/$\overline{W}$ bit transmit/receive	Transmitted by DMAC/DTC* (ICDRT writing)	Transmitted by CPU (ICDRT writing)	Received by CPU (ICDRR reading)	Received by CPU (ICDRR reading)
Dummy data read	–	Processed by CPU (ICDRR reading)	–	Processed by CPU (ICDRR reading)
Main data transmit/receive	Transmitted by DMAC/DTC (ICDRT writing)	Received by DMAC/DTC (ICDRR reading)	Transmitted by DMAC/DTC (ICDRT writing)	Received by DMAC/DTC (ICDRR reading)
Last frame processing	Not necessary	Received by CPU (ICDRR reading)	Not necessary	Received by CPU (ICDRR reading)
DTC transfer data frame count setting	Transmission: Actual data count + 1 (+1 is required for the slave address + R/$\overline{W}$ bit transfer)	Reception; Actual data count	Transmission; Actual data count	Reception; Actual data count

Note: * After issuing a start condition (writing 1 to BBSY and 0 to SCP), enable the DMAC/DTC transfer.

13. The description is modified as follows in Table 22.7 List of pin functions in each operating mode of "22. Pin Function Controller (PFC)".

<<Only for SH7214 Group and SH7216 Group>>

[Before change]

Pin number	Pin number	Pin name				
		Initial function				
		On-chip ROM unabled mode		On-chip ROM enabled mode	Single-chip mode	
BGA	LQFP	MCU mode 0	MCU mode 1	MCU mode 2	MCU mode 3	Settable function in PFC
B5	167	PE9				PE9/DACK2/TIOC3B/TX_EN
C5	168	PE10				PE10/DREQ3/TIOC3C/SSL3/ TXD2/TX_CLK

[After change]

Pin number	Pin number	Pin name				
		Initial function				
		On-chip ROM unabled mode		On-chip ROM enabled mode	Single-chip mode	
BGA	LQFP	MCU mode 0	MCU mode 1	MCU mode 2	MCU mode 3	Settable function in PFC
B5	168	PE9				PE9/DACK2/TIOC3B/TX_EN
C5	167	PE10				PE10/DREQ3/TIOC3C/SSL3/ TXD2/TX_CLK

14. The description is modified as follows in Table 27.13 FCU Modes/States and Acceptable Commands in "27. Flash Memory (ROM)". (The section and table numbers are for SH7214 Group and SH7216 Group. Table 23.12 of Section 23 for SH7239 Group and SH7237 Group.)

[Before change]

	P/E Normal Mode			Status Read Mode							Lock Bit Read Mode		
Item	**Programming-Suspended**	**Erasure-Suspended**	**Other State**	**Programming/Erasure Processing**	**Programming/Erasure Suspension Processing**	**Lock Bit Read 2 Processing**	**Programming-Suspended**	**Erasure-Suspended**	**Command-Locked**	**Other State**	**Programming-Suspended**	**Erasure-suspended**	**Other State**
FRDY bit in FSTATR0	1	1	1	0	0	0	1	1	0/1	1	1	1	1
SUSRDY bit in FSTATR0	0	0	0	1	0	0	0	0	0	0	0	0	0
ERSSPD bit in FSTATR0	0	1	0	0	0/1	0	0	1	0	0	0	1	0
PRGSPD bit in FSTATR0	1	0	0	0	0/1	0	1	0	0	0	1	0	0
CMDLK bit in FASTAT	0	0	0	0	0	0	0	0	1	0	0	0	0
Normal mode transition	A	A	A	×	×	×	A	A	×	A	A	A	A
Status read mode transition	A	A	A	×	×	×	A	A	×	A	A	A	A
Lock bit read mode transition (lock bit read 1)	A	A	A	×	×	×	A	A	×	A	A	A	A
Program	×	*	A	×	×	×	×	*	×	A	×	*	A
Block erase	×	×	A	×	×	×	×	×	×	A	×	×	A
P/E suspend	×	×	×	A	×	×	×	×	×	×	×	×	×
P/E resume	A	A	×	×	×	×	A	A	×	×	A	A	×
Status register clear	A	A	A	×	×	×	A	A	A	A	A	A	A
Lock bit read 2	A	A	A	×	×	×	A	A	×	A	A	A	A
Lock bit program	×	*	A	×	×	×	×	*	×	A	×	*	A
Peripheral clock notification	×	×	A	×	×	×	×	×	×	A	×	×	A

[After change]

	P/E Normal Mode			Status Read Mode								Lock Bit Read Mode		
Item	Programming-Suspended	Erasure-Suspended	Other State	Programming/Erasure Processing	Programming Processing During Erasure-Suspended	Programming/Erasure Suspension Processing	Lock Bit Read 2 Processing	Programming-Suspended	Erasure-Suspended	Command-Locked (FRDY = 0)	Command-Locked (FRDY = 1)	Other State	Programming-Suspended	Erasure-suspended	Other State
FRDY bit in FSTATR0	1	1	1	0	0	0	0	1	1	0	1	1	1	1	1
SUSRDY bit in FSTATR0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
ERSSPD bit in FSTATR0	0	1	0	0	1	0/1	0/1	0	1	0/1	0/1	0	0	1	0
PRGSPD bit in FSTATR0	1	0	0	0	0	0/1	0/1	1	0	0/1	0/1	0	1	0	0
CMDLK bit in FASTAT	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
Normal mode transition	A	A	A	×	×	×	×	A	A	×	×	A	A	A	A
Status read mode transition	A	A	A	×	×	×	×	A	A	×	×	A	A	A	A
Lock bit read mode transition (lock bit read 1)	A	A	A	×	×	×	×	A	A	×	×	A	A	A	A
Program	×	*	A	×	×	×	×	×	*	×	×	A	×	*	A
Block erase	×	×	A	×	×	×	×	×	×	×	×	A	×	×	A
P/E suspend	×	×	×	A	×	×	×	×	×	×	×	×	×	×	×
P/E resume	A	A	×	×	×	×	×	A	A	×	×	×	A	A	×
Status register clear	A	A	A	×	×	×	×	A	A	×	A	A	A	A	A
Lock bit read 2	A	A	A	×	×	×	×	A	A	×	×	A	A	A	A
Lock bit program	×	*	A	×	×	×	×	×	*	×	×	A	×	*	A
Peripheral clock notification	×	×	A	×	×	×	×	×	×	×	×	A	×	×	A

15. The description is modified as follows in the SUSRDY bit in "27.3.7 Flash Status Register 0 (FSTATR0)" of "27. Flash Memory (ROM)". (The section number is for SH7214 Group and SH7216 Group. Section 23 is for SH7239 Group and SH7237 Group.)

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
3	SUSRDY	0	R	Suspend Ready Indicates whether the FCU is ready to accept a P/E suspend command. 0: The FCU cannot accept a P/E suspend command 1: The FCU can accept a P/E suspend command [Setting condition] •After initiating programming/erasure, the FCU has entered a state where it is ready to accept a P/E suspend command. [Clearing conditions] •The FCU has accepted a P/E suspend command. •The FCU has entered a command-locked state during programming or erasure.

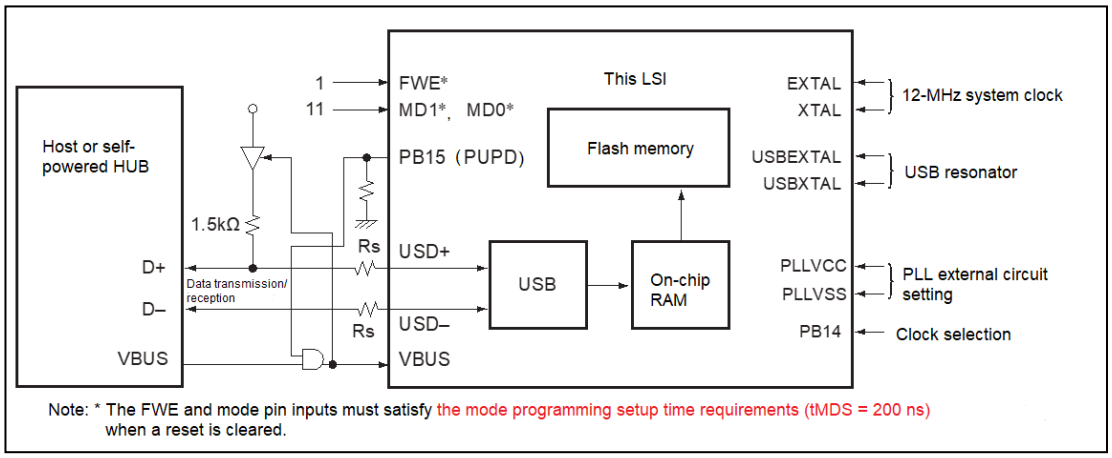
[After change]

Bit	Bit Name	Initial Value	R/W	Description
3	SUSRDY	0	R	Suspend Ready Indicates whether the FCU is ready to accept a P/E suspend command. 0: The FCU cannot accept a P/E suspend command 1: The FCU can accept a P/E suspend command [Setting condition] •After initiating programming/erasure, the FCU has entered a state where it is ready to accept a P/E suspend command. [Clearing conditions] •The FCU has accepted a P/E suspend command. •The FCU has entered a command-locked state during programming or erasure. •Programming or erasure has finished.

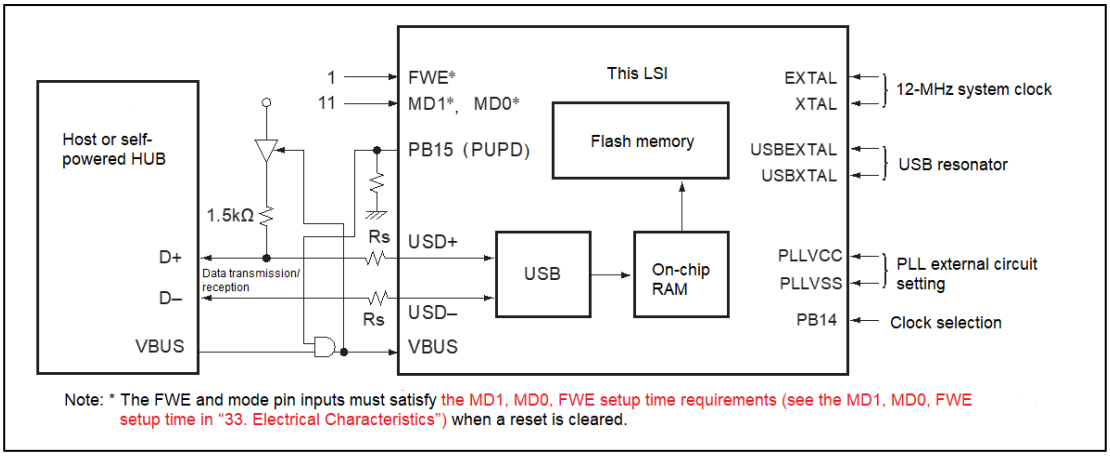
16. The description is modified as follows in Figure 27.9 System Configuration in USB Boot Mode in "27.5.4 USB Boot Mode" of "27. Flash Memory (ROM)".

<<Only for SH7214 Group and SH7216 Group>>

[Before change]



[After change]

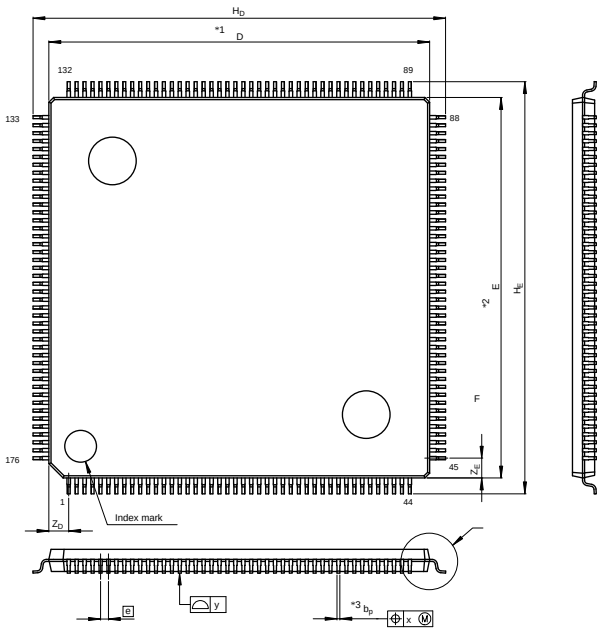


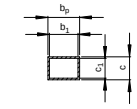
17. The description is modified as follows in Figure C.1 Package Dimensions (1) in "C. Package Dimensions" of "Appendix".

<<Only for SH7214 Group and SH7216 Group>>

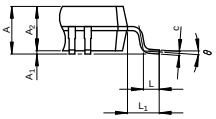
[After change]

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A / FP-176E / FP-176EV	1.8g





Terminal cross section



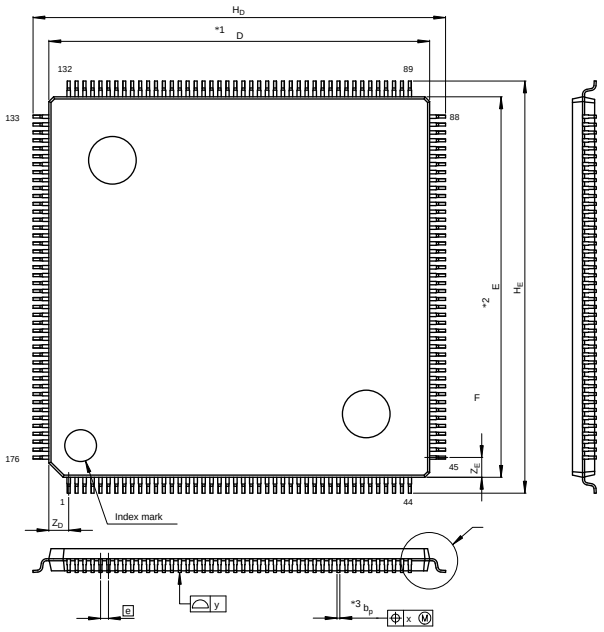
Detail F

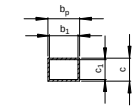
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

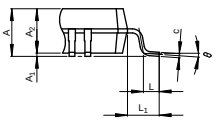
[After change]

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A / FP-176E / FP-176EV	1.8g





Terminal cross section



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Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—