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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A797A/E	Rev.	1.00
Title	Correction of Errors in SH7239 Group, SH7237 Group User's Manual (Hardware)		Information Category	Technical Notification		
Applicable Product	SH7239 Group SH7237 Group	Lot No. All lots	Reference Document	SH7239 Group, SH7237 Group User's Manual: Hardware Rev. 1.00 (R01UH0086EJ0100)		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the corrections to errors in the hardware manual of the above applicable products.

Please pay attention to these corrections when using the products.

The following items in the SH7239 Group, SH7237 Group User's Manual (Hardware) are corrected.

(1) Section 15 Watchdog Timer (WDT) p. 660 Description of watchdog timer control/status register (WTCSR)

(2) Section 15 Watchdog Timer (WDT) p. 665 Description of watchdog timer mode usage

(3) Section 16 Serial Communication Interface (SCI) p. 689 Description of serial status register (SCSSR)

(4) Section 23 Flash Memory (ROM) p. 1190 Figure 23.18 Flow for Using the Peripheral Clock Notification Command

(1) Section 15 Watchdog Timer (WDT) p. 660

15.3.2 Watchdog Timer Control/Status Register (WTCSR)

[Before correction]

WTCSR is initialized to H'18 by a power-on reset caused by the $\overline{\text{RES}}$ pin or in software standby mode.

[After correction]

WTCSR is initialized to H'18 by a power-on reset caused by the $\overline{\text{RES}}$ pin, an internal reset caused by the WDT, or in software standby mode.

(2) Section 15 Watchdog Timer (WDT) p. 665

The following is added to the description in section 15.4.2, Using Watchdog Timer Mode.

[After correction]

7. Since WTCSR is initialized by an internal reset caused by the WDT, the TME bit in WTCSR is cleared to 0. This makes the counter stop (be initialized). To use the WDT in watchdog timer mode again, after clearing the WOVF flag in WRCSR, set watchdog timer mode again.

(3) Section 16 Serial Communication Interface (SCI) p. 689

16.3.7 Serial Status Register (SCSSR)

[Before correction]

Bit	Bit Name	Initial Value	R/W	Description
2	TEND	1	R	Transmit End [Clearing condition] • When 0 is written to TEND after reading TEND = 1

[After correction]

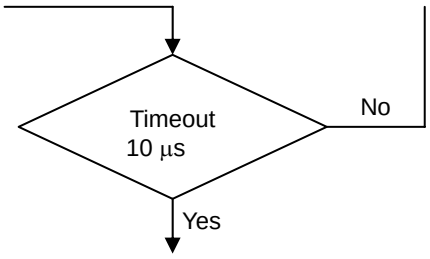
Bit	Bit Name	Initial Value	R/W	Description
2	TEND	1	R	Transmit End [Clearing condition] • When 0 is written to TDRE after reading TDRE = 1

(4) Section 23 Flash Memory (ROM) p. 1190

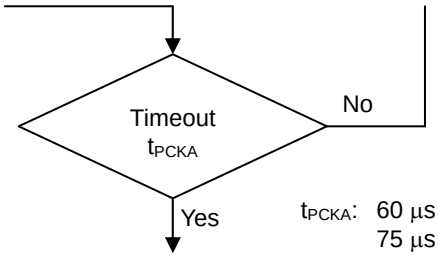
23.6.3 FCU Command Usage

Figure 23.18 Flow for Using the Peripheral Clock Notification Command

[Before correction]



[After correction]



t_{PCKA}: 60 µs for Pϕ = 50 MHz
75 µs for Pϕ = 40 MHz
120 µs for Pϕ = 25 MHz
150 µs for Pϕ = 20 MHz