Date: Apr. 28, 2011

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A794A/E	Rev.	1.00
Title	Correction of Errors in SH7214 Group, SH7216 Group User's Manual (Hardware)		Information Category	Technical Notification		
Applicable Product	SH7214 Group SH7216 Group	Lot No. All lots	Reference Document	SH7214 Group, SH7216 Group User's Manual: Hardware (REJ09B0543-0200)		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the corrections to errors in the hardware manual of the above applicable products.

Refer to the following for details.

The description in section 15.3.2 "Watchdog Timer Control/Status Register (WTCSR)" of section 15 "Watchdog Timer (WDT)" on p. 744 is corrected as follows.

[Before correction]

WTCSR is initialized to H'18 by a power-on reset caused by the $\overline{\text{RES}}$ pin or in software standby mode.

[After correction]

WTCSR is initialized to H'18 by a power-on reset caused by the $\overline{\text{RES}}$ pin, an internal reset caused by the WDT, or in software standby mode.

The following is added to the description in section 15.4.2 "Using Watchdog Timer Mode" of section 15 "Watchdog Timer (WDT)" on p. 749.

[After correction]

7. Since WTCSR is initialized by an internal reset caused by the WDT, the TME bit in WTCSR is cleared to 0. This makes the counter stop (be initialized). To use the WDT in watchdog timer mode again, after clearing the WOVF flag in WRCSR, set watchdog timer mode again.

The description of the TEND bit in section 16.3.7 "Serial Status Register (SCSSR)" of section 16 "Serial Communication Interface (SCI)" on p. 772 is corrected as follows.

[Before correction]

Bit	Bit Name	Initial Value	R/W	Description
2	TEND	1	R	Transmit End [Clearing condition] • When 0 is written to TEND after reading TEND = 1

[After correction]

Bit	Bit Name	Initial Value	R/W	Description
2	TEND	1	R	Transmit End [Clearing condition] • When 0 is written to TDRE after reading TDRE = 1

The following description is added to section 21.9 "Usage Notes" in section 21 "Controller Area Network (RCAN-ET)".

[After change]

21.9 Usage Notes

21.9.1 Module Stop Mode

The clock supply to RCAN-ET can be stopped or started by using the standby control register 6 (STBCR6). With the initial value, the clock supply is stopped. Access to the RCAN-ET registers should be made only after releasing RCAN-ET from module stop mode.

21.9.2 Reset

RCAN-ET can be reset by hardware reset or software reset.

- Hardware reset

  RCAN-ET is reset to the initial state by power-on reset or on entering module stop mode.

- Software reset

  By setting the MCR0 bit in Master Control Register (MCR), RCAN-ET registers, excluding the MCR0 bit, and the CAN communication circuitry are initialized.

Since the IRR0 bit in Interrupt Request Register (IRR) is set by the initialization upon reset, it should be cleared while RCAN-ET is in configuration mode during the reset sequence.

The areas except for message control field 1 (CONTROL1) of mailboxes are not initialized by reset because they are in RAM. After power-on reset, all mailboxes should be initialized while RCAN-ET is in configuration mode during the reset sequence.

21.9.3 CAN Sleep Mode

In CAN sleep mode, the clock supply to the major parts in the module is stopped. Therefore, do not make access in CAN sleep mode except for access to the MCR, GSR, IRR, and IMR registers.

21.9.4 Register Access

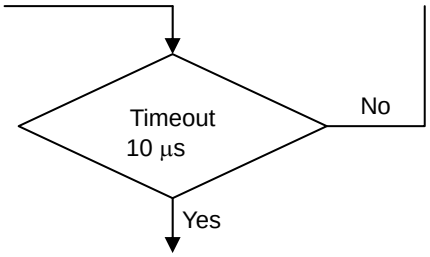
If the mailbox area is accessed while the CAN communication circuitry in RCAN-ET is storing a received CAN bus frame in a mailbox, a 0 to five peripheral clock cycles of wait state is generated.

21.9.5 Interrupts

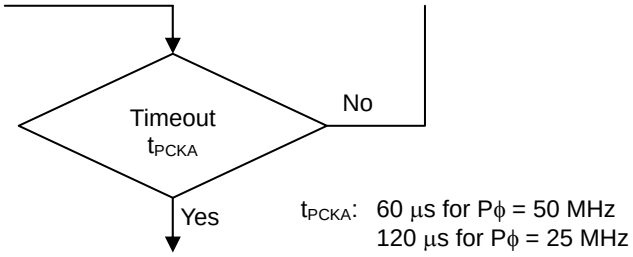
As shown in table 22.2, a Mailbox 0 receive interrupt can activate the DTC. If configured such that the DTC is activated by a Mailbox 0 receive interrupt and clearing of the interrupt source flag upon DTC transfer is enabled, use block transfer mode and read the whole Mailbox 0 message up to the message control field 1 (CONTROL1).

Figure 27.19 "Flow for Using the Peripheral Clock Notification Command" in section 27 "Flash Memory (ROM)" on p. 1521 is corrected as follows.

[Before correction]



[After correction]



The description in section 31.3 "Boundary Scan TAP Controller" of section 31 "User Debugging Interface (H-UDI)" on p. 1626 is corrected as follows.

[Before correction]

3. When the boundary scan function is executed, the maximum frequency of TCK is 25 MHz.

[After correction]

3. When the boundary scan function is executed, the maximum frequency of TCK is 6.25 MHz. When an H-UDI function is executed, the maximum frequency of TCK is 25 MHz.

Table 33.21 and figure 33.66 in section 33.3.17 "H-UDI Related Pin Timing" of section 33 "Electrical Characteristics" on p. 1808 and p. 1809, respectively, are corrected as follows.

[Before correction]

Item	Symbol	Min.	Max.	Unit	Figure
TCK cycle time	t_{TCKcyc}	50*	—	ns	Figure 33.65
TCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time	t_{TDIS}	15	—	ns	Figure 33.66
TDI hold time	t_{TDIH}	15	—	ns	
TMS setup time	t_{TMSS}	15	—	ns	
TMS hold time	t_{TMSH}	15	—	ns	
TDO delay time	t_{TDOD}	—	30	ns	

Note: * This value must exceed the cycle time for the peripheral clock (Pϕ).

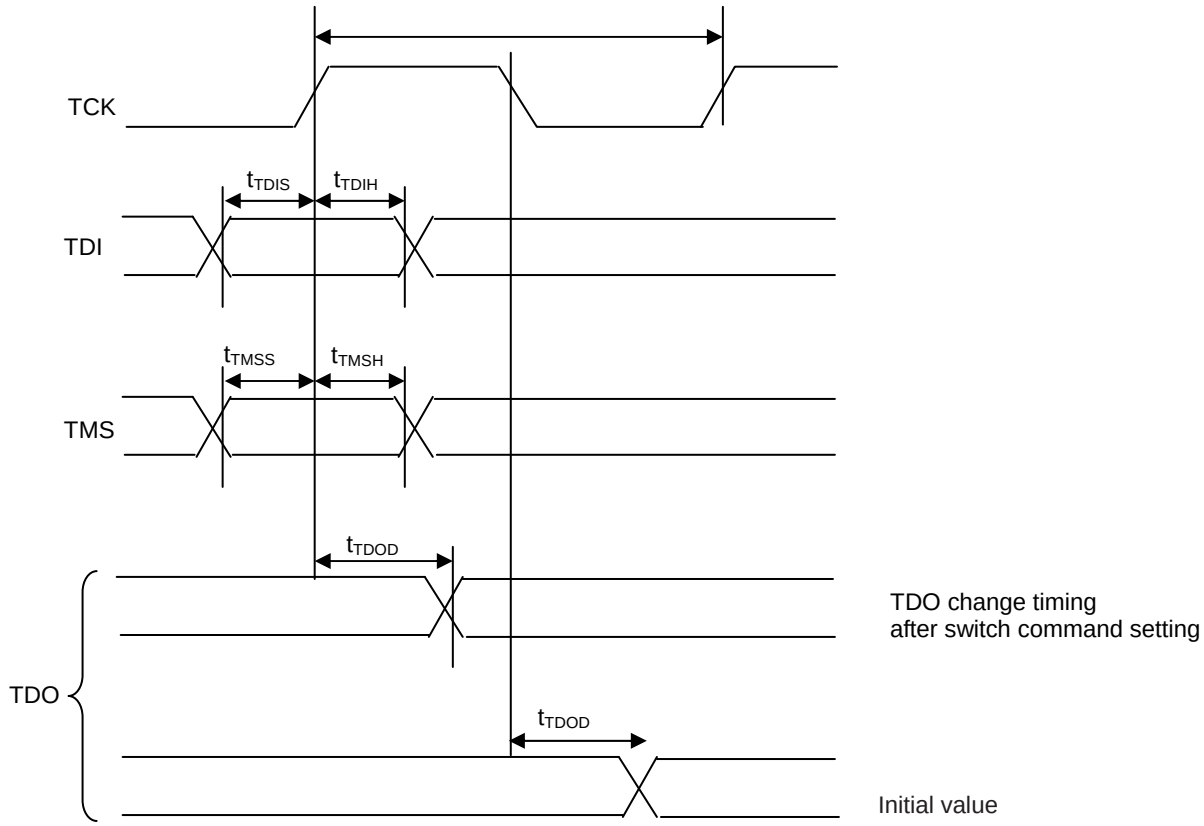
[After correction]

Item	Symbol	Min.	Max.	Unit	Figure
TCK cycle time	t_{TCKcyc}	40*1	—	ns	Figure 33.65
		160*2	—	ns	
TCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time	t_{TDIS}	15	—	ns	Figure 33.66
TDI hold time	t_{TDIH}	15	—	ns	
TMS setup time	t_{TMSS}	15	—	ns	
TMS hold time	t_{TMSH}	15	—	ns	
TDO delay time	t_{TDOD}	—	30*1	ns	
		—	80*2	ns	
Output pins other than TDO	t_{OTHERD}	—	80*2	ns	

Notes: 1. This value must exceed the cycle time for the peripheral clock (Pϕ).

2. TCK cycle time when the boundary scan function is executed

[Before correction]



[After correction]

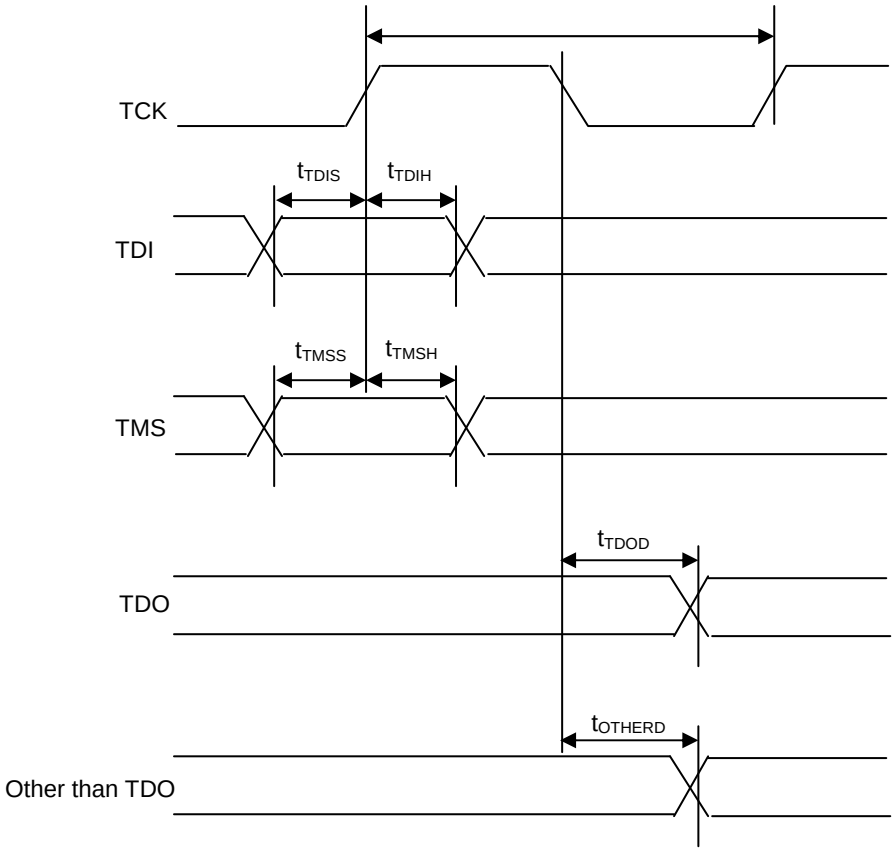


Table 33.24 in section 33.6 "Flash Memory Characteristics" of section 33 "Electrical Characteristics" on p. 1814 is corrected as follows.

[Before correction]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Suspend delay time during writing	t_{SPD}	—	—	T.B.D.	µs	Figure 33.70
First suspend delay time during erasing (in suspension priority mode)	t_{SESD1}	—	—	T.B.D.	µs	Pϕ = 50 MHz

[After correction]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Suspend delay time during writing	t_{SPD}	—	—	225	µs	Pϕ = 20 MHz
				175		Pϕ = 40 MHz
				155		Pϕ = 50 MHz
First suspend delay time during erasing (in suspension priority mode)	t_{SESD1}	—	—	220	µs	Pϕ = 20 MHz
				130		Pϕ = 40 MHz
				120		Pϕ = 50 MHz

Table 33.25 in section 33.7 "FLD Characteristics" of section 33 "Electrical Characteristics" on p. 1816 is corrected as follows.

[Before correction]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Suspend delay time during writing	t_{SPD}	—	—	T.B.D.	µs	Figure 33.70
First suspend delay time during erasing (in suspension priority mode)	t_{SESD1}	—	—	T.B.D.	µs	Pϕ = 50 MHz

[After correction]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Suspend delay time during writing	t_{SPD}	—	—	225	µs	Pϕ = 20 MHz
				175		Pϕ = 40 MHz
				155		Pϕ = 50 MHz
First suspend delay time during erasing (in suspension priority mode)	t_{SESD1}	—	—	220	µs	Pϕ = 20 MHz
				130		Pϕ = 40 MHz
				120		Pϕ = 50 MHz

Figure C.2 "Package Dimensions (2)" in appendix C "Package Dimensions" on p. 1834 is corrected as follows.

[Before correction]

RENESAS Code PLQP0176LB-A

Previous Code FP176-A/FP-176AV

MASS [Typ.] 1.4g

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	20	—
E	—	20	—
C	0.12	0.17	0.22
C1	—	0.15	—
L	0.4	0.50	0.6

[After correction]

RENESAS Code PLQP0176LA-B

Previous Code —

MASS [Typ.] 1.3g

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20	20.1
E	19.9	20	20.1
C	0.09	0.145	0.20
C1	—	0.125	—
L	0.35	0.50	0.65

The following tables of "Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output" are added to section 9 "Bus State Controller (BSC)" on p. 330.

[After correction]

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**00 (11 Bits)**	**00 (8 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A25	A17		Unused
A16	A24	A16		
A15	A23	A15		
A14	A22*2	A22*2	A12 (BA1)	Specifies bank
A13	A21*2	A21*2	A11 (BA0)	
A12	A20	L/H*1	A10/AP	Specifies address/precharge
A11	A19	A11	A9	Address
A10	A18	A10	A8	
A9	A17	A9	A7	
A8	A16	A8	A6	
A7	A15	A7	A5	
A6	A14	A6	A4	
A5	A13	A5	A3	
A4	A12	A4	A2	
A3	A11	A3	A1	
A2	A10	A2	A0	
A1	A9	A1		Unused
A0	A8	A0		
Examples of connected memory				
64-Mbit product (512 Kwords × 32 bits × 4 banks, column 8 bits product): 1				
16-Mbit product (512 Kwords × 16 bits × 2 banks, column 8 bits product): 2				

Notes: 1. L/H is a bit used in the command specification; it is fixed at L or H according to access the mode.

2. Bank address specification

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**01 (12 Bits)**	**00 (8 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A24	A17		Unused
A16	A23	A16		
A15	A23*2	A23*2	A13 (BA1)	Specifies bank
A14	A22*2	A22*2	A12 (BA0)	
A13	A21	A13	A11	Address
A12	A20	L/H*1	A10/AP	Specifies address/precharge
A11	A19	A11	A9	Address
A10	A18	A10	A8	
A9	A17	A9	A7	
A8	A16	A8	A6	
A7	A15	A7	A5	
A6	A14	A6	A4	
A5	A13	A5	A3	
A4	A12	A4	A2	
A3	A11	A3	A1	
A2	A10	A2	A0	
A1	A9	A1		Unused
A0	A8	A0		
Examples of connected memory				
128-Mbit product (1 Mword × 32 bits × 4 banks, column 8 bits product): 1				
64-Mbit product (1 Mword × 16 bits × 4 banks, column 8 bits product): 2				

Notes: 1. L/H is a bit used in the command specification; it is fixed at L or H according to access the mode.

2. Bank address specification

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**01 (12 Bits)**	**01 (9 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A26	A17		Unused
A16	A25	A16		
A15	A24*2	A24*2	A13 (BA1)	Specifies bank
A14	A23*2	A23*2	A12 (BA0)	
A13	A22	A13	A11	Address
A12	A21	L/H*1	A10/AP	Specifies address/precharge
A11	A20	A11	A9	Address
A10	A19	A10	A8	
A9	A18	A9	A7	
A8	A17	A8	A6	
A7	A16	A7	A5	
A6	A15	A6	A4	
A5	A14	A5	A3	
A4	A13	A4	A2	
A3	A12	A3	A1	
A2	A11	A2	A0	
A1	A10	A1		Unused
A0	A9	A0		
Examples of connected memory				
256-Mbit product (2 Mwords × 32 bits × 4 banks, column 9 bits product): 1				
128-Mbit product (2 Mwords × 16 bits × 4 banks, column 9 bits product): 2				

Notes: 1. L/H is a bit used in the command specification; it is fixed at L or H according to access the mode.

2. Bank address specification

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**01 (12 Bits)**	**10 (10 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A27	A17		Unused
A16	A26	A16		
A15	A25*2	A25*2	A13 (BA1)	Specifies bank
A14	A24*2	A24*2	A12 (BA0)	
A13	A23	A13	A11	Address
A12	A22	L/H*1	A10/AP	Specifies address/precharge
A11	A21	A11	A9	Address
A10	A20	A10	A8	
A9	A19	A9	A7	
A8	A18	A8	A6	
A7	A17	A7	A5	
A6	A16	A6	A4	
A5	A15	A5	A3	
A4	A14	A4	A2	
A3	A13	A3	A1	
A2	A12	A2	A0	
A1	A11	A1		Unused
A0	A10	A0		
Examples of connected memory				
512-Mbit product (4 Mwords × 32 bits × 4 banks, column 10 bits product): 1				
256-Mbit product (4 Mwords × 16 bits × 4 banks, column 10 bits product): 2				

Notes: 1. L/H is a bit used in the command specification; it is fixed at L or H according to access the mode.

2. Bank address specification

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**10 (13 Bits)**	**01 (9 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A26	A17		Unused
A16	A25	A16	A14 (BA1)	Specifies bank
A15	A24*[2]	A25*[2]	A13 (BA0)	
A14	A23*[2]	A24*[2]	A12	Address
A13	A22	A13	A11	
A12	A21	L/H*[1]	A10/AP	Specifies address/precharge
A11	A20	A11	A9	Address
A10	A19	A10	A8	
A9	A18	A9	A7	
A8	A17	A8	A6	
A7	A16	A7	A5	
A6	A15	A6	A4	
A5	A14	A5	A3	
A4	A13	A4	A2	
A3	A12	A3	A1	
A2	A11	A2	A0	
A1	A10	A1		Unused
A0	A9	A0		
Examples of connected memory				
512-Mbit product (4 Mwords × 32 bits × 4 banks, column 9 bits product): 1				
256-Mbit product (4 Mwords × 16 bits × 4 banks, column 9 bits product): 2				

Notes: 1. L/H is a bit used in the command specification; it is fixed at L or H according to access the mode.

2. Bank address specification