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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A005A/E	Rev.	1.00
Title	The correction of errors in the I2C Bus Interface (RIIC) Hardware Manual		Information Category	Technical Notification		
Applicable Product	RX610 Group RX62N、RX621 Group RX62T Group	Lot No. All Lot	Reference Document	RX610 Group RX62N、RX621 Group RX62T Group Hardware Manual		

In the applicable products mentioned above, there are some errors in the User's Manual: Hardware, regarding the description, example of flowchart, and operation timing (3) on the RIIC master receive operation.

Therefore, we would like to correct them as follows. In the following, "section xx" represents "section 22" in the RX610 Group, "section 30" in the RX62N, RX621 Group, and "section 23" in the RX62T Group, respectively.

1. The corrections of errors「xx.3.4 Master Receiver Operation」

【before】

5. After one byte of data has been received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the eighth or ninth cycle of SCL clock (the clock signal) as selected by the RDRFS bit in ICMR3. Reading out ICDRR at this time will produce the received data, and the RDRF flag is automatically cleared to 0 at the same time. Furthermore, the value of the acknowledgement field received during the ninth cycle of SCL clock is returned as the value set in the ACKBT bit of ICMR3.
6. When the next value to be received will be the final byte, set the WAIT bit in ICMR3 to 1 (so that waiting is applied) before reading ICDRR. This causes the SCLn line to be held low from the falling edge of the ninth clock cycle after reception of the next data (i.e. the final byte), enabling issuance of a stop condition. However, when the ICMR3.RDRFS bit is 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next (final) byte, set the ACKBT bit in ICMR3 to 1 (NACK).

【after】

5. After one byte of data has been received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the eighth or ninth cycle of SCL clock (the clock signal) as selected by the RDRFS bit in ICMR3. Reading out ICDRR at this time will produce the received data, and the RDRF flag is automatically cleared to 0 at the same time. Furthermore, the value of the acknowledgement field received during the ninth cycle of SCL clock is returned as the value set in the ACKBT bit of ICMR3.Furthermore, if the next byte to be received is the next to last byte, set the ICMR3.WAIT bit to 1 (for wait insertion) before reading the ICDRR (containing the second byte from last). As well as enabling NACK output even in the case of delays in processing to set the ICMR3.ACKBT bit to 1 (NACK) in step (6), due to other interrupts etc., this fixes the SCLn line to the low level on the rising edge of the ninth clock cycle in reception of the last byte, so the state is such that issuing a stop condition is possible.
6. When the ICMR3.RDRFS bit is 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next (final) byte, set the ACKBT bit in ICMR3 to 1 (NACK).

2. The corrections of errors「xx.3.4 Example of Master Reception Flowchart」

【before】

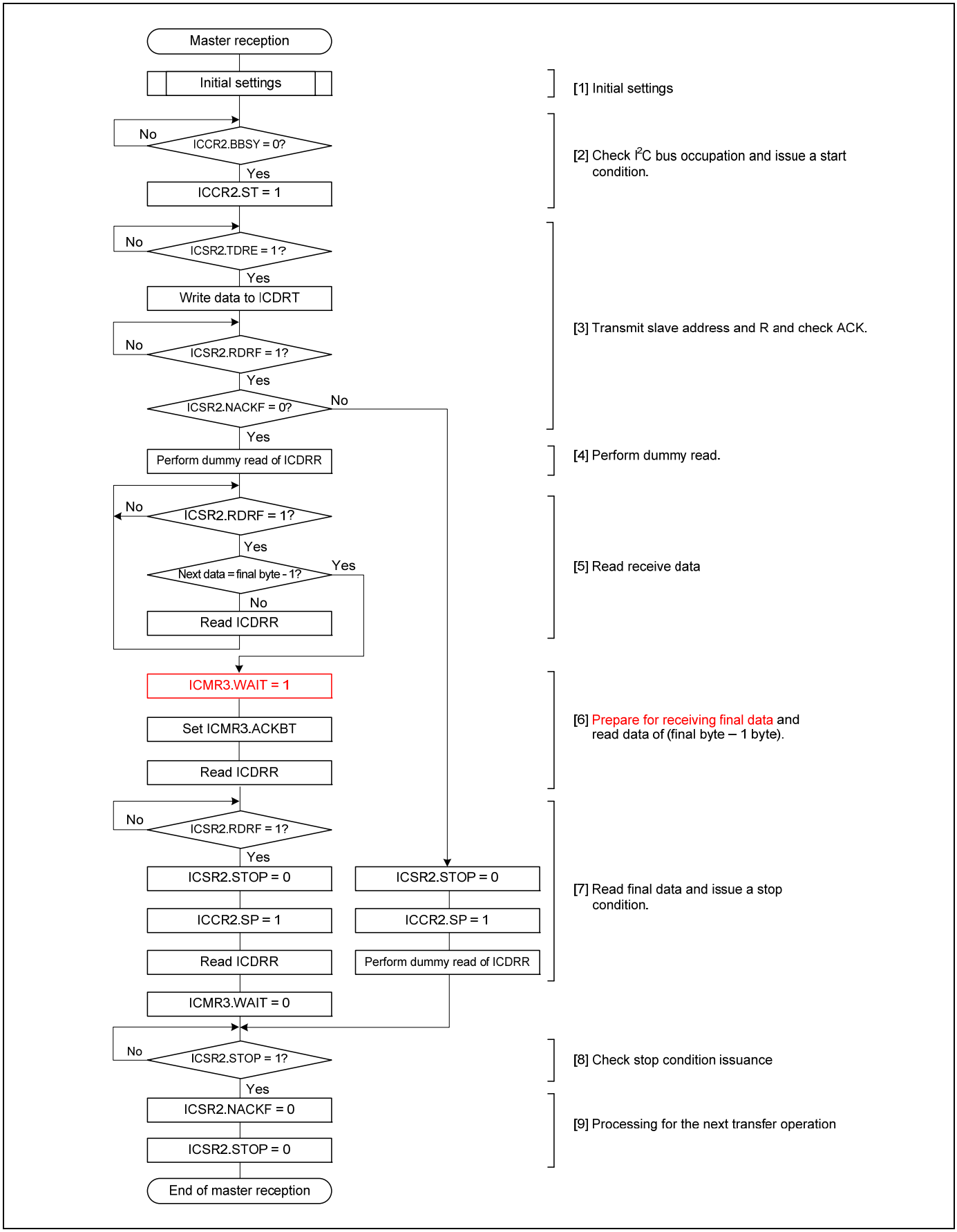

Figure xx.10 Example of Master Reception Flowchart (7-Bit Address Format)

【after】

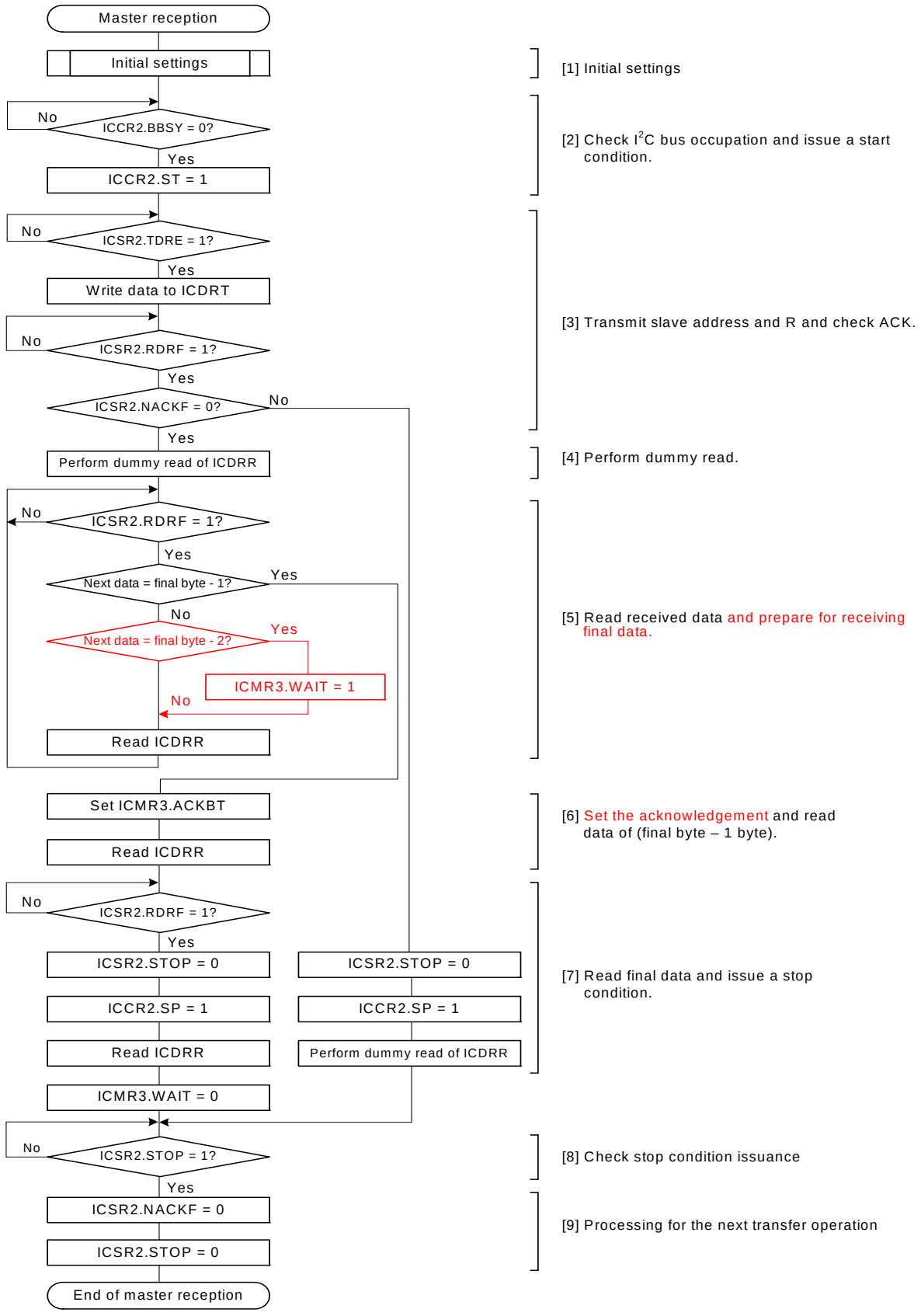

Figure xx.10 Example of Master Reception Flowchart (7-Bit Address Format)

3. The corrections of errors「xx.3.4 Master Receive Operation Timing (3)」

【before】

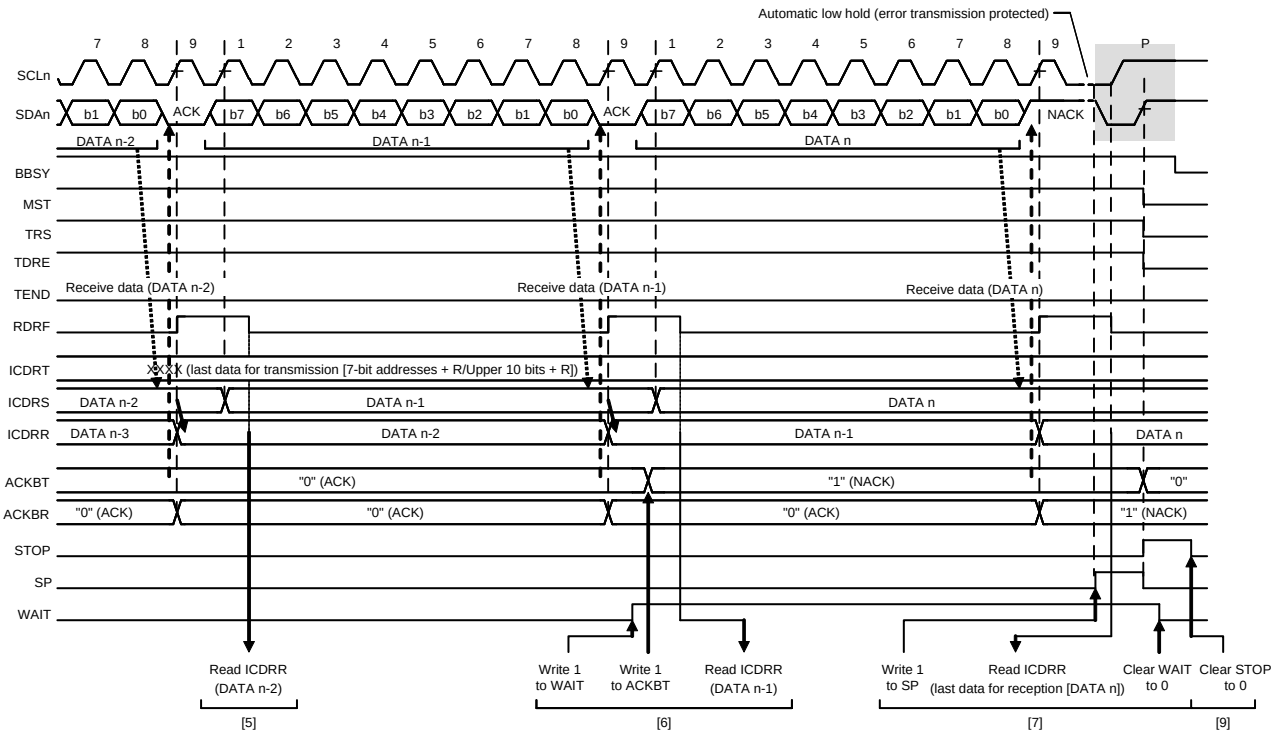

Figure xx.13 Master Receive Operation Timing (3) (when RDRFS=0)

【after】

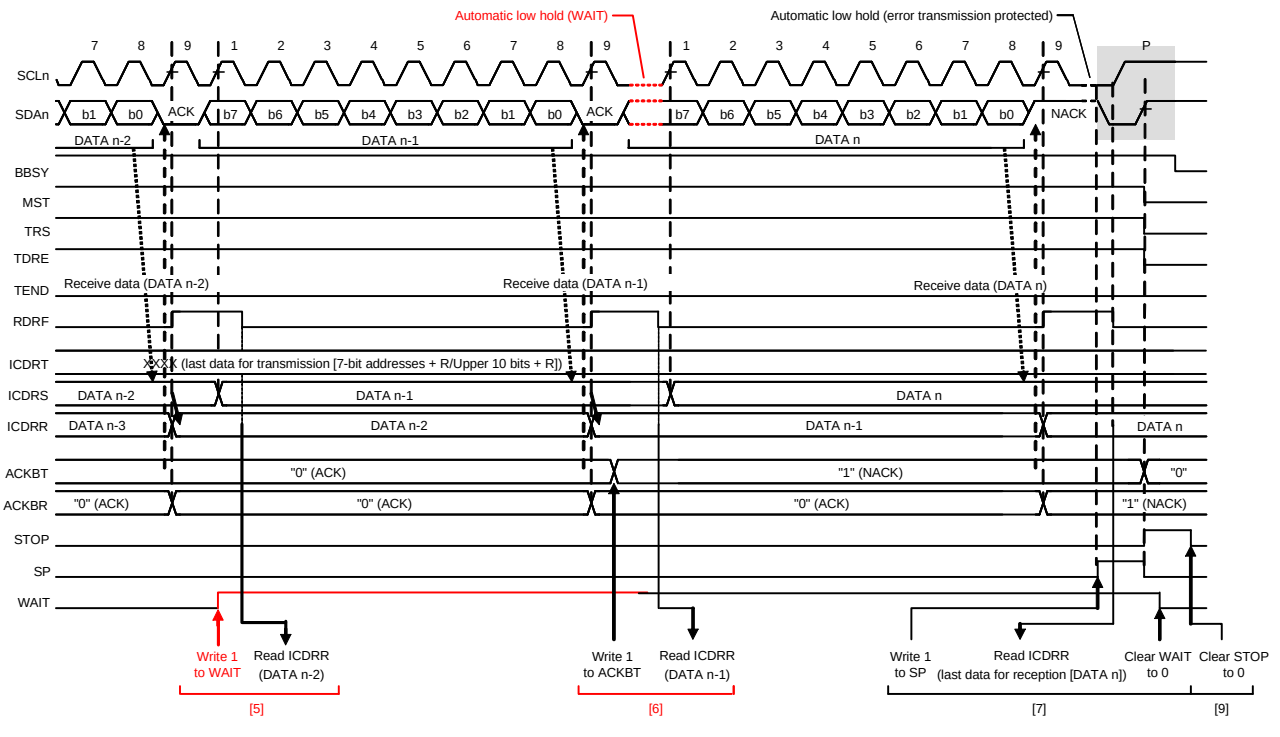

Figure xx.13 Master Receive Operation Timing (3) (when RDRFS=0)