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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU	Document No.	TN-H8*-264A/EA	Rev.	1.0
Title	Correction of Errors Concerning the 8-Bit Timer (TMR) in the H8S/2168 Group and H8S/2158		Information Category	Correction or Supplement of Documents	
Applicable Product	H8S/2168, H8S/2167, H8S/2166, and H8S/2158	Lot No.: All	Reference Document	H8S/2168 Group Hardware Manual REJ09B0078-0200Z Rev.2.0 H8S/2158 Hardware Manual ADE-602-255A Rev.2.0	

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the correction of errors concerning the function of the 8-bit timer (TMR) in the H8S/2168 Group Hardware Manual and H8S/2158 Hardware Manual as shown below.

The descriptions of cascading of the TMR_X and TMR_Y for the 8-bit timer (TMR) are deleted.

Correction 1: Section 12.1, Features, in the H8S/2168 Group Hardware Manual

[Before Change]

- Cascading of two channels
  - — Cascading of TMR_0 and TMR_1

    Operation as a 16-bit timer can be performed using TMR_0 as the upper half and TMR_1 as the lower half (16-bit count mode).

    TMR_1 can be used to count TMR_0 compare-match occurrences (compare-match count mode).
  - — Cascading of TMR_Y and TMR_X

    Operation as a 16-bit timer can be performed using TMR_Y as the upper half and TMR_X as the lower half (16-bit count mode).

    TMR_X can be used to count TMR_Y compare-match occurrences (compare-match count mode).

[After Change]

- Cascading of TMR_0 and TMR_1
  - — (TMR_Y and TMR_X cannot be cascaded)

    Operation as a 16-bit timer can be performed using TMR_0 as the upper half and TMR_1 as the lower half (16-bit count mode).

    TMR_1 can be used to count TMR_0 compare-match occurrences (compare-match count mode).

Correction 2: Table 12.2, Clock Input to TCNT and Count Condition, in the H8S/2168 Group Hardware Manual

[Before Change]

	TCR			STCR		
Channel	**CKS2**	**CKS1**	**CKS0**	**ICKS1**	**ICKS0**	**Description**
TMR_Y	0	1	1	—	—	Increments at falling edge of internal clock φ/2048
	1	0	0	—	—	Increments at overflow signal from TCNT_X*
TMR_X	0	0	0	—	—	Disables clock input
	0	0	1	—	—	Increments at falling edge of internal clock φ
	0	1	1	—	—	Increments at falling edge of internal clock φ/4
	1	0	0	—	—	Increments at compare-match A from TCNT_Y

[After Change]

	TCR			STCR		
Channel	**CKS2**	**CKS1**	**CKS0**	**ICKS1**	**ICKS0**	**Description**
TMR_Y	0	1	1	—	—	Increments at falling edge of internal clock φ/2048
	1	0	0	—	—	Setting prohibited
TMR_X	0	0	0	—	—	Disables clock input
	0	0	1	—	—	Increments at falling edge of internal clock φ
	0	1	1	—	—	Increments at falling edge of internal clock φ/4
	1	0	0	—	—	Setting prohibited

Correction 3: Note of table 12.2, Clock Input to TCNT and Count Condition, in the H8S/2168 Group Hardware Manual

[Before Change]

Note: * If the TMR_0 clock input is set as the TCNT_1 overflow signal and the TMR_1 clock input is set as the TCNT_0 compare-match signal simultaneously, a count-up clock cannot be generated. Similarly, If the TMR_Y clock input is set as the TCNT_X overflow signal and the TMR_X clock input is set as the TCNT_Y compare-match signal simultaneously, a count-up clock cannot be generated. Simultaneous setting of these two conditions should therefore be avoided.

[After Change]

Note: * If the TMR_0 clock input is set as the TCNT_1 overflow signal and the TMR_1 clock input is set as the TCNT_0 compare-match signal simultaneously, a count-up clock cannot be generated. Simultaneous setting of this condition should therefore be avoided.

Correction 4: Section 12.7, TMR_Y and TMR_X Cascaded Connection, in the H8S/2168 Group Hardware Manual

The descriptions other than section 12.7.3, Input Capture Operation, are deleted: the first four lines in section 12.7 and the descriptions of section 12.7.1, 16-Bit Count Mode, and section 12.7.2, Compare-Match Count Modem, are deleted.

Section 12.7.3 is changed to section 12.7.

Correction 5: Section 12.9.6, Mode Setting with Cascaded Connection, in the H8S/2168 Group Hardware Manual

[Before Change]

If the 16-bit count mode and compare-match count mode are set simultaneously, the input clock pulses for TCNT_0 and TCNT_1 (or TCNT_Y and TCNT_X) are not generated…

[After Change]

If the 16-bit count mode and compare-match count mode are set simultaneously, the input clock pulses for TCNT_0 and TCNT_1 are not generated…

Correction 6: Section 13.1, Features, in the H8S/2158 Hardware Manual

[Before Change]

- Cascading of two channels
  - Cascading of TMR_0 and TMR_1

    Operation as a 16-bit timer can be performed using TMR_0 as the upper half and TMR_1 as the lower half (16-bit count mode).

    TMR_1 can be used to count TMR_0 compare-match occurrences (compare-match count mode).
  - Cascading of TMR_Y and TMR_X

    Operation as a 16-bit timer can be performed using TMR_Y as the upper half and TMR_X as the lower half (16-bit count mode).

    TMR_X can be used to count TMR_Y compare-match occurrences (compare-match count mode).

[After Change]

- Cascading of TMR_0 and TMR_1
  - (TMR_Y and TMR_X cannot be cascaded)

    Operation as a 16-bit timer can be performed using TMR_0 as the upper half and TMR_1 as the lower half (16-bit count mode).

    TMR_1 can be used to count TMR_0 compare-match occurrences (compare-match count mode).

Correction 7: Table 13.2, Clock Input to TCNT and Count Condition, in the H8S/2158 Hardware Manual

[Before Change]

	TCR			STCR		
Channel	**CKS2**	**CKS1**	**CKS0**	**ICKS1**	**ICKS0**	**Description**
TMR_Y	0	1	1	—	—	Increments at falling edge of internal clock φ/2048
	1	0	0	—	—	Increments at overflow signal from TCNT_X*
TMR_X	0	0	0	—	—	Disables clock input
	0	0	1	—	—	Increments at falling edge of internal clock φ
	0	1	1	—	—	Increments at falling edge of internal clock φ/4
	1	0	0	—	—	Increments at compare-match A from TCNT_Y

[After Change]

	TCR			STCR		
Channel	**CKS2**	**CKS1**	**CKS0**	**ICKS1**	**ICKS0**	**Description**
TMR_Y	0	1	1	—	—	Increments at falling edge of internal clock φ/2048
	1	0	0	—	—	Setting prohibited
TMR_X	0	0	0	—	—	Disables clock input
	0	0	1	—	—	Increments at falling edge of internal clock φ
	0	1	1	—	—	Increments at falling edge of internal clock φ/4
	1	0	0	—	—	Setting prohibited

Correction 8: Note of table 13.2, Clock Input to TCNT and Count Condition, in the H8S/2158 Hardware Manual

[Before Change]

Note: * If the TMR_0 clock input is set as the TCNT_1 overflow signal and the TMR_1 clock input is set as the TCNT_0 compare-match signal simultaneously, a count-up clock cannot be generated. Similarly, If the TMR_Y clock input is set as the TCNT_X overflow signal and the TMR_X clock input is set as the TCNT_Y compare-match signal simultaneously, a count-up clock cannot be generated. Simultaneous setting of these two conditions should therefore be avoided.

[After Change]

Note: * If the TMR_0 clock input is set as the TCNT_1 overflow signal and the TMR_1 clock input is set as the TCNT_0 compare-match signal simultaneously, a count-up clock cannot be generated. Simultaneous setting of this condition should therefore be avoided.

Correction 9: Section 13.7, TMR_Y and TMR_X Cascaded Connection, in the H8S/2158 Hardware Manual

The descriptions other than section 13.7.3, Input Capture Operation, are deleted: the first four lines in section 13.7 and the descriptions of section 13.7.1, 16-Bit Count Mode, and section 13.7.2, Compare-Match Count Modem, are deleted.

Section 13.7.3 is changed to section 13.7.

Correction 10: Section 13.9.6, Mode Setting with Cascaded Connection, in the H8S/2158 Hardware Manual

[Before Change]

If the 16-bit count mode and compare-match count mode are set simultaneously, the input clock pulses for TCNT_0 and TCNT_1 (or TCNT_Y and TCNT_X) are not generated…

[After Change]

If the 16-bit count mode and compare-match count mode are set simultaneously, the input clock pulses for TCNT_0 and TCNT_1 are not generated…