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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RX*-A145A/E	Rev.	1.00
Title	Correction of erroneous descriptions in the RX230 Group, RX231 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX231 Group	Lot No. All	Reference Document	RX230 Group, RX231 Group User's Manual: Hardware Rev.1.10 (R01UH0496EJ0110)		

This is to inform you of corrections in the RX230 Group, RX231 Group User's Manual: Hardware Rev.1.10 as follows.

<Details of corrections>

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The number of pins in Table 1 Specification Differences Depending on Packages is corrected as follows.

[Before correction]

Chapter	Specification Differences	
	Products with 40 pins or less	Products with 48 pins or more

[After correction]

Chapter	Specification Differences	
	48-pin package products	64- and 100-pin package products

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The item of the SD host interface in Table 2 Major Specification Differences by Product Group and Chip versions (2/2) is corrected as follows.

[Before correction]

Section	RX231 Group			RX230 Group
	Chip version B	Chip version A	Chip version C	
40. SD Host Interface (SDHIa)	The SD host interface is present.	The SD host interface is not present.		

[After correction]

Section	RX231 Group			RX230 Group
	Chip version B	Chip version A	Chip version C	
40. SD Host Interface (SDHIa)	The SD host interface is present (except 48-pin package products).	The SD host interface is not present.		

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Note in the SD host interface is deleted.

[Before correction]

- SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported
  Note: 48-pin packages support 1-bit mode only

[After correction]

- SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported

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The line of the SD host interface in Table 1.2 Comparison of Functions for Different Packages is corrected as follows.

[Before correction]

Module/Functions		RX230 Group			RX231 Group		
		100 Pins	64 Pins	48 Pins	100 Pins	64 Pins	48 Pins
Communication functions	CAN module	Not supported			1 channel		
	SD Host Interface	Not supported			1 channel		

[After correction]

Module/Functions		RX230 Group			RX231 Group		
		100 Pins	64 Pins	48 Pins	100 Pins	64 Pins	48 Pins
Communication functions	CAN module	Not supported			1 channel*1		
	SD Host Interface	Not supported			1 channel*1		Not supported

Note 1. Only for chip version B

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The SDHI item for the following parts of 48-pin package products in Table 1.3 List of Products is changed from “Available” to “Not available”.

[Before correction]

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318BDNE	R5F52318BDNE#U0	PWQN0048KB-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Available	Available	Available	–40 to +85°C
	R5F52318BDFL	R5F52318BDFL#30	PLQP0048KB-B					Available	Available	Available	
	R5F52317BDNE	R5F52317BDNE#U0	PWQN0048KB-A	384 Kbytes	64 Kbytes			Available	Available	Available	
	R5F52317BDFL	R5F52317BDFL#30	PLQP0048KB-B					Available	Available	Available	

[After correction]

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318BDNE	R5F52318BDNE#U0	PWQN0048KB-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Available	Not available	Available	–40 to +85°C
	R5F52318BDFL	R5F52318BDFL#30	PLQP0048KB-B					Available	Not available	Available	
	R5F52317BDNE	R5F52317BDNE#U0	PWQN0048KB-A	384 Kbytes	64 Kbytes			Available	Not available	Available	
	R5F52317BDFL	R5F52317BDFL#30	PLQP0048KB-B					Available	Not available	Available	

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The SDHI item for the following parts of 48-pin package products in Table 1.4 List of Products is changed from “Available” to “Not available”.

[Before correction]

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318BGNE	R5F52318BGNE#U0	PWQN0048KB-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Available	Available	Available	–40 to +105°C
	R5F52318BGFL	R5F52318BGFL#30	PLQP0048KB-B					Available	Available	Available	
	R5F52317BGNE	R5F52317BGNE#U0	PWQN0048KB-A	384 Kbytes	64 Kbytes			Available	Available	Available	
	R5F52317BGFL	R5F52317BGFL#30	PLQP0048KB-B					Available	Available	Available	

[After correction]

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	SDHI	CAN	Operating Temperature
RX231	R5F52318BGNE	R5F52318BGNE#U0	PWQN0048KB-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Available	Not available	Available	–40 to +105°C
	R5F52318BGFL	R5F52318BGFL#30	PLQP0048KB-B					Available	Not available	Available	
	R5F52317BGNE	R5F52317BGNE#U0	PWQN0048KB-A	384 Kbytes	64 Kbytes			Available	Not available	Available	
	R5F52317BGFL	R5F52317BGFL#30	PLQP0048KB-B					Available	Not available	Available	

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The description of the chip versions in Figure 1.1 is corrected as follows.

[Before correction]

Chip versions
RX231 Group
A: Security function not included, SDHI module not included, CAN module included
B: Security function included, SDHI module included, CAN module included
C: Security function not included, SDHI module not included, CAN module not included

[After correction]

Chip versions
RX231 Group
A: Security function not included, SDHI module not included, CAN module included
B: Security function included, SDHI module included (except 48-pin package products), CAN module included
C: Security function not included, SDHI module not included, CAN module not included

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The pins of the SDHI are deleted from Table 1.10 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) and the USB pin is added.

[Before correction]

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
24		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	SDHI_D1	TSCAP	
25		PB5/PC3	MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4		SDHI_CD		
26		PB3/PC2	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOCD3/TCLKD	SCK6	SDHI_WP		
27		PB1/PC1	MTIOC0C/MTIOC4C/TMCI0/ TIOCB3	TXD6/SMOSI6/SSDA6	SDHI_CLK		IRQ4/ CMPOB1
28	VCC						
29		PB0/PC0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA	SDHI_CMD		

[After correction]

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
24		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0		TSCAP	
25		PB5/PC3	MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4	USB0_VBUS			
26		PB3/PC2	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOCD3/TCLKD	SCK6			
27		PB1/PC1	MTIOC0C/MTIOC4C/TMCI0/ TIOCB3	TXD6/SMOSI6/SSDA6			IRQ4/ CMPOB1
28	VCC						
29		PB0/PC0	MTIC5W/TIOCA3	RXD6/SMISO6/SSCL6/RSPCKA			

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The allocation port for the IRQ2 pin is corrected from " ○ (available)" to "× (not available)" in Table 22.1 Allocation of Pin Functions to Multiple Pins

[Before correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
Interrupt	IRQ2 (input)	P32	○	○	×
		P12	○	×	×
		PD2	○	×	×

[After correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
Interrupt	IRQ2 (input)	P32	○	×	×
		P12	○	×	×
		PD2	○	×	×

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The allocation port for the MTIOC0C pin is corrected from " ○ (available)" to "× (not available)" in Table 22.1 Allocation of Pin Functions to Multiple Pins

[Before correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
Multi-function timer unit 2	MTIOC0C (input/output)	P32	○	○	×
		PB1	○	○	○

[After correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
Multi-function timer unit 2	MTIOC0C (input/output)	P32	○	×	×
		PB1	○	○	○

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The allocation port for the TMO3 pin is corrected from " ○ (available)" to "× (not available)" in Table 22.1 Allocation of Pin Functions to Multiple Pins

[Before correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
8-bit timer	TMO3 (output)	P13	○	×	×
		P32	○	○	×
		P55	○	○	×

[After correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
8-bit timer	TMO3 (output)	P13	○	×	×
		P32	○	×	×
		P55	○	○	×

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The allocation port for the TXD6, SMOSI6, and SSDA6 pins is corrected from " ○ (available)" to "× (not available)" in Table 22.1 Allocation of Pin Functions to Multiple Pins

[Before correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
Serial communications interface	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P32	○	○	×
		PB1	○	○	○

[After correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
Serial communications interface	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P32	○	×	×
		PB1	○	○	○

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The allocation port for the RTCOUT and RTCIC2 pins is corrected from " ○ (available)" to "× (not available)" in Table 22.1 Allocation of Pin Functions to Multiple Pins

[Before correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
Realtime clock	RTCOUT (output)	P16	○	○	×
		P32	○	○	×
	RTCIC0 (input)*1	P30	○	○	×
	RTCIC1 (input)*1	P31	○	○	×
	RTCIC2 (input)*1	P32	○	○	×

[After correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
Realtime clock	RTCOUT (output)	P16	○	○	×
		P32	○	×	×
	RTCIC0 (input)*1	P30	○	○	×
	RTCIC1 (input)*1	P31	○	○	×
	RTCIC2 (input)*1	P32	○	×	×

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The allocation port for the SDHI pins and the USB0_VBUSEN pin is corrected from " ○ (available)" to "× (not available)" in Table 22.1 Allocation of Pin Functions to Multiple Pins

[Before correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
SD host interface	SDHI_CLK (output)	PB1	○	○	○
	SDHI_CMD (input/output)	PB0	○	○	○
	SDHI_D0 (input/output)	PC3	○	○	×
	SDHI_D1 (input/output)	PB6	○	○	×
		PC4	○	○	○
	SDHI_D2 (input/output)	PB7	○	○	×
	SDHI_D3 (input/output)	PC2	○	○	×
	SDHI_CD (input)	PB5	○	○	○
	SDHI_WP (input)	PB3	○	○	○
USB 2.0 host/function module	USB0_VBUSEN (output)	P16	○	○	○
		P24	○	×	×
		P26	×	○	○
		P32	○	○	×

[After correction]

Module/Function	Pin Functions	Allocation Port	Package		
			100-pin	64-pin	48-pin
SD host interface	SDHI_CLK (output)	PB1	○	○	×
	SDHI_CMD (input/output)	PB0	○	○	×
	SDHI_D0 (input/output)	PC3	○	○	×
	SDHI_D1 (input/output)	PB6	○	○	×
		PC4	○	○	×
	SDHI_D2 (input/output)	PB7	○	○	×
	SDHI_D3 (input/output)	PC2	○	○	×
	SDHI_CD (input)	PB5	○	○	×
	SDHI_WP (input)	PB3	○	○	×
USB 2.0 host/function module	USB0_VBUSEN (output)	P16	○	○	○
		P24	○	×	×
		P26	×	○	○
		P32	○	×	×

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The pins of the SDHI in Table 22.17 Register Settings for Input/Output Pin Function in 48-Pin are deleted.

[Before correction]

PSEL[4:0] Settings	Pin			
	PB0	PB1	PB3	PB5
10001b	—	—	—	USB0_VBUS
11010b	SDHI_CMD	SDHI_CLK	SDHI_WP	SDHI_CD

[After correction]

PSEL[4:0] Settings	Pin			
	PB0	PB1	PB3	PB5
10001b	—	—	—	USB0_VBUS

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The pins of the SDHI in Table 22.20 Register Settings for Input/Output Pin Function in 48-Pin are deleted.

[Before correction]

PSEL[4:0] Settings	Pin			
	PC4	PC5	PC6	PC7
11001b	TSCAP	TS23	TS22	—
11010b	SDHI_D1	—	—	—

[After correction]

PSEL[4:0] Settings	Pin			
	PC4	PC5	PC6	PC7
11001b	TSCAP	TS23	TS22	—