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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A040A/E	Rev.	1.00
Title	Changes in the Voltage Monitor 2 Interrupt Specifications		Information Category	Technical Notification		
Applicable Products	See below	Lot No. –	Reference Document			

Specifications for the voltage monitor 2 interrupt have been partially modified in the products below.

1. Applicable products:

   R8C/11 Group, R8C/13 Group,

   R8C/14 Group, R8C/15 Group, R8C/16 Group, R8C/17 Group

   R8C/18 Group, R8C/19 Group, R8C/1A Group, R8C/1B Group

2. Change:

   When in voltage monitor 2 interrupt mode (VW2C6 bit in the VW2C register is 0), regardless of the setting of the VW2C1 bit in the VW2C register (voltage monitor 2 digital filter disabled mode select bit), an interrupt request is generated when Vdet2 > VCC and when VCC > Vdet2.

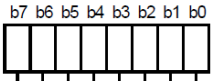
3. Examples of changes to the hardware manual (R8C/1A Group, R8C/1B Group (REJ09B0252-0130)).

Table 7.1 Specifications of Voltage Detection Circuit

Item		Voltage Detection 1	Voltage Detection 2
VCC monitor	Voltage to monitor	Vdet1	Vdet2
	Detection target	Passing through Vdet1 by rising or falling	Passing through Vdet2 by rising or falling
	Monitor	None	VCA13 bit in VCA1 register
			Whether VCC is higher or lower than Vdet2
Process when voltage is detected	Reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset at Vdet1 > VCC; restart CPU operation at VCC > Vdet1	Reset at Vdet2 > VCC; restart CPU operation after a specified time
	Interrupt	None	Voltage monitor 2 interrupt
			~~Interrupt request at Vdet2 > VCC and VCC > Vdet2 when digital filter is enabled; interrupt request at Vdet2 > VCC or VCC > Vdet2 when digital filter is disabled~~
Digital filter	Switch enabled/disabled	Available	Available
	Sampling time	(Divide-by-n of fRING-S) x 4 n: 1, 2, 4, and 8	(Divide-by-n of fRING-S) x 4 n: 1, 2, 4, and 8

Interrupt request at Vdet2 > VCC and VCC > Vdet2

Voltage Monitor 2 Circuit Control Register (1)



Symbol	Address	After Reset(8)
VW2C	0037h	00h

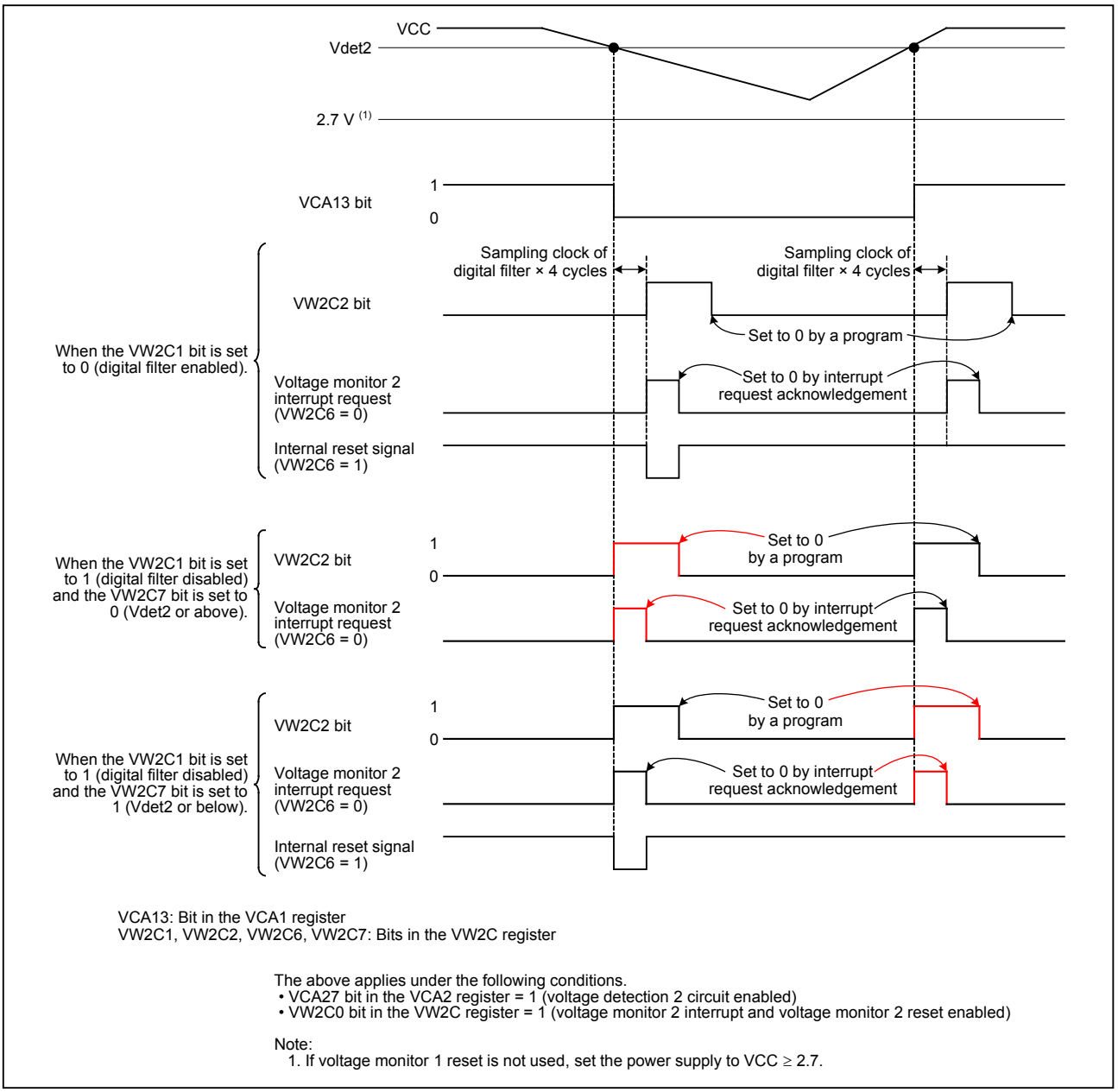
Bit Symbol	Bit Name	Function	RW
VW2C0	Voltage monitor 2 interrupt / reset enable bit(6, 10)	0 : Disable 1 : Enable	RW
VW2C1	Voltage monitor 2 digital filter disabled mode select bit(2)	0 : Digital filter enabled mode (digital filter circuit enabled) 1 : Digital filter disabled mode (digital filter circuit disabled)	RW
VW2C2	Voltage change detection flag(3,4,8)	0 : Not detected 1 : Vdet2 crossing detected	RW
VW2C3	WDT detection flag(4,8)	0 : Not detected 1 : Detected	RW
VW2F0	Sampling clock select bits	b5 b4 0 0 : fRING-S divided by 1 0 1 : fRING-S divided by 2 1 0 : fRING-S divided by 4 1 1 : fRING-S divided by 8	RW
VW2F1			RW
VW2C6	Voltage monitor 2 circuit mode select bit(5)	0 : Voltage monitor 2 interrupt mode 1 : Voltage monitor 2 reset mode	RW
VW2C7	Voltage monitor 2 interrupt / reset generation condition select bit(7,9)	0 : When VCC reaches Vdet2 or above. 1 : When VCC reaches Vdet2 or below.	RW

NOTES :

1. Set the PRC3 bit in the PRCR register to 1 (rewrite enable) before writing to this register. When rewriting the VW2C register, the VW2C2 bit may be set to 1. Set the VW2C2 bit to 0 after rewriting the VW2C register.
2. When the voltage monitor 2 interrupt is used to exit stop mode and to return again, write 0 to the VW2C1 bit before writing 1.
3. This bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, it is set to 0 (and remains unchanged even if 1 is written to it).
5. This bit is enabled when the VW2C0 bit is set to 1 (voltage monitor 2 interrupt/reset enabled).
6. The VW2C0 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disable) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled).
7. The VW2C7 bit is enabled when the VW2C1 bit is set to 1 (digital filter disabled mode).
8. Bits VW2C2 and VW2C3 remain unchanged after a software reset, watchdog timer reset, or voltage monitor 2 reset.
9. When the VW2C6 bit is set to 1 (voltage monitor 2 reset mode), set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below). (Do not set to 0.)
10. Set the VW2C0 bit to 0 (disabled) when the VCA13 bit in the VCA1 register is set to 1 (VCC ≥ Vdet2 or voltage detection 2 circuit disabled), the VW2C1 bit is set to 1 (digital filter disabled mode), and the VW2C7 bit is set to 0 (when VCC reaches Vdet2 or above).
    Set the VW2C0 bit to 0 (disabled) when the VCA13 bit is set to 0 (VCC < Vdet2), the VW2C1 bit is set to 1 (digital filter disabled mode), and the VW2C7 bit is set to 1 (when VCC reaches Vdet2 or below).

Figure 7.6 VW2C Register

The VW2C7 bit is disabled when the VW2C6 bit is 0 (voltage monitor 2 interrupt mode).



VCA13: Bit in the VCA1 register
VW2C1, VW2C2, VW2C6, VW2C7: Bits in the VW2C register

The above applies under the following conditions.
- VCA27 bit in the VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in the VW2C register = 1 (voltage monitor 2 interrupt and voltage monitor 2 reset enabled)

Note:
1. If voltage monitor 1 reset is not used, set the power supply to VCC ≥ 2.7.

Figure 7.9 Operating Example of Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset

Table 7.3 Setting Procedure of Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset Associated Bits

Step	When Using Digital Filter		When Not Using Digital Filter	
	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).			
2	Wait for td(E-A)			
3(2)	Select the sampling clock of the digital filter by bits VW2F0 to VW2F1 in the VW2C register.		Select the timing of the ~~interrupt and~~ reset request by the VW2C7 bit in the VW2C register(1).	
4(2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).		Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).	
5(2)	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode).	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode).
6	Set the VW2C2 bit in the VW2C register to 0 (passing of Vdet2 is not detected).			
7	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).		–	
8	Wait for 4 cycles of the sampling clock of the digital filter		– (No wait time)	
9	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt/reset enabled).			

NOTES:
1. Set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below) for the voltage monitor 2 reset.
2. When the VW2C0 bit is set to 0 (disabled), steps 3, 4 and 5 can be executed simultaneously (with 1 instruction).