

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0283A/E	Rev.	1.00
Title	Changes to the User's Manuals: Hardware for the RX26T and RX660 Groups regarding the Data Transfer Rate of the CANFD		Information Category	Technical Notification		
Applicable Product	RX26T Group, RX660 Group	Lot No.	Reference Document	RX26T Group User's Manual: Hardware Rev.1.10 (R01UH0979EJ0110) RX660 Group User's Manual: Hardware Rev.1.00 (R01UH0937EJ0100)		
		All				

This document describes the changes regarding the data transfer rate for communications of the CANFD module in the user's manuals: hardware for the applicable products stated above.

The page, section, table, and figure numbers below are for the manual for the RX26T group. See the table on the following page for the corresponding page, section, table, and figure numbers in the manual for the RX660 group.

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Note 2 is added as follows to the description of Data transfer rate in Table 36.1, CAN FD Module Specifications, in section 36.1, Overview.

Before correction

Table 36.1 CAN FD Module Specifications

Item	Description
Protocol	ISO 11898-1:2015 compliant
Data transfer rate	Arbitration phase: up to 1 Mbps Data phase: up to 8 Mbps ¹
Operating frequency ²	Register block: up to 60 MHz (PCLKB) Message buffer RAM: up to 120 MHz (PCLKA)
(Omitted)	

Note 1. This is only available for products that support the CAN FD protocol.

Note 2. The frequency ratio of PCLKA and PCLKB should be 2 : 1. Also, the frequency of PCLKB should be equal to or higher than that of the DLL clock.

After correction

Table 36.1 CAN FD Module Specifications

Item	Description
Protocol	ISO 11898-1:2015 compliant
Data transfer rate	Arbitration phase: up to 1 Mbps Data phase: up to 8 Mbps ^{1,2}
Operating frequency ³	Register block: up to 60 MHz (PCLKB) Message buffer RAM: up to 120 MHz (PCLKA)
(Omitted)	

Note 1. This is only available for products that support the CAN FD protocol.

Note 2. The bit rate for communications depends on the board design and external environment. Determine it following sufficient evaluation.

Note 3. The frequency ratio of PCLKA and PCLKB should be 2 : 1. Also, the frequency of PCLKB should be equal to or higher than that of the DLL clock.

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Table 49.43 CANFD Timing, in section 49.4.5.16, CANFD, is changed as follows, and a figure is newly added.

Before correction

Table 49.43 CANFD Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = T_{opr}

Item		Symbol	Min.	Max.	Unit
Classic CAN mode	Bit rate for communications		—	1	Mbps
	Bit rate for communications (only for data)		—	5	Mbps

After correction

Table 49.43 CANFD Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = T_{opr},
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Internal delay time	t _{NODE}	—	50	ns	Figure 49.77

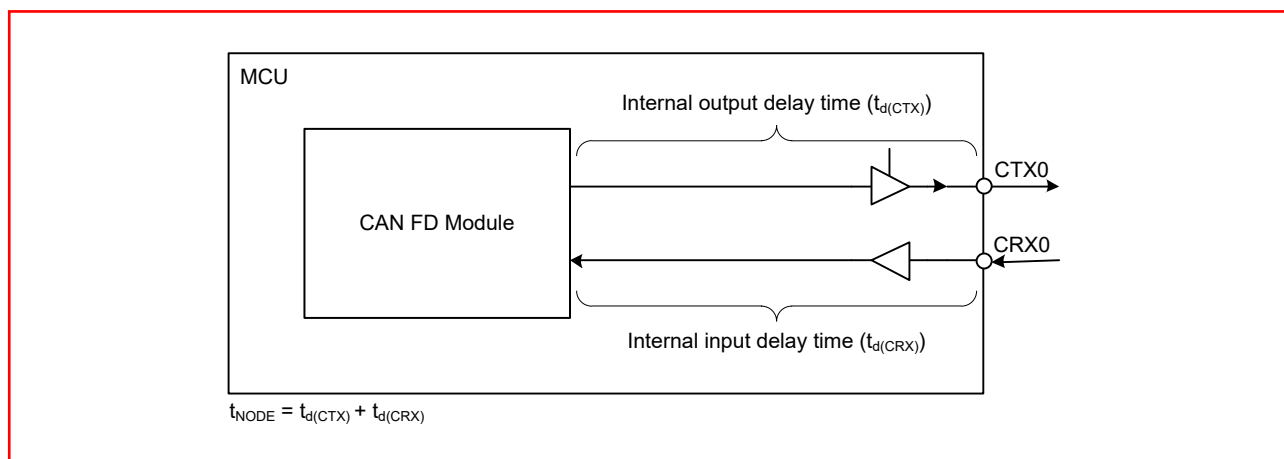


Figure 49.77 Definition of Internal Delay Time

• Reference Document

Group	Manual Title (Document Number)	Page	Section	Table	Figure
RX26T Group	RX26T Group User's Manual: Hardware Rev.1.10 (R01UH0979EJ0110)	2051 of 2917	36.1	Table 36.1	—
		2891 of 2917	49.4.5.16	Table 49.43	Figure 49.77
RX660 Group	RX660 Group User's Manual: Hardware Rev.1.00 (R01UH0937EJ0100)	1572 of 2278	33.1	Table 33.1	—
		2253 of 2278	45.4.6.12	Table 45.42	Figure 45.59