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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A226A/E	Rev.	1.00
Title	Change in the CPU Operation Frequency for the M16C/63 Group		Information Category	Technical Notification		
Applicable Product	M16C/63 Group	Lot No. —	Reference Document	M16C/63 Group User's Manual: Hardware Rev.2.00 (R01UH0137EJ0200)		

In the Electrical Characteristics chapter of the M16C/63 Group user's manual, the CPU operation clock ($f_{(BCLK)}$) contained misinformation. The information has been corrected.

1. Description

The recommended operating condition of $f_{(XIN)}$ is a maximum of 10 MHz when 1.8 V ≤ V_{CC1} < 2.7 V. However $f_{(BCLK)}$ exceeds 10 MHz in the range of 1.8 V ≤ V_{CC1} < 2.7 V in the figure showing the relation between $f_{(BCLK)}$ and V_{CC1}.

2. Modification

This section describes changes showing premodifications and post modifications according to the M16/63 Group User's Manual: Hardware Rev.2.00 (R01UH0137EJ0200).

Premodification:

• Excerpt from Table 31.4 Recommended Operating Conditions (3/4) on page 740

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock input oscillation frequency	2.7 V ≤ V_{CC1} ≤ 5.5 V	1		20	MHz
		1.8 V ≤ V_{CC1} < 2.7 V	1		10	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768		kHz
$f_{(BCLK)}$	CPU operation clock	2.7 V ≤ V_{CC1} ≤ 5.5 V			20	MHz
		1.8 V ≤ V_{CC1} < 2.7 V			(Note 2)	MHz

Notes:
2. Calculated by the following equation according to V_{CC1}: 16.67 x V_{CC1} - 25 [MHz]
See Figure 31.1 "Relation between $f_{(BCLK)}$ and V_{CC1}"

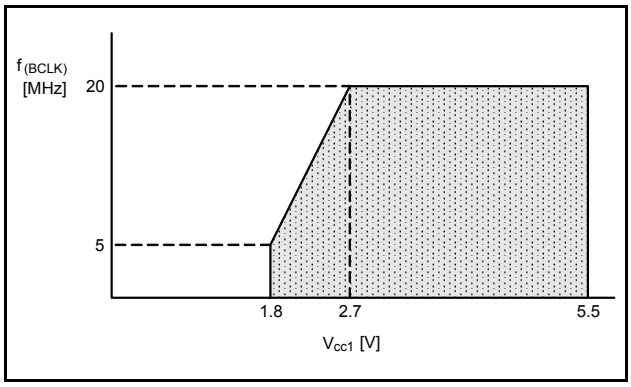
Post modification:

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock input oscillation frequency	2.7 V ≤ V_{CC1} ≤ 5.5 V	1		20	MHz
		1.8 V ≤ V_{CC1} < 2.7 V	1		10	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768		kHz
$f_{(BCLK)}$	CPU operation clock	2.7 V ≤ V_{CC1} ≤ 5.5 V, **1 MHz ≤ $f_{(XIN)}$ ≤ 20 MHz**			20	MHz
		2.1 V ≤ V_{CC1} < 2.7 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 10 MHz			**10**	**MHz**
		1.8 V ≤ V_{CC1} < 2.1 V, 1 MHz ≤ $f_{(XIN)}$ ≤ 10 MHz			(Note 2)	MHz

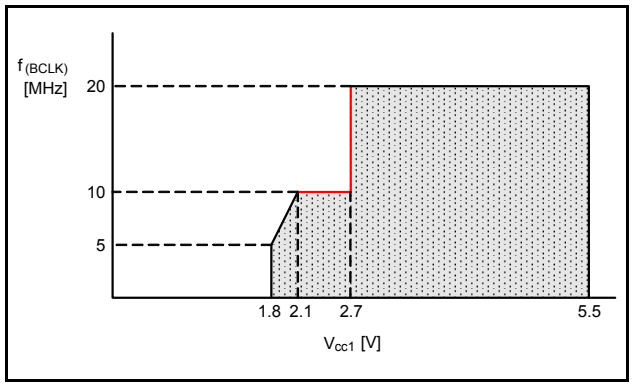
Notes:
2. Calculated by the following equation according to V_{CC1}: 16.67 x V_{CC1} - 25 [MHz]
See Figure 31.1 "Relation between $f_{(BCLK)}$ and V_{CC1}"

Premodification:

- Excerpt from Figure 31.1 Relation between $f_{(BCLK)}$ and V_{CC1} on page 741



Post modification:



Supplement

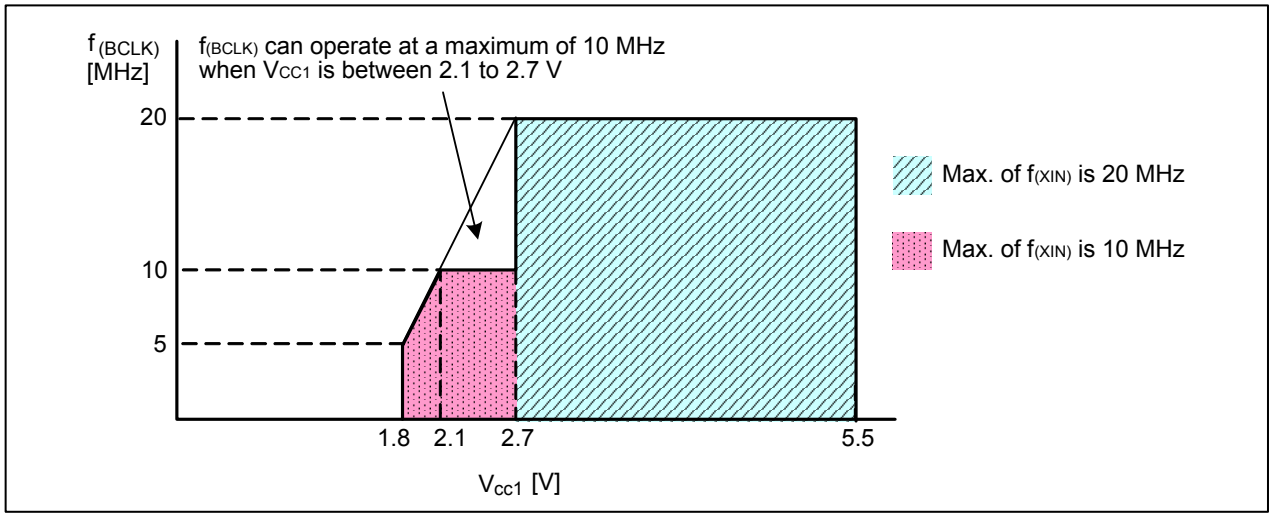


Figure 1. Relation between $f_{(BCLK)}$ and V_{CC1}