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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A060A/E	Rev.	1.00
Title	Caution on using wait mode and stop mode		Information Category	Technical Notification		
Applicable Product	R8C/36T-A, R8C/38T-A	Lot No. _	Reference Document	Latest user's Manual: Hardware of applicable products		

This caution below applies to wait mode and stop mode in the above mentioned Applicable Products.

1. Description

The Interrupt request bit(IR bit) of the Interrupt Control Register may not be set to "1"(Interrupt requested), when two or more peripheral function interrupts to be used for exiting wait mode/stop mode are generated simultaneously under the condition that there are two or more peripheral functions and their operations in wait mode/stop mode are enabled [Note 1]. In this case, the interrupt request flag will not be set to “1” and interrupt processing will not be executed even though another same interrupt source is generated.

Note 1. The peripheral functions, the interrupt request bit (the IR bit in the corresponding interrupt control register) of which is set to “1” (interrupt requested) in wait mode/stop mode.

2. Conditions

The problem described above occurs when all the following conditions are met.

(1) In Wait mode/Stop mode

(2) There are two or more peripheral functions and their operations in wait mode/stop mode are enabled.

3. Countermeasure

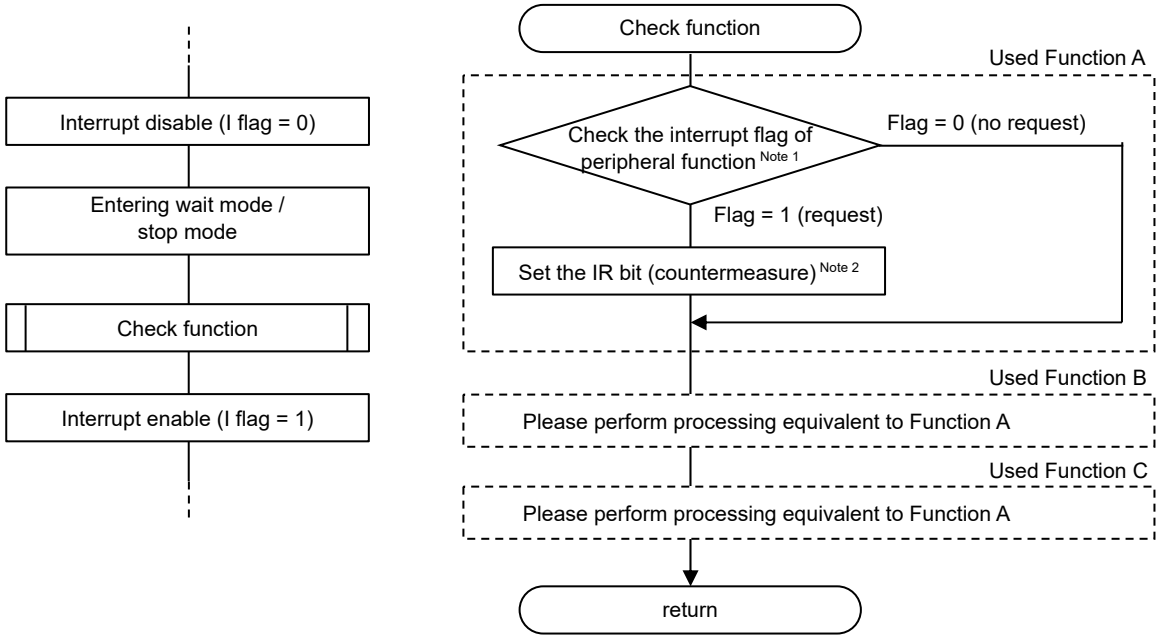
Execute the following countermeasure in your software.

・Setting the I flag of flag register to "0"(disable interrupts) before entering wait mode/stop mode.

・After exiting wait mode/stop mode, check the interrupt request flag of the peripheral function.

・If the peripheral function interrupt flag is set to "1", set the IR bit in the corresponding interrupt control register to "1".

・And then, setting the I flag of flag register to "1"(enable interrupts). In this way, the interrupts which have been generated can be processed properly.



Note 1. The timer RC, timer RD, timer RE2, and synchronous serial communication unit/ I^2C bus interface interrupts each have multiple interrupt request sources. An interrupt request is generated by the logical OR of those interrupt request sources. Check the interrupt flags that are the bits of enabled interrupt request source status register (status register) by interrupt request source enable register (enable register). Branch to "Flag = 0" when interrupt request source enable register is disabled.

Note 2. Use the MOV instruction when setting the IR bit in the interrupt control register to "1" as a measure for this caution (caution on using wait mode and stop mode).

Figure. Flowchart of countermeasure

3.1 Caution on software measures

・ To enter wait mode, disable the interrupts (set the I flag in the Flag register (FLG) to "0") and set the CM30 bit in the CM3 register to "1". Don't use the WAIT instruction.

・ To enter stop mode, disable the interrupts (set the I flag in the Flag register (FLG) to "0") and set the CM10 bit in the CM1 register to "1".

・ When an "interrupt-judging function" is called as a measure for this caution (caution on using wait mode and stop mode), the stack area are consumed.

3.2 Description of judgement bit

The following table shows the interrupt source, the interrupt flags of its peripheral functions and the interrupt request bit.

Table. Interrupt flag of the peripheral functions

Interrupt Source	Interrupt flag of the peripheral functions	Interrupt request bit	References
INT4	INT4S bit in the INTSTS register Note 2	IR bit in the INT4IC register	3.3(1) ,3.3(13)
Timer RC_0	Each bit in the TRCSR_0 register Note 1	IR bit in the TRCIC_0 register	3.3(2) ,3.3(13)
Timer RE2	Each bit in the TREIFR register Note 1	IR bit in the TRE2IC register	3.3(3) ,3.3(13)
UART2 transmit/NACK2	U2TIF bit in the U2IR register Note 2	IR bit in the U2TIC register	3.3(4) ,3.3(13)
UART2 receive/ACK2	U2RIF bit in the U2IR register Note 2	IR bit in the U2RIC register	3.3(4) ,3.3(13)
Key input	KIIS bit in the KIS register Note 2	IR bit in the KUPIC register	3.3(5) ,3.3(13)
Synchronous serial communication unit/ I^2C bus interface	Each bit in the SISR_0 register Note 1	IR bit in the SSUIC_0/ IICIC_0 register	3.3(6) ,3.3(13)
UART0_0 transmit	U0TIF bit in the U0IR_0 register Note 2	IR bit in the U0TIC_0 register	3.3(7) ,3.3(13)
UART0_0 receive	U0RIF bit in the U0IR_0 register Note 2	IR bit in the U0RIC_0 register	3.3(7) ,3.3(13)
UART0_1 transmit	U0TIF bit in the U0IR_1 register Note 2	IR bit in the U0TIC_1 register	3.3(7) ,3.3(13)
UART0_1 receive	U0RIF bit in the U0IR_1 register Note 2	IR bit in the U0RIC_1 register	3.3(7) ,3.3(13)
INT2	INT2S bit in the INTSTS register Note 2	IR bit in the INT2IC register	3.3(1) ,3.3(13)
Timer RJ_0	LINIF bit in the LINIR_0 register Note 2	IR bit in the TRJIC_0 register	3.3(8) ,3.3(13)
Timer RB2_0	TRBIF bit in the TRBIR_0 register	IR bit in the TRB2IC_0 register	3.3(9) ,3.3(13)
INT1	INT1S bit in the INTSTS register Note 2	IR bit in the INT1IC register	3.3(1) ,3.3(13)
INT3	INT3S bit in the INTSTS register Note 2	IR bit in the INT3IC register	3.3(1) ,3.3(13)
INT0	INT0S bit in the INTSTS register Note 2	IR bit in the INT0IC register	3.3(1) ,3.3(13)
UART2 bus collision detection	U2BCNIF bit in the U2IR register Note 2	IR bit in the U2BCNIC register	3.3(4) ,3.3(13)
Voltage monitor 1 Note 3	VW1C2 bit in the VW1C register	IR bit in the VCMP1IC register	3.3(10) ,3.3(13)
Voltage monitor 2 Note 3	VW2C2 bit in the VW2C register	IR bit in the VCMP2IC register	3.3(11) ,3.3(13)
TSCU	SIF bit in the TSCUFR register	IR bit in the TSCUIC register	3.3(12) ,3.3(13)

Note:
1. The bits of status register that the corresponding interrupt enable bits are set to 1.
2. Refer to “3.3 Register and flag used in a judgement” for the details on the applicable registers and bits.
3. The interrupt source is enabled only when the maskable interrupt is selected.

3.3 Register and flag used in judgement

The red words (registers and bits) are not described in Hardware manual. In the case of not applicable, it is not necessary to change the software of these registers and bits.

(1) INT Interrupt Status Register (INTSTS)

Address: 00235h (INTSTS)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	-	-	-	INT4S	INT3S	INT2S	INT1S	INT0S
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0S	INT0 interrupt request flag Note 1,2	0: No interrupt requested 1: Interrupt requested	R/W
b1	INT1S	INT1 interrupt request flag Note 1,2		R/W
b2	INT2S	INT2 interrupt request flag Note 1,2		R/W
b3	INT3S	INT3 interrupt request flag Note 1,2		R/W
b4	INT4S	INT4 interrupt request flag Note 1,2		R/W
b5-b7	-	Reserved	Set to 0.	R/W

Note 1. [Conditions for setting to 0]
- When the corresponding IR bit changes from 1 to 0
- When 0 is written to this bit after reading it as 1.

[Conditions for setting to 1]
- When the corresponding interrupt request occurs

Note 2. The results writing this bit are as follows.
- If 1 is read, writing 0 to the same bit is to 0.
- If 0 is read, writing 0 to the same bit does not change it.（If the bit changes from 0 to 1 after a 0 is read, it remains 1 even if 0 is written.）
- The bit remains unchanged if 1 is written to it.

(2) Timer RC_0 Status Register (TRCSR_0)

Address: 00145h (TRCSR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	-	-	-	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/ compare match A flag	[Conditions for setting to 0] • When 0 is written to this bit after reading it as 1. • Set to 0 by the DTC acknowledge when the DTC is activated by an IMFi interrupt. [Condition for setting to 1] • Input Capture Function When the value of the TRCCNT register is transferred to the TRCGRA register at the input edge of the TRCIOi pin. • Output Compare Function/ PWM Mode/ PWM2 Mode When the values of registers TRCCNT and TRCGRi match. (i = A to D)	R/W
b1	IMFB	Input capture/ compare match B flag		R/W
b2	IMFC	Input capture/ compare match C flag		R/W
b3	IMFD	Input capture/ compare match D flag		R/W
b4-b6	-	Nothing is assigned. The write value must be 1. The read value is 1.		-
b7	OVF	Timer overflow flag	[Conditions for setting to 0] • When 0 is written to this bit after reading it as 1. [Condition for setting to 1] • When the TRCCNT register overflows from FFFFh to 0000h.	R/W

(3) Timer RE2 Interrupt Flag Register (TREIFR)

Real-Time Clock Mode

Address: 0017Ah (TREIFR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TADJSF	-	-	RSTADJ	ADJ30S	ALIE	RTCF	ALIF
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ALIF	Alarm interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b1	RTCF	Real-time clock periodic interrupt flag		R/W
b2	ALIE	Alarm interrupt enable bit	0: Alarm interrupt disabled 1: Alarm interrupt enabled	R/W
b3	ADJ30S	30-second adjustment bit	When 1 is written to this bit, the value of the TRESEC register changes as follows. When TRESEC register value ≦ 29: TRESEC←00 When TRESEC register value ≧ 30: TRESEC←00、TREMIN←TREMIN+1 The read value is 0.	W
b4	RSTADJ	Second counter reset adjustment bit	When 1 is written to this bit, the value of the TRESEC register is set to 00 and the initial Counter is initialized. The read value is 0.	W
b5-b6	-	Nothing is assigned. The write value must be 0. The read value is 0.		-
b7	TADJSF	Correction status flag	0: No correction 1: Being correction	R/W

Address: 0017Bh (TREIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	YRIE	MOIE	DYIE	HRIE	MNIE	SEIE	SEIE05	SEIE025
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SEIE025	Periodic interrupt triggered every 0.25 seconds enable bit	0: Periodic interrupt triggered every 0.25 seconds disable 1: Periodic interrupt triggered every 0.25 seconds enable	R/W
b1	SEIE05	Periodic interrupt triggered every 0.5 seconds enable bit	0: Periodic interrupt triggered every 0.5 seconds disable 1: Periodic interrupt triggered every 0.5 seconds enable	R/W
b2	SEIE	Periodic interrupt triggered every second enable bit	0: Periodic interrupt triggered every second disable 1: Periodic interrupt triggered every second enable	R/W
b3	MNIE	Periodic interrupt triggered every minute enable bit	0: Periodic interrupt triggered every minute disable 1: Periodic interrupt triggered every minute enable	R/W
b4	HRIE	Periodic interrupt triggered every hour enable bit	0: Periodic interrupt triggered every hour disable 1: Periodic interrupt triggered every hour enable	R/W
b5	DYIE	Periodic interrupt triggered every day enable bit	0: Periodic interrupt triggered every day disable 1: Periodic interrupt triggered every day enable	R/W
b6	MOIE	Periodic interrupt triggered every month enable bit	0: Periodic interrupt triggered every month disable 1: Periodic interrupt triggered every month enable	R/W
b7	YRIE	Periodic interrupt triggered every year enable bit	0: Periodic interrupt triggered every year disable 1: Periodic interrupt triggered every year enable	R/W

(4) UART2 Interrupt Status Register (U2IR)

Address: 000D8h (U2IR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	U2TIF	U2RIF	U2NAKIF	U2BCNIF	-	-	-	-
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0-b3	-	Reserved	Set to 0.	R/W
b4	U2BCNIF	Bus collision detection interrupt request flag Note 1,2	0: No interrupt requested 1: Interrupt requested	R/W
b5	U2NAKIF	NACK interrupt request flag Note 1,2		R/W
b6	U2RIF	Receive interrupt request flag Note 1,2		R/W
b7	U2TIF	Transmit/ACK interrupt request flag Note 1,2		R/W

Note 1. [Conditions for setting to 0]
- When the corresponding IR bit changes from 1 to 0
- When 0 is written to this bit after reading it as 1.

[Conditions for setting to 1]
- When the corresponding interrupt request occurs

Note 2. The results writing this bit are as follows.
- If 1 is read, writing 0 to the same bit is to 0.
- If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, it remains 1 even if 0 is written.)
- The bit remains unchanged if 1 is written to it.

(5) Key Input Interrupt Status Register (KIS)

Address: 00237h (KIS)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KIIS	-	-	-	-	-	-	-
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0-b6	-	Reserved	Set to 0.	R
b7	KIIS	Key input interrupt request flag Note 1,2	0: No interrupt requested 1: Interrupt requested	R/W

Note 1. [Conditions for setting to 0]
- When the corresponding IR bit changes from 1 to 0
- When 0 is written to this bit after reading it as 1.

[Conditions for setting to 1]
- When the corresponding interrupt request occurs

Note 2. The results writing this bit are as follows.
- If 1 is read, writing 0 to the same bit is to 0.
- If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, it remains 1 even if 0 is written.)
- The bit remains unchanged if 1 is written to it.

(6) SI Status Register (SISR)

SSU Function:

Address: 000EAh (SISR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	ORER_AL	AAS	CE_ADZ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE_ADZ	Conflict error flag	0: No conflict error 1: Conflict error	R/W
b1	AAS	Reserved	Set to 0.	R/W
b2	ORER_AL	Overrun error flag	0: No overrun error 1: Overrun error	R/W
b3	STOP	Reserved	Set to 0.	R/W
b4	NACKF	Reserved	Set to 0.	R/W
b5	RDRF	Receive data register full flag	0: No data in the SIRDR register 1: Data present in the SIRDR register	R/W
b6	TEND	Transmit end flag	0: The TDRE bit is 0 when the last bit of transmit data is transmitted 1: The TDRE bit is 1 when the last bit of transmit data is transmitted	R/W
b7	TDRE	Transmit data empty flag	0: Data is not transferred from registers SITDR to SISDR 1: Data is transferred from registers SITDR to SISDR	R/W

I²C bus Function:

Address: 000EAh (SISR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	ORER_AL	AAS	CE_ADZ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE_ADZ	General call address recognition flag	This flag is set to 1 when a general call address is detected.	R/W
b1	AAS	Slave address recognition flag	This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SIMR2 register in slave receive mode (slave address detection, general call address detection).	R/W
b2	ORER_AL	Arbitration lost flag/overrun error flag	In I²C bus interface mode, this flag indicates that arbitration is lost in master mode. This flag is set to 1 when: • The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode • The SDA pin is held high at start condition detection in master transmit/receive mode In clock synchronous serial mode, this bit indicates that an overrun error has occurred. This flag is set to 1 when: • The last bit of the next data is received while the RDRF bit is set to 1.	R/W
b3	STOP	Stop condition detection flag	This flag is set to 1 when a stop condition is detected after the frame is transferred.	R/W
b4	NACKF	No acknowledge detection flag	This flag is set to 1 when no ACKnowledge is detected from the receive device after transmission.	R/W
b5	RDRF	Receive data register full flag	This flag is set to 1 when receive data is transferred from registers SISDR to SIRDR.	R/W
b6	TEND	Transmit end flag	In I²C bus interface mode, this flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is 1. In clock synchronous mode, this flag is set to 1 when the last bit of the transmit frame is transmitted.	R/W
b7	TDRE	Transmit data empty flag	This flag is set to 1 when: • Data is transferred from registers SITDR to SISDR and the SITDR register becomes empty. • The TRS bit in the SICR1 register is set to 1 (transmit mode) • A start condition is generated (including retransmission) • Slave receive mode is changed to slave transmit mode	R/W

(7) UART0 Interrupt Flag and Enable Register (U0IR)

Address: 00088h (U0IR_0), 00098h (U0IR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	U0TIF	U0RIF	-	-	U0TIE	U0RIE	-	-
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0-b1	-	Nothing is assigned. The write value must be 0. The read value is 0.		-
b2	U0RIE	UART0 receive interrupt enable bit	0: Receive interrupt disabled 1: Receive interrupt enabled	R/W
b3	U0TIE	UART0 transmit interrupt enable bit	0: Transmit interrupt disabled 1: Transmit interrupt enabled	R/W
b4-b5	-	Nothing is assigned. The write value must be 0. The read value is 0.		-
b6	U0RIF	UART0 receive interrupt request flag Note 1,2	0: No interrupt requested 1: Interrupt requested	R/W
b7	U0TIF	UART0 transmit interrupt request flag Note 1,2		R/W

Note 1. [Conditions for setting to 0]
- When the corresponding IR bit changes from 1 to 0
- When 0 is written to this bit after reading it as 1.

[Conditions for setting to 1]
- When the corresponding interrupt request occurs

Note 2. The results writing this bit are as follows.
- If 1 is read, writing 0 to the same bit is to 0.
- If 0 is read, writing 0 to the same bit does not change it.（If the bit changes from 0 to 1 after a 0 is read, it remains 1 even if 0 is written.）
- The bit remains unchanged if 1 is written to it.

(8) Timer RJ/ LIN Interrupt Request Register (LINIR)

Address: 0008Dh (LINIR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	-	-	-	-	-	-	-	TRJIF
After Reset	X	X	X	X	X	X	X	0

Bit	Symbol	Bit Name	Function	R/W
b0	LINIF	Timer RJ/ LIN interrupt request flag Note 1,2	0: No interrupt requested 1: Interrupt requested	R/W
b1-b7	-	Nothing is assigned. The write value must be 0. The read value is 0.		-

Note 1. [Conditions for setting to 0]
- When the corresponding IR bit changes from 1 to 0
- When 0 is written to this bit after reading it as 1.

[Conditions for setting to 1]
- When the corresponding interrupt request occurs

Note 2. The results writing this bit are as follows.
- If 1 is read, writing 0 to the same bit is to 0.
- If 0 is read, writing 0 to the same bit does not change it.（If the bit changes from 0 to 1 after a 0 is read, it remains 1 even if 0 is written.）
- The bit remains unchanged if 1 is written to it.

(9) Timer RB2 Interrupt Request Register (TRBIR)

Address: 00137h (TRBIR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRBIE	TRBIF	-	-	-	-	-	-
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0-b5	-	Nothing is assigned. The write value must be 0. The read value is 0.		-
b6	TRBIF	Timer RB2 interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b7	TRBIE	Timer RB2 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W

(10) Voltage Monitor 1 Circuit Control Register (VW1C)

Address: 00039h (VW1C)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	-	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit	0: Disabled 1: Enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter mode select bit	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag	0: Not detected 1: Detected by passing through Vdet1	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bits	00b: fLOCO divided by 1 01b: fLOCO divided by 2 10b: fLOCO divided by 4 11b: fLOCO divided by 8	R/W
b5	VW1F1			R/W
b6	-	Reserved	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit	0: VCC reaches Vdet1 or above 1: VCC reaches Vdet1 or below	R/W

(11) Voltage Monitor 2 Circuit Control Register (VW2C)

Address: 0003Ah (VW2C)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW2C7	-	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW2C0	Voltage monitor 2 interrupt enable bit	0: Disabled 1: Enabled	R/W
b1	VW2C1	Voltage monitor 2 digital filter mode select bit	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	VW2C2	Voltage change detection flag	0: Not detected 1: Detected by passing through Vdet2	R/W
b3	VW2C3	Voltage detection 2 signal monitor flag	0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detection 2 circuit disabled	R
b4	VW2F0	Sampling clock select bits	00b: fLOCO divided by 1 01b: fLOCO divided by 2 10b: fLOCO divided by 4 11b: fLOCO divided by 8	R/W
b5	VW2F1			R/W
b6	-	Reserved	Set to 0.	R/W
b7	VW2C7	Voltage monitor 2 interrupt generation condition select bit	0: VCC reaches Vdet2 or above 1: VCC reaches Vdet2 or below	R/W

(12) TSCU Flag Register (TSCUFR)

Address: 06B12h (TSCUFR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SIF	-	-	-	-	MVF	OVFER	DTSR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTSR	Data transfer status flag	[Conditions for setting to 0] • When data transfer to RAM is completed. • When 1 is written to the TSCUINT bit in the TSCUCR0 register. Note1 [Condition for setting to 1] •When data 1 is captured to the buffer. • When the primary counter overflows.	R
b1	OVFER	Overflow error flag	[Conditions for setting to 0] • When 1 is written to the TSCUINT bit in the TSCUCR0 register. Note1 • When 0 is written by program. [Condition for setting to 1] When the primary counter overflows.	R/W
b2	MVF	TSCU operation flag	0: Touch sensor control unit is stopped 1: Touch sensor control unit is in operation	R
b6- b3	-	Nothing is assigned. The write value must be 0. The read value is 0.		-
b7	SIF	TSCU interrupt request flag	[Sources for setting to 0] • When 1 is written to the TSCUINT bit in the TSCUCR0 register. Note1 • When 0 is written after read. Note2 [Sources for setting to 1] When a measurement of the touch sensor is completed.	R/W

Note 1. This flag is not set to 0 only by setting the TSCUSTRT bit in the TSCUCR0 register to 0 (measurement stops).

Note 2. The results writing this bit are as follows.

・If 1 is read, writing 0 to the same bit is to 0.

・If 0 is read, writing 0 to the same bit does not change it.（If the bit changes from 0 to 1 after a 0 is read, it remains 1 even if 0 is written.）

・The bit remains unchanged if 1 is written to it.

(13) Interrupt Control Register

Address: 00041H (FMRDYIC), 00046H (INT4IC), 00047H (TRCIC_0), 0004AH (TRE2IC), 0004BH (U2TIC), 0004CH (U2RIC), 0004DH (KUPIC), 0004EH (ADIC), 0004FH (SSUIC_0/ IICIC_0), 00051H (U0TIC_0), 00052H (U0RIC_0), 00053H (U0TIC_1), 00054H (U0RIC_1), 00055H (INT2IC), 00056H (TRJIC_0), 00058H (TRB2IC_0), 00059H (INT1IC), 0005AH (INT3IC), 0005DH (INT0IC), 0005EH (U2BCNIC), 0006BH (TRGIC), 00072H (VCMP1IC), 00073H (VCMP2IC), 00075H (TSCUIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	-	-	-	-	IR	ILVL2	ILVL1	ILVL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bits	000B: Level 0 (interrupt disabled) 001B-111B: Level 1 to Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W Note
b4-b7	-	Nothing is assigned. The write value must be 0. The read value is 0.		-

Note. Only 0 can be written to the IR bit. (Do not write 1 to this bit.) However, a case to use as this measure is excluded. In this case, use the MOV instruction when setting the IR bit in the interrupt control register to “1” as a measure for “caution on using wait mode and stop mode”.

3.4 Example of software measures (using wait mode)

Examples of the software measures when using wait mode are shown below.

Example)

Interrupts to exit wait mode: Timer RE2 interrupt (ILVL=1), Periodic interrupt triggered every second enable bit (SEIE=1)

INT0 interrupt (ILVL=6)

The peripheral functions the operations of which are enabled in wait mode: INT1 interrupt (ILVL=0)

Entering wait mode		Descriptions
BCLR	1, FMR0	CPU rewrite mode disabled
BSET	0, PRCR	Writing to CM3 register enabled
FCLR	I	Interrupt disabled
BSET	0, CM3	Enter wait mode
NOP		
NOP		
NOP		
NOP		
BCLR	0, PRCR	Writing to CM3 register disabled (Protection enabled)
JSR	CHECK_ICU	The check function is called
FSET	I	Interrupt enabled
NOP		NOP instruction

Check function		Descriptions
CHECK_ICU:		
BTST	1, TREIFR	Judge the RTCF bit
JNC	CHK_ICU001	Branch to the label when RTCF bit is 0
MOV.B	#009H, TRE2IC	Set the IR bit (Countermeasure)
CHK_ICU001:		
BTST	0, INTSTS	Judge the INT0S bit
JNC	CHK_ICU002	Branch to the label when INT0S bit is 0
MOV.B	#00EH, INT0IC	Set the IR bit (Countermeasure)
CHK_ICU002:		
BTST	1, INTSTS	Judge the INT1S bit
JNC	CHK_ICU003	Branch to the label when INT1S bit is 0
MOV.B	#008H, INT1IC	Set the IR bit (Countermeasure)
CHK_ICU003:		
RTS		Return to subroutine

3.5 Example of software measures (using stop mode)

Examples of the software measures when using stop mode are shown below.

Example)

Interrupts to exit wait mode: INT1 interrupt (ILVL=7), INT0 interrupt (ILVL=5)

Entering stop mode		Descriptions
BCLR	1, FMR0	CPU rewrite mode disabled
BSET	0, PRCR	Writing to CM1 register enabled
FCLR	I	Interrupt disabled
BSET	0, CM1	Enter stop mode（CM10=1）
JMP.B	LABEL_001	Branches to the label
LABEL_001:		
NOP		
NOP		
NOP		
NOP		
BCLR	0, PRCR	Writing to CM1 register disabled (Protection enabled)
JSR	CHECK_ICU	The check function is called
FSET	I	Interrupt enabled
NOP		NOP instruction

Check function		Descriptions
CHECK_ICU:		
BTST	1, INTSTS	Judge the INT1S bit
JNC	CHK_ICU001	Branch to the label when INT1S bit is 0
MOV.B	#00FH, INT1IC	Set the IR bit (Countermeasure)
CHK_ICU001:		
BTST	0, INTSTS	Judge the INT0S bit
JNC	CHK_ICU002	Branch to the label when INT0S bit is 0
MOV.B	#00DH, INT0IC	Set the IR bit (Countermeasure)
CHK_ICU002:		
RTS		Return to subroutine