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Old Company Name in Catalogs and Other Documents

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HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	28 September 2001		No.	TN-SH7-360A/E
THEME	BREQ from external device and refresh of DRAM/synchronous DRAM			
CLASSIFICATION	☐ Spec change ☐ Supplement of Documents	■ Limitation on Use		
PRODUCT NAME	HD6417751			Lot No.etc. ALL
REFERENCE DOCUMENTS	SH7751 Hardware Manual		Rev.	EffectiveDate
			1-2	From Eternity

1.   Contents

We would like to inform you that there are some notes on using BREQ# from the external device.

      1.1.   SH-4 may hung up when BREQ# is input to SH-4 under the following conditions.

      1.2.   SH-4 may assert BACK# to low only one cycle by CKIO when BREQ# is input under

           the following conditions.

           [Conditions]

           (1) in the master mode (MD7=1)

           (2) using PCIC's DMA transfer or target transfer

           (3) using CAS before RAS refresh/auto refresh for DRAM/synchronous DRAM.

2.   Workaround

There are two workarounds available to avoid these two phenomena.

      2.1.   Don't use BREQ# signal.

      2.2.   Clear the MCR.RFSH to 0, when the normal operation is running. When the REFRESH for DRAM/synchronous DRAM should be operated, clear BCR1.BREQEN to 0 and do the refresh operation. The operation flow is as follows.

[Refresh operation flow]

Set RTCSR to occur the Compare-match interrupt at intervals that are required by DRAM/synchronous DRAM connected to SH-4.

Do the operation in the following order in SR.BL=1, when the Compare-match interrupt occurs.

a.   Clear BCR1.BREQEN to 0 not to accept the bus requests from PCIC and the external devices. Clear DMAOR.DME to 0 to stop DMAC.

b.   Do the dummy read operation from the external memory through P2 space to confirm that both PCIC and the external devices have released the bus.

c.   Disable the Compare-match interrupt, set the refresh intervals. (Set RTCSR, RTCNT, RTCOR, and RFCR.)

d. Set MCR.RFSH to 1, and continue the refresh operation until RFCR.OVF = 1.

e. Clear the MCR.RFSH to 0.

f. Restore RTCSR and RTCOR to the value before changed in (c), clear RTCSR.CMF to 0.

g. Enable the Compare-match interrupt. (Set RTCSR, RTCNT, and RTCOR)

h. Set BCR1.BREQEN to 1 to accept the request from PCIC and the external devices. Set DMAOR.DME to 1 to restart DMAC, if DMAC is used.

i. Return to main routine. (SR.BL=0)

[Note]

If BCR.BREQEN is not changed in other routines, SR.BL can be cleared to 0 and the multiple interrupts can be accepted after clearing RTCSR.CMF to 0 at the end of step (c).

3. Setting minimum refresh intervals

Set RTCOR and RTCSR to minimize the refresh intervals for shortening total refresh time. When using workaround 2.2 and the refresh interval is too short, the refresh operation occupy the local BUS (SH BUS), so CPU, PCIC and DMA can't access the SH bus during refreshing. (PCIC can access to the external PCI device if using PIO transfers.)

The minimum refresh interval time depends on the setting of MCR.TRAS and MCR.TRC. Th minimum refresh interval time can be set to 8CKIO/1refresh, when MCR.TRAS=3'b000 and MCR.TRC = 3'b000. A example of 8CKIO/1refresh is described as below.

Example of 8CKIO/1refresh

    (MCR.TRAS=3'b000 and MCR.TRC = 3'b000)

        RTCSR=H'A508

        RTCOR=H'A502

[Note]

● The above example can be used when no external memory access occurs. (All memory access in the Compare-match interrupt handler hit to the instruction cache and the operand cache.)