Date: Nov. 28, 2011

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A825A/E	Rev.	1.00
Title	Amendments of SH7730 hardware manual		Information Category	Technical Notification		
Applicable Product	SH7730 Group	Lot No. All	Reference Document	SH7730 Hardware Manual Rev3.00 (REJ09B0359-0300)		

There are the amendments of SH7730 hardware manual Rev3.00.

Amendments

1. Page 294 of 1170

   11.4.1 Common Control Register (CMNCR) DPRTY bit.

   Original:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	CKO STP	CKO DRV	—	—	—	—	—	—	—	DMSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BSD	MAP[1:0]		BLOCK	DPRTY[1:0]		—	—	—	—	—	END IAN	—	HIZ MEM	HIZ CNT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0/1*	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W	R/W

   Amended:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	CKO STP	CKO DRV	—	—	—	—	—	—	—	DMSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BSD	MAP[1:0]		BLOCK			—	—	—	—	—	END IAN	—	HIZ MEM	HIZ CNT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0/1*	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W

2. Page 296 of 1170

11.4.1 Common Control Register (CMNCR) DPRTY bit.

Original:

10, 9	DPRTY [1:0]	00	R/W	DMA Burst Transfer Priority Specify the priority for a refresh request/bus mastership request during DMA burst transfer. 00: Accepts a refresh request and bus mastership request during DMA burst transfer 01: Accepts a refresh request but does not accept a bus mastership request during DMA burst transfer 10: Accepts neither a refresh request nor a bus mastership request during DMA burst transfer 11: Setting prohibited

Amended:

10, 9	—	00	R	Reserved These bits are always read as 0. The write value should always be 0.

3. Page 401 of 1170

11.5.10 Bus Arbitration

Original:

Bits DPRTY[1:0] in CMNCR can select whether or not the bus request is received during DMAC burst transfer.

Amended:

The above description is deleted.

4. Page 330 of 1170

11.4.6 Refresh Timer Control/Status Register (RTCSR) CMIE bit.

Original:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CMF	CMIE	CKS[2:0]			RRC[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Amended:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CMF		CKS[2:0]			RRC[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Original:

6	CMIE	0	R/W	Compare Match Interrupt Enable Enables or disables a CMF interrupt request when the CMF bit of RTCSR is set to 1. 0: Disables the CMF interrupt request 1: Enables the CMF interrupt request

Amended:

6	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

5. Page 333 of 1170

11.4.8 Refresh Time Constant Register (RTCOR)

Original:

If the CMIE bit of the RTCSR is set to 1, an interrupt is requested by this matching signal. This request is maintained until the CMF bit in RTCSR is cleared to 0. Clearing the CMF bit in RTCSR affects only interrupts and does not affect refresh requests. This makes it possible to count the number of refresh requests during refresh by interrupts, and to specify the refresh and interval timer interrupts simultaneously.

Amended:

Clearing the CMF bit in RTCSR does not affect refresh requests.