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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

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Title	Amendments to the RX140 Group User's Manual: Hardware Rev.1.10		Information Category	Technical Notification		
Applicable Product	RX140 Group	Lot No. All	Reference Document	RX140 Group User's Manual: Hardware Rev.1.10 (R01UH0905EJ0110)		

This document describes corrections to the RX140 Group User's Manual: Hardware Rev.1.10.

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A statement in the first paragraph of section 3.1, Operating Mode Types and Selection, is corrected as follows.

Before correction

Operating modes are selected by the pin level when a reset is released.

After correction

The operating mode is selectable in either of the following ways.

- Level on the mode-setting pin (MD) on release from a reset (an RES# pin reset or power-on reset)
- Control by software following release from the reset state

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In Table 6.2, Targets Initialized by Each Reset Source, the voltage monitoring 0 reset is deleted from the set of reset sources associated with setting the operating mode.

Before correction

Table 6.2 Targets Initialized by Each Reset Source

Target to be Initialized	Reset Source						
	RES# Pin Reset	Power-On Reset	Voltage Monitoring 0 Reset	Independent Watchdog Timer Reset	Voltage Monitoring 1 Reset	Voltage Monitoring 2 Reset	Software Reset
(Omitted)							
Operating mode*3	○	○	○	—	—	—	—
Registers other than the above, CPU, and internal state	○	○	○	○	○	○	○

After correction

Table 6.2 Targets for Initialization by Each Reset Source

Target to be Initialized	Reset Source						
	RES# Pin Reset	Power-On Reset	Voltage Monitoring 0 Reset	Independent Watchdog Timer Reset	Voltage Monitoring 1 Reset	Voltage Monitoring 2 Reset	Software Reset
(Omitted)							
Operating mode*3	○	○	—	—	—	—	—
Registers other than the above, CPU, and internal state	○	○	○	○	○	○	○

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Statements on restrictions are added to the description of the CKSEL[2:0] bits in section 9.2.2, System Clock Control Register 3 (SCKCR3), as follows.

Before correction

CKSEL[2:0] Bits (Clock Source Select)

These bits select the source of the system clock (ICLK), peripheral module clock (PCLKB and PCLKD), and FlashIF clock (FCLK) from low-speed on-chip oscillator (LOCO), high-speed on-chip oscillator (HOCO), the main clock oscillator, the sub-clock oscillator, and the PLL circuit.
Transitions to clock sources which are not in operation are prohibited.

After correction

CKSEL[2:0] Bits (Clock Source Select)

These bits select the source of the system clock (ICLK), peripheral module clock (PCLKB and PCLKD), and FlashIF clock (FCLK) from low-speed on-chip oscillator (LOCO), high-speed on-chip oscillator (HOCO), the main clock oscillator, the sub-clock oscillator, and the PLL circuit.
Transitions to clock sources which are not in operation are prohibited.
In middle-speed operating mode 2, do not select the main clock oscillator as the clock source.
In low-speed operating mode, the sub-clock oscillator is the only selectable clock source.

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A statement on a restriction is added to the description of Middle-Speed Operating Mode 2 in section 11.2.7, Sub Operating Power Control Register (SOPCCR), as follows.

Before correction

- Middle-Speed Operating Mode 2

As compared to middle-speed operating mode, this mode reduces power consumption for low-speed operation.
The maximum operating frequency when reading the flash memory is 1 MHz for all of ICLK, FCLK, PCLKB, and PCLKD and when the operating voltage range is between 1.8 V and 5.5 V.

After correction

- Middle-Speed Operating Mode 2

As compared to middle-speed operating mode, this mode reduces power consumption for low-speed operation. In middle-speed operating mode 2, do not select the main clock oscillator as the clock source.
The maximum operating frequency when reading the flash memory is 1 MHz for all of ICLK, FCLK, PCLKB, and PCLKD and when the operating voltage range is between 1.8 V and 5.5 V.

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A statement in the descriptions of the RSTCKSEL[2:0] bits in section 11.2.8, Sleep Mode Return Clock Source Switching Register (RSTCKCR), is corrected as follows.

Before correction

RSTCKSEL[2:0] Bits (Sleep Mode Return Clock Source Select)

The RSTCKSEL[2:0] bits select the clock source to be used at exit from sleep mode.
The clock source selected by the RSTCKSEL[2:0] bits is enabled only when the RSTCKEN bit is 1.
When making a transition from the sleep mode to the high-speed operating mode shown in Figure 11.4, the any of the LOCO, HOCO, or main clock oscillator is selectable.
When making a transition from the sleep mode to the middle-speed operating mode or the middle-speed operating mode 2, either of the LOCO, or main clock oscillator is selectable.
When making a transition from the sleep mode to the middle-speed operating mode 2, set the frequencies of each clock (ICLK, FCLK, PCLKB, and PCLKD) to 1 MHz or less.

After correction

RSTCKSEL[2:0] Bits (Sleep Mode Return Clock Source Select)

The RSTCKSEL[2:0] bits select the clock source to be used at exit from sleep mode.
The clock source selected by the RSTCKSEL[2:0] bits is enabled only when the RSTCKEN bit is 1.
When making a transition from the sleep mode to the high-speed operating mode shown in Figure 11.4, the any of the LOCO, HOCO, or main clock oscillator is selectable. When making a transition from the sleep mode to the middle-speed operating mode, either of the LOCO, or main clock oscillator is selectable. When making a transition from the sleep mode to the middle-speed operating mode 2, the LOCO is selectable. When making a transition from the sleep mode to the middle-speed operating mode 2, set the frequencies of each clock (ICLK, FCLK, PCLKB, and PCLKD) to 1 MHz or less.

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"Main clock oscillator" is deleted from the row labeled "Middle-speed operating mode 2 or low-speed operating mode after exit from middle-speed operating mode 2" in Table 11.5, When Exiting Sleep Mode to High-Speed Operating Mode and Middle-Speed Operating Mode, as follows.

Before correction

Table 11.5 When Exiting Sleep Mode to High-Speed Operating Mode and Middle-Speed Operating Mode

Operating Mode during Sleep	Clock Source during Sleep	RSTCKSEL	Operating Mode after Exiting	Clock Source after Exiting
		(Omitted)		
Middle-speed operating mode 2 or low-speed operating mode after exit from middle-speed operating mode 2	Sub-clock oscillator	000b (LOCO)	Middle-speed operating mode 2	LOCO*1
		010b (main clock oscillator)		Main clock oscillator*1

After correction

Table 11.5 When Exiting Sleep Mode to High-Speed Operating Mode and Middle-Speed Operating Mode

Operating Mode during Sleep	Clock Source during Sleep	RSTCKSEL	Operating Mode after Exiting	Clock Source after Exiting
		(Omitted)		
Middle-speed operating mode 2 or low-speed operating mode after exit from middle-speed operating mode 2	Sub-clock oscillator	000b (LOCO)	Middle-speed operating mode 2	LOCO*1

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40.2.2, Note on RAM Self-Diagnosis, is added to section 40, RAM.

After correction

40.2.2 Note on RAM Self-Diagnosis

As the RAM has a write buffer, data may be read from the write buffer rather than the RAM cells if a value is written to an address and then read from the same address. To proceed with RAM self-diagnosis by writing data and then reading the written data, follow the procedure below to ensure that the data in the RAM will be read.

(1) Write any value to the target address of self-diagnosis.
(2) Write any value to an address which is at least four locations away from that in (1).
(3) Read the data from the address to which writing proceeded in (1).

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Section 41.4.4, Data Flash Wait Cycle Setting Register (DFLWAITR) is deleted from Section 41, Flash Memory (FLASH). RX140 group products do not require the insertion of wait cycles regardless of the operating frequency.

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The characteristics listed in Table 42.40, Timing of Recovery from Low Power Consumption Modes (1), are divided into entries for “Oscillation stabilization wait time ($t_{SBYOSCWT}$)” and “Time required for operations by the sequencer before release form software standby mode (t_{SBYSEQ})” as follows. The erroneous expressions for $t_{SBYOSCWT}$ are also corrected.

Before correction

Table 42.40 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.		Unit	Test Conditions
							$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time from software standby mode*1	High-speed operating mode/ Middle-speed operating mode	Main clock oscillator operating	Main clock oscillator operating	t_{SBYMC}	—	—	t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 4 / f_{ICLK}	4 / f_{LOCO} + 11 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$	µs	Figure 42.24
			Main clock oscillator and PLL circuit operating	t_{SBYPC}			t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 4 / f_{ICLK}			
		Sub-clock oscillator operating		t_{SBYSC}			3 / f_{SOSC} + 1 / f_{ICLK}			
		HOCO clock oscillator operating		t_{SBYHO}			t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 4 / f_{ICLK}			
		Low-speed on-chip oscillator		t_{SBYLO}			t_{LOCO} + 1 / f_{ICLK}			

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).

Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.

Note 3. For n, the greatest value is selected from among the internal clock division settings.

After correction

Table 42.40 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation stabilization wait time*1	High-speed operating mode/ Middle-speed operating mode	Main clock oscillator operating	Main clock oscillator operating	$t_{SBYOSCWTMC}$	—	—	t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 1 / f_{ICLK}	µs	
			Main clock oscillator and PLL circuit operating	$t_{SBYOSCWTPC}$	—	—	t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 1 / f_{ICLK}		
		Sub-clock oscillator operating		$t_{SBYOSCWTSC}$	—	—	3 / f_{SOSC} + 1 / f_{ICLK}		
		High-speed on-chip oscillator operating		$t_{SBYOSCWTHO}$	—	—	t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 1 / f_{ICLK}		
		Low-speed on-chip oscillator operating		$t_{SBYOSCWTLO}$	—	—	t_{LOCO} + 1 / f_{ICLK}		
Time required for operations by the sequencer before release from software standby mode*2				t_{SBYSEQ}	—	—	4 / f_{LOCO} + 11 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$		
Recovery time from software standby mode*3	High-speed operating mode/ Middle-speed operating mode	Main clock oscillator operating	Main clock oscillator operating	t_{SBYMC}	—	—	$t_{SBYOSCWTMC}$ + t_{SBYSEQ}		Figure 42.24
			Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	—	$t_{SBYOSCWTPC}$ + t_{SBYSEQ}		
		Sub-clock oscillator operating		t_{SBYSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		
		High-speed on-chip oscillator operating		t_{SBYHO}	—	—	$t_{SBYOSCWTHO}$ + t_{SBYSEQ}		
		Low-speed on-chip oscillator operating		t_{SBYLO}	—	—	$t_{SBYOSCWTLO}$ + t_{SBYSEQ}		

Note 1. When multiple oscillators are operating before entry to software standby mode, the oscillation stabilization wait time will be selected as the largest value among those for the operating oscillators.

Note 2. For n, the largest value is selected from among the internal clock division settings.

Note 3. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization wait time and the time required for operations by the sequencer before release from software standby mode.

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The characteristics listed in Table 42.41, Timing of Recovery from Low Power Consumption Modes (2), are divided into entries for “Oscillation stabilization wait time ($t_{SBYOSCWT}$)” and “Time required for operations by the sequencer before release from software standby mode (t_{SBYSEQ})” as follows. The new arrangement also has separate tables for the characteristics in middle-speed operating mode 2 and the low-speed operating mode. In Table 42.41, the characteristics of t_{SBYMC} are deleted and the erroneous expressions for $t_{SBYOSCWT}$ are corrected.

Before correction

Table 42.41 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.		Unit	Test Conditions
							$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time from software standby mode*1	Middle-speed operating mode 2/Low-speed operating mode	Main clock oscillator operating	Main clock oscillator operating	t_{SBYMC}	—	—	t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 4 / f_{ICLK}	9 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$	μs	Figure 42.24
			Main clock oscillator and PLL circuit operating	t_{SBYPC}			t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 4 / f_{ICLK}			
		Sub-clock oscillator operating		t_{SBYSC}			3 / f_{SOSC} + 1 / f_{ICLK}			
		HOCO clock oscillator operating		t_{SBYHO}			t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 4 / f_{ICLK}			
		Low-speed on-chip oscillator		t_{SBYLO}			t_{LOCO} + 1 / f_{ICLK}			

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).

Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.

Note 3. For n, the greatest value is selected from among the internal clock division settings.

After correction

Table 42.41 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation stabilization wait time*1	Middle-speed operating mode 2	Main clock oscillator and PLL circuit operating	$t_{SBYOSCWTPC}$	—	—	t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 1 / f_{ICLK}	µs	
		Sub-clock oscillator operating	$t_{SBYOSCWTSC}$	—	—	3 / f_{SOSC} + 1 / f_{ICLK}		
		High-speed on-chip oscillator operating	$t_{SBYOSCWTHO}$	—	—	t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 1 / f_{ICLK}		
		Low-speed on-chip oscillator operating	$t_{SBYOSCWTLO}$	—	—	t_{LOCO} + 1 / f_{ICLK}		
Time required for operations by the sequencer before release from software standby mode*2			t_{SBYSEQ}	—	—	9 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$		
Recovery time from software standby mode*3	Middle-speed operating mode 2	Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	—	$t_{SBYOSCWTPC}$ + t_{SBYSEQ}		Figure 42.24
		Sub-clock oscillator operating	t_{SBYSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		
		High-speed on-chip oscillator operating	t_{SBYHO}	—	—	$t_{SBYOSCWTHO}$ + t_{SBYSEQ}		
		Low-speed on-chip oscillator operating	t_{SBYLO}	—	—	$t_{SBYOSCWTLO}$ + t_{SBYSEQ}		

Note 1. When multiple oscillators are operating before entry to software standby mode, the oscillation stabilization wait time will be selected as the largest value among those for the operating oscillators.
Note 2. For n, the largest value is selected from among the internal clock division settings.
Note 3. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization wait time and the time required for operations by the sequencer before release from software standby mode.

Table 42.42 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation stabilization wait time	Low-speed operating mode	Sub-clock oscillator operating	$t_{SBYOSCWTSC}$	—	—	3 / f_{SOSC} + 1 / f_{ICLK}	µs	
Time required for operations by the sequencer before release from software standby mode*1			t_{SBYSEQ}	—	—	9 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$		
Recovery time from software standby mode*2	Low-speed operating mode	Sub-clock oscillator operating	t_{SBYSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		Figure 42.24

Note 1. For n, the largest value is selected from among the internal clock division settings.
Note 2. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization wait time and the time required for operations by the sequencer before release from software standby mode.

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The characteristics listed in Table 42.42, Timing of Recovery from Low Power Consumption Modes (3), are divided into entries for “Oscillation stabilization wait time ($t_{SBYOSCWT}$)” and “Time required for operations by the sequencer before release from software standby mode (t_{SBYSEQ})” as follows. The erroneous expressions for $t_{SBYOSCWT}$ are also corrected.

Before correction

Table 42.42 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Time to shift to the snooze mode from the software standby mode*1	Main clock oscillator operating	Main clock oscillator operating	t_{SNZ}	—	—	t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 4 / f_{ICLK}	3 / f_{ICLK} + 2n / $f_{source\ clock}$	µs	Figure 42.25
		Main clock oscillator and PLL circuit operating				t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 4 / f_{ICLK}			
	Sub-clock oscillator operating					3 / f_{SOSC} + 1 / f_{ICLK}			
	HOCO clock oscillator operating					t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 4 / f_{ICLK}			
	Low-speed on-chip oscillator					t_{LOCO} + 1 / f_{ICLK}			

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).

Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.

Note 3. For n, the greatest value is selected from among the internal clock division settings.

After correction

Table 42.43 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Oscillation stabilization wait time*1	Main clock oscillator operating	Main clock oscillator operating	$t_{SBYOSCWTMC}$	—	—	t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 1 / f_{ICLK}	µs	
		Main clock oscillator and PLL circuit operating	$t_{SBYOSCWTPC}$	—	—	t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 1 / f_{ICLK}		
	Sub-clock oscillator operating		$t_{SBYOSCWTSC}$	—	—	3 / f_{SOSC} + 1 / f_{ICLK}		
	High-speed on-chip oscillator operating		$t_{SBYOSCWTHO}$	—	—	t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 1 / f_{ICLK}		
	Low-speed on-chip oscillator operating		$t_{SBYOSCWTLO}$	—	—	t_{LOCO} + 1 / f_{ICLK}		
Time required for operations by the sequencer before release from software standby mode*2			t_{SBYSEQ}	—	—	3 / f_{ICLK} + 2n / $f_{source\ clock}$		
Time to shift to the snooze mode from the software standby mode*3	Main clock oscillator operating	Main clock oscillator operating	t_{SNZMC}	—	—	$t_{SBYOSCWTMC}$ + t_{SBYSEQ}		Figure 42.25
		Main clock oscillator and PLL circuit operating	t_{SNZPC}	—	—	$t_{SBYOSCWTPC}$ + t_{SBYSEQ}		
	Sub-clock oscillator operating		t_{SNZSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		
	High-speed on-chip oscillator operating		t_{SNZHO}	—	—	$t_{SBYOSCWTHO}$ + t_{SBYSEQ}		
	Low-speed on-chip oscillator operating		t_{SNZLO}	—	—	$t_{SBYOSCWTLO}$ + t_{SBYSEQ}		

Note 1. When multiple oscillators are operating before entry to software standby mode, the oscillation stabilization wait time will be selected as the largest value among those for the operating oscillators.

Note 2. For n, the largest value is selected from among the internal clock division settings.

Note 3. The time to shift to the snooze mode from the software standby mode is determined by the value obtained by adding the oscillation stabilization wait time and the time required for operations by the sequencer before release from software standby mode.

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Table 42.43, Timing of Recovery from Low Power Consumption Modes (4), is corrected as follows.

Before correction

Table 42.43 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.*2	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed operating mode	t_{DSLP}	—	—	4 / f_{LOCO} + 10 / f_{ICLK} + 3n / $f_{source\ clock}$	μs	Figure 42.26
	Middle-speed operating mode				4 / f_{LOCO} + 10 / f_{ICLK} + 3n / $f_{source\ clock}$		
	Middle-speed operating mode 2				8 / f_{ICLK} + 3n / $f_{source\ clock}$		
	Low-speed operating mode				8 / f_{ICLK} + 3n / $f_{source\ clock}$		

After correction

Table 42.44 Timing of Recovery from Low Power Consumption Modes (5)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.*2	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed operating mode	t_{DSLP}	—	—	4 / f_{LOCO} + 8 / f_{ICLK} + 2 / f_{PCLKB} + 3n / $f_{source\ clock}$	μs	Figure 42.26
	Middle-speed operating mode				4 / f_{LOCO} + 8 / f_{ICLK} + 2 / f_{PCLKB} + 3n / $f_{source\ clock}$		
	Middle-speed operating mode 2				6 / f_{ICLK} + 2 / f_{PCLKB} + 3n / $f_{source\ clock}$		
	Low-speed operating mode				6 / f_{ICLK} + 2 / f_{PCLKB} + 3n / $f_{source\ clock}$		

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The output clock cycle time for SCI channels 6, 8, 9, and 12 in Table 42.50, SCI Timing, is corrected as follows.

Before correction

Table 42.50 SCI Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
(Omitted)								
SCI (channel 6,8,9,12)	(Omitted)							
	Output clock cycle time	Asynchronous		t_{Scyc}	16	—	t_{Pcyc}	Figure 42.39
		Clock synchronous	2.4 V ≤ VCC ≤ 5.5 V		4	—		
			1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz	8	—		
				PCLKB ≤ 24 MHz	4	—		
	(Omitted)							

After correction

Table 42.51 SCI Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
(Omitted)								
SCI (channel 6,8,9,12)	(Omitted)							
	Output clock cycle time	Asynchronous		t_{Scyc}	8	—	t_{Pcyc}	Figure 42.39
		Clock synchronous	2.4 V ≤ VCC ≤ 5.5 V		4	—		
			1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz	8	—		
				PCLKB ≤ 24 MHz	4	—		
	(Omitted)							

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A note is added to Table 42.66, Temperature Sensor Characteristics, as follows.

Before correction

Table 42.66 Temperature Sensor Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
Sampling time	—	5	—	—	µs	

After correction

Table 42.67 Temperature Sensor Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
Sampling time*1	—	5	—	—	µs	

Note 1. Set the S12AD.ADSSTRT register so that the sampling time of the 12-bit A/D converter meets this specification.

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The blank check time for 8 bytes stated in Table 42.73, ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode, is corrected as follows.

Before correction

Table 42.73 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			FCLK = 48 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
(Omitted)												
Blank check time	8-byte	t_{BC8}	—	—	45.0	—	—	8.9	—	—	8.2	µs
(Omitted)												

After correction

Table 42.74 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			FCLK = 48 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
(Omitted)												
Blank check time	8-byte	t_{BC8}	—	—	45.0	—	—	8.9	—	—	8.7	µs
(Omitted)												