To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A630A/E	Rev.	1.00
Title	Amendments of general-purpose port pins of the SH7720 hardware manual		Information Category	Technical Notification		
Applicable Product	SH7720 Group SH7721 Group	Lot No. All	Reference Document	SH7720 hardware manual Rev2.00 (REJ09B0033-0200)		

There are the amendments of general-purpose port pins of the SH7720 hardware manual.

1. Page 14 of 1382 Table 1.2 List of Pin Assignments

Original:

C14 E17 $\overline{\text{ADTRG}}$/PTF0 External trigger signal I/IO VccQ

Amended:

C14 E17 $\overline{\text{ADTRG}}$/PTF0 ADC External trigger signal/general-purpose port I/I VccQ

2. Page 32 of 1382 Table 1.3 SH7720 Pin Functions

Original:

I/O port PTF0 I/O General purpose port 7-bit general-purpose port pins

Amended:

I/O port PTF0 I General purpose port 7-bit general-purpose port pins

3. Page 1112 of 1382 Table 34.1 Multiplex Pins

Original:

E	PTE6	input (port)	AFE_RXIN input (AFEIF) / IIC_SCL output (IIC)
E	PTE5	input (port)	$\overline{\text{AFE\_RDET}}$ input (AFEIF) / IIC_SDA output (IIC)
F	PTF0	input/output (port)	$\overline{\text{ADTRG}}$ input (ADC)

Amended:

E	PTE6	input (port)	AFE_RXIN input (AFEIF) / IIC_SCL input/output (IIC)
E	PTE5	input (port)	$\overline{\text{AFE\_RDET}}$ input (AFEIF) / IIC_SDA input/output (IIC)
F	PTF0	input (port)	$\overline{\text{ADTRG}}$ input (ADC)

4. Page 1125 of 1382 34.1.6 Port F Control Register (PFCR)

Original:

Bit 1,0 PF0MD1,0 PF0 Mode 01: Port Output

Amended:

Bit 1,0 PF0MD1,0 PF0 Mode 01: Reserved

5. Page 1155 of 1382 Figure 35.5 Port E

Original:

PTE6 (input/output) / AFE_RXIN (input) / IIC_SCL (output)

PTE5 (input/output) / $\overline{\text{AFE\_RDET}}$ (input) / IIC_SDA (output)

Amended:

PTE6 (input) / AFE_RXIN (input) / IIC_SCL (input/output)

PTE5 (input) / $\overline{\text{AFE\_RDET}}$ (input) / IIC_SDA (input/output)

6. Page 1156 of 1382 Table 35.5 Port E Data Register (PEDR) Read/Write Operations

Original:

PEnMD1,0	Pin State	Read	Write
0,0	Other function	PEDR value	Value is written to PEDR, but does not affect pin state.
0,1	Output	PEDR value	Write value is output from pin.
1,0	Input (Pull-up MOS on)	Pin state	Value is written to PEDR, but does not affect pin state.
1,1	Input (Pull-up MOS off)	Pin state	Value is written to PEDR, but does not affect pin state.

Note: n = 5 to 6

Amended:

PEnMD1,0	Pin State	Read	Write
0, -	Other function	PEDR value	Value is written to PEDR, but does not affect pin state.
1, -	Input (Pull-up MOS off)	Pin state	Value is written to PEDR, but does not affect pin state.

Note: n = 5 to 6

7. Page 1157 of 1382 Figure 35.6 Port F

Original:

PTF0 (input/output) / $\overline{\text{ADTRG}}$ (input)

Amended:

PTF0 (input) / $\overline{\text{ADTRG}}$ (input)

8. Page 1158 of 1382 Table 35.6 Port F Data Register (PFDR) Read/Write Operations

Original:

PFnMD1,0	Pin State	Read	Write
0,1	Output		Reserved

Note: n = 0

Amended:

PFnMD1,0	Pin State	Read	Write
0,1	Reserved	-	-

Note: n = 0

9. Page 1347 of 1382 Table A.1 SH7720 Pin States

Original:

PLBG02 56GA-A	PLBG02 56KA-A	Pin Name	Power-On Reset	Manual Reset	Software Standby	Hardware Standby	Bus Release	I/O	Handling of Unused Pins
C14	E17	$\overline{\text{ADTRG}}$/PTF0	V	I/P	Z/K	Z/Z	I/P	I/IO	Open

Amended:

PLBG02 56GA-A	PLBG02 56KA-A	Pin Name	Power-On Reset	Manual Reset	Software Standby	Hardware Standby	Bus Release	I/O	Handling of Unused Pins
C14	E17	$\overline{\text{ADTRG}}$/PTF0	V	I/P	Z/K	Z/Z	I/P	I/I	Open